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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0098A/E	Rev.	1.00
Title	Ethernet MAC (GMAC) function issue		Information Category	Technical Notification		
Applicable Product	RZ/T2M Group RZ/N2L Group	Lot No. All	Reference Document	RZ/T2M Group User's Manual: Hardware Rev.1.00 (R01UH0916EJ0100) RZ/N2L Group User's Manual: Hardware Rev.1.10 (R01UH0955EJ0110)		

We would like to inform about issues regarding Ethernet MAC (GMAC) function as described below.

No.	Issues	Workaround
1	When the Receive FIFO operates in the cut-through mode, the Receive FIFO Read Controller may stop functioning. If this issue happens, software reset is needed to recover functioning.	Operate Receive FIFO in store and forward mode by setting bit 25 (RSF) in operation mode register (Operation_Mode) to 1.
2	Filter i Command in Remote Wake-Up Frame Filter Register (wkupfmfilter_reg[n] n＝0 to 7) is a 4-bit read-write field. When reding it, bit 1 (And_Previous) and bit 2 (INV) always return zero.	Do not use value read from this field. Software should maintain a copy of the value written to this field and use that instead of reading it.
3	Even if bit 3 (CAST) of Filter i Command in Remote Wake-Up Frame Filter Register (wkupfmfilter_reg[n] n＝0 to 7) is set to 0 to process packet with unicast address, if the packet with broadcast address is received, it is also processed to determine whether it is remote wake up packet or not. If CRC matches, it is regarded as remote wake up packet incorrectly.	Use packet with multicast address for remote wake up packet and set CAST to 1. Otherwise, when using packet with unicast address, don't use it which match the condition of packet with broadcast address.
4	When bit 1 (And_Previous) of Filter i Command in Remote Wake-Up Frame Filter Register (wkupfmfilter_reg[n] n＝0 to 7) is used to chain multiple filters, PMT interrupt is generated incorrectly if individual filters match different packets. (For example, the first packet received matches filter 0 only and then the second packet received matches filter 1 only.)	Do not use And_Previous and set it to 0. Otherwise, do not use remote wake up packet which matches defect condition.
5	When LPITXA and LPIEN bits in LPI Control and Status register (LPI_Control_Status) are set to 1, MAC transmitter may enter LPI state prematurely if TX MAC is idle but TX DMA is still active.	Set the LPITXA and LPIEN bits only after ensuring that TX DMA is in IDLE state. When bits[22:20] (TS[2:0]) in the status register (Status) indicate that the TX DMA is in Stopped or Suspend state, the TX DMA is in IDLE.