

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

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Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A675A/E	Rev.	1.00
Title	The error in the master transmission operation or the master transmission/reception operation of SSU mode.		Information Category	Technical Notification		
Applicable Product	SH7203 Group, SH7205 Group, SH7083 Group, SH7084 Group, SH7085 Group, SH7086 Group, SH7136 Group, SH7137 Group, SH7263 Group, SH7265 Group, SH7285 Group, SH7286 Group		Lot No.	Reference Document	See below	
			ALL			

We would like to inform you that the following error occurs about synchronous serial communication unit (SSU) included in the above-mentioned applicable products.

1. Error occurrence condition

In case that below 2 conditions are fulfilled in the master transmission operation or the master transmission/reception operation of SSU mode.

- (1) Set the SS control register 2 (SSCR2) as TENDSTS=1 and SCSTATS=0.
- (2) Write the next transmission data to the SS transmit data register (SSTDR) during transmission of the last bit or one bit before the last bit of the actual transmission.

2 Error phenomenon

In the next transmission, SSCK output losses 1 bit clock and the transmission is not executed correctly.

3. Workarounds

In the master transmission operation or the master transmission/reception operation of SSU mode, please operate one of the following three ways.

- (1) Please write the next transmission data to the SSTDR after the TDRE bit of the SS status register (SSSR) is set to 1 and before the transmission of one bit before the last bit starts.
- (2) Please write the next transmission data to the SSTDR after the TEND bit of the SSSR is set to 1.
- (3) Please set the SSCR2 as "TENDSTS=0" or "TENDSTS=1 and SCSATS=1".

Applicable Products and Reference Documents

Group	Reference Document Title	Rev.	Document No.
SH7203	SH7203 Group Hardware Manual	Rev.2.0	REJ09B0313-0200
SH7205	SH7205 Group Hardware Manual	Rev.1.0	REJ09B0372-0100
SH7083, SH7084, SH7085, SH7086	SH7080 Group Hardware Manual	Rev.3.0	REJ09B0181-0300
SH7136, SH7137	SH7137 Group Hardware Manual	Rev.1.0	REJ09B0402-0100
SH7263	SH7263 Group Hardware Manual	Rev.2.0	REJ09B0290-0200
SH7265	SH7265 Group Hardware Manual	Rev.1.0	REJ09B0351-0100
SH7285, SH7286	S7280 Group Hardware Manual	Rev.1.0	REJ09B0383-0100