Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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| Product Category | MPU&MCU | Document No. | TN-SH7-A598A/E | Rev. | 1.00 | |
|-----------------------|--|-------------------------|--|------|---------|--|
| Title | Error corrections in SH7147 series hardware manual (Rev1.00 | Information Category | Technical Notification | | | |
| Applicable Product | | Lot No. | Deference | | | |
| | SH7147 Group | Document | SH7147 Group Hardware Manual Rev1.0 (REJ09B0230-0100) | | Rev1.00 | |

We greatly appreciate your purchasing our semiconductor products.

We would like to inform you of the clerical error referring on-chip debugging E10A-USB in SH7147 Series Hardware Manual (Rev. 1.00). Please attend the following points.

* SH7147 series products are <u>not supported of E10A-USB emulator</u>. Please refer to "E10A-USB emulator Target devices" list on RENESAS homepage for detailed information.

1. 1. The modification

(1) Pin Function controller (PFC)

•P755-756 Port D control register L2 (PDCRL2)

[Before]

| | | Initial | | |
|-----|----------|---------|-----|--|
| Bit | Bit Name | Value | R/W | Description |
| 15 | | 0 | R | Reserved |
| | | | | This bit is always read as 0. The write value should |
| | | | | always be 0. |
| 14 | PD7MD2 | 0 | R/W | PD7 Mode |
| 13 | PD7MD1 | 0 | R/W | Select the function of the |
| 12 | PD7MD0 | 0* | R/W | PD7/D7/TXD2/SCS/AUDSYNC pin. Fixed to |
| | | | | AUDSYNC output when using the AUD function |
| | | | | of E10A. |
| | | | | 000: PD7 I/O (port) |
| | | | | 001: D7 I/O (BSC) |
| | | | | 011: AUDSYNC output (AUD) |
| | | | | 101: SCS I/O (SSU) |
| | | | | 110: TXD2 output (SCI) |
| | | | | Other than above: Setting prohibited |
| 11 | | 0 | R | Reserved |
| | | | | This bit is always read as 0. The write value should |
| | | | | always be 0. |



RENESAS TECHNICAL UPDATE TN-SH7-A598A/E

| | | Initial | | |
|-----|----------|---------|-----|--|
| Bit | Bit Name | Value | R/W | Description |
| 10 | PD6MD2 | 0 | R/W | PD6 Mode |
| 9 | PD6MD1 | 0 | R/W | Select the function of the PD6/D6/RXD2/AUDCK pin. |
| 8 | PD6MD0 | 0* | R/W | Fixed to AUDCK output when using the AUD function |
| | | | | of E10A. |
| | | | | 000: PD6 I/O (port) |
| | | | | 001: D6 I/O (BSC) |
| | | | | 011: AUDCK output (AUD) |
| | | | | 110: RXD2 input (SCI) |
| | | | | Other than above: Setting prohibited |
| 7 | | 0 | R | Reserved |
| | | | | This bit is always read as 0. The write value should |
| | | | | always be 0. |
| 6 | PD5MD2 | 0 | R/W | PD5 Mode |
| 5 | PD5MD1 | 0 | R/W | Select the function of the PD5/D5/SCK1/AUDMD pin. |
| 4 | PD5MD0 | 0* | R/W | Fixed to AUDMD input when using the AUD function |
| | | | | of E10A. |
| | | | | 000: PD5 I/O (port) |
| | | | | 001: D5 I/O (BSC) |
| | | | | 011: AUDMD input (AUD) |
| | | | | 110: SCK1 I/O (SCI) |
| | | | | Other than above: Setting prohibited |
| 3 | | 0 | R | Reserved |
| | | | | This bit is always read as 0. The write value should |
| | | | | always be 0. |
| 2 | PD4MD2 | 0 | R/W | PD4 Mode |
| 1 | PD4MD1 | 0 | R/W | Select the function of the PD4/D4/TXD1/AUDRST pir |
| 0 | PD4MD0 | 0* | R/W | Fixed to AUDRST input when using the AUD function |
| | | | | of E10A. |
| | | | | 000: PD4 I/O (port) |
| | | | | 001: D4 I/O (BSC) |
| | | | | 011: AUDRST input (AUD) |
| | | | | 110: TXD1 output (SCI) |
| | | | | Other than above: Setting prohibited |



| [After] | | | | |
|---------|----------|---------|-----|--|
| | | Initial | | |
| Bit | Bit Name | Value | R/W | Description |
| 15 | | 0 | R | Reserved |
| | | | | This bit is always read as 0. The write value should |
| | | | | always be 0. |
| 14 | PD7MD2 | 0 | R/W | PD7 Mode |
| 13 | PD7MD1 | 0 | R/W | Select the function of the |
| 12 | PD7MD0 | 0* | R/W | PD7/D7/TXD2/SCS/AUDSYNC pin. |
| | | | | 000: PD7 I/O (port) |
| | | | | 001: D7 I/O (BSC) |
| | | | | 011: AUDSYNC output (AUD) |
| | | | | 101: SCS I/O (SSU) |
| | | | | 110: TXD2 output (SCI) |
| | | | | Other than above: Setting prohibited |
| 11 | | 0 | R | Reserved |
| | | | | This bit is always read as 0. The write value should |
| | | | | always be 0. |
| 10 | PD6MD2 | 0 | R/W | PD6 Mode |
| 9 | PD6MD1 | 0 | R/W | Select the function of the PD6/D6/RXD2/AUDCK pin. |
| 8 | PD6MD0 | 0* | R/W | 000: PD6 I/O (port) |
| | | | | 001: D6 I/O (BSC) |
| | | | | 011: AUDCK output (AUD) |
| | | | | 110: RXD2 input (SCI) |
| | | | | Other than above: Setting prohibited |
| 7 | | 0 | R | Reserved |
| | | | | This bit is always read as 0. The write value should |
| | | | | always be 0. |
| 6 | PD5MD2 | 0 | R/W | PD5 Mode |
| 5 | PD5MD1 | 0 | R/W | Select the function of the PD5/D5/SCK1/AUDMD pin. |
| 4 | PD5MD0 | 0* | R/W | 000: PD5 I/O (port) |
| | | | | 001: D5 I/O (BSC) |
| | | | | 011: AUDMD input (AUD) |
| | | | | 110: SCK1 I/O (SCI) |
| | | | | Other than above: Setting prohibited |
| 3 | | 0 | R | Reserved |
| | | | | This bit is always read as 0. The write value should |
| | | | | always be 0. |



RENESAS TECHNICAL UPDATE TN-SH7-A598A/E

[Before]

| | | Initial | | |
|-----|----------|---------|-----|--|
| Bit | Bit Name | Value | R/W | Description |
| 2 | PD4MD2 | 0 | R/W | PD4 Mode |
| 1 | PD4MD1 | 0 | R/W | Select the function of the PD4/D4/TXD1/AUDRST pin. |
| 0 | PD4MD0 | 0* | R/W | 000: PD4 I/O (port) |
| | | | | 001: D4 I/O (BSC) |
| | | | | 011: AUDRST input (AUD) |
| | | | | 110: TXD1 output (SCI) |
| | | | | Other than above: Setting prohibited |

P18-23-24 Port D Control Register L1 (PDCRL1)

| D :/ | Dit News | Initial | D 444 | Description |
|-------------|----------|---------|----------|--|
| | Bit Name | | | Description |
| 15 | | 0 | ĸ | Reserved This hit is always read as 0. The write value should |
| | | | | always be 0 |
| 14 | PD3MD2 | 0 | R/W | PD3 Mode |
| 13 | PD3MD1 | Õ | R/W | Select the function of the PD3/D3/RXD1/AUDATA3 |
| 12 | PD3MD0 | 0* | R/W | pin. Fixed to AUDATA3 output when using the AUD |
| | | | | function of E10A. |
| | | | | 000: PD3 I/O (port) |
| | | | | 001: D3 I/O (BSC) |
| | | | | 011: AUDATA3 output (AUD) |
| | | | | 110: RXD1 input (SCI) |
| 44 | | 0 | D | Other than above: Setting prohibited |
| 11 | | 0 | ĸ | Reserved |
| | | | | always he f |
| 10 | PD2MD2 | 0 | R/W | PD2 Mode |
| 9 | PD2MD1 | 0 0 | R/W | Select the function of the PD2/D2/SCK0/AUDATA2 |
| 8 | PD2MD0 | 0* | R/W | pin. Fixed to AUDATA2 output when using the AUD |
| | | | | function of E10A. |
| | | | | 000: PD2 I/O (port) |
| | | | | 001: D2 I/O (BSC) |
| | | | | 011: AUDATA2 output (AUD) |
| | | | | 110: SCKU I/O (SCI) Other then shows Setting prohibited |
| 7 | | 0 | R | Reserved |
| 1 | | 0 | IX I | This bit is always read as 0. The write value should |
| | | | | always be 0. |
| 6 | PD1MD2 | 0 | R/W | PD1 Mode |
| 5 | PD1MD1 | 0 | R/W | Select the function of the PD1/D1/TXD0/AUDATA1 |
| 4 | PD1MD0 | 0* | R/W | pin. Fixed to AUDATA1 output when using the AUD |
| | | | | function of E10A. |
| | | | | 000: PD1 I/O (port) |
| | | | | |
| | | | | 110: TXD0 output (SCI) |
| | | | | Other than above: Setting prohibited |
| 3 | | 0 | R | Reserved |
| - | | - | | This bit is always read as 0. The write value should |
| | | | | always be 0. |
| 2 | PD0MD2 | 0 | R/W | PD0 Mode |
| 1 | PD0MD1 | 0 | R/W | Select the function of the PD0/D0/RXD0/AUDATA0 |
| 0 | PD0MD0 | 0* | R/W | pin. Fixed to AUDATA0 output when using the AUD |
| | | | | tunction of E10A. |
| | | | | |
| | | | | |
| | | | | 110: RXD0 input (SCI) |
| | | | | Other than above: Setting prohibited |
| | | | | e and a mail abortor obtaing promotion |



| [After] | | | | |
|-------------|----------|---------|------------|--|
| D '/ | | Initial | 5.44 | |
| Bit | Bit Name | Value | <u>R/W</u> | Description |
| 15 | | 0 | R | Reserved |
| | | | | I his bit is always read as 0. The write value should |
| 1.4 | | 0 | D/\// | always be 0. |
| 14 | | 0 | | PD3 MOde Salact the function of the PD3/D3/PVD1/ALIDATA3 |
| 12 | | 0* | R/M | nin |
| 12 | I DOMDO | 0 | | 000: PD3 I/O (port) |
| | | | | 001: D3 I/O (BSC) |
| | | | | 011: AUDATA3 output (AUD) |
| | | | | 110: RXD1 input (SCI) |
| | | | | Other than above: Setting prohibited |
| 11 | | 0 | R | Reserved |
| | | | | This bit is always read as 0. The write value should |
| | | | | always be 0. |
| 10 | PD2MD2 | 0 | R/W | PD2 Mode |
| 9 | PD2MD1 | 0 | R/W | Select the function of the PD2/D2/SCK0/AUDATA2 |
| 8 | PD2MD0 | 0* | R/W | pin. |
| | | | | 000: PD2 I/O (port) |
| | | | | 001: DZ I/O (BSC) |
| | | | | 110 SCK0 I/O (SCI) |
| | | | | Other than above: Setting prohibited |
| 7 | | 0 | R | Reserved |
| - | | - | | This bit is always read as 0. The write value should |
| | | | | always be 0. |
| 6 | PD1MD2 | 0 | R/W | PD1 Mode |
| 5 | PD1MD1 | 0 | R/W | Select the function of the PD1/D1/TXD0/AUDATA1 |
| 4 | PD1MD0 | 0* | R/W | pin. |
| | | | | 000: PD1 I/O (port) |
| | | | | 001: D1 I/O (BSC) |
| | | | | 011: AUDATA1 output (AUD) |
| | | | | 110: TXD0 output (SCI) Other then above: Setting prehibited |
| 2 | | 0 | D | Posonvod |
| 3 | | 0 | n | This hit is always read as 0. The write value should |
| | | | | always be 0 |
| 2 | PD0MD2 | 0 | R/W | PD0 Mode |
| 1 | PD0MD1 | Õ | R/W | Select the function of the PD0/D0/RXD0/AUDATA0 |
| 0 | PD0MD0 | Ō* | R/W | pin. |
| | | | | 000: PD0 I/O (port) |
| | | | | 001: D0 I/O (BSC) |
| | | | | 011: AUDATA0 output (AUD) |
| | | | | 110: RXD0 input (SCI) |
| | | | | Other than above: Setting prohibited |

(2) Advanced User Debugger (AUD)

• P940 (4) Other limitations

[Before]

• When using an on-chip debugger, such as E10A, the AUD cannot be used as the user function regardless of the existence of AUD options.

[After]

Delete

• P943 (3) Other limitations

[Before]

• When using an on-chip debugger, such as E10A, the AUD cannot be used as the user function regardless of the existence of AUD options.

[After]

Delete

