To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-H8*-A378A/E	Rev.	1.00
Title	The error correction for User Boot Mode in Flash Memory		Information Category	Technical Notification		
Applicable Product	H8S/2556 Group H8S/2552 Group H8S/2506 Group	Lot No. All lots	Reference Document	H8S/2556 Group H8S/2552 Group H8S/2506 Group Hardware Manual (REJ09B0099-0500 Rev.5.00)		

We would like to inform you that there are some errors in Section 20 Flash Memory of H8S/2556 Group, H8S/2552 Group, H8S/2506 Group Hardware Manual.

20.1.2 Operating Mode

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[Before Change]

Table 20.1 MD Pin Setting and Operating Mode

Pin	Reset state	On-chip ROM valid mode*1	User program mode*2	User boot mode	Boot mode	Programmer mode
$\overline{RES}$	0	1	1	1	1	1
MD0	0/1	0/1	0/1	1	0/1	0
MD1	0/1	1	1	0	1	0
MD2	0/1	1	1	0	0	0

Notes: 1 On-chip ROM valid mode indicates mode 6 and mode 7. For details, see section 3, MCU Operating Modes.

2 To transit to User program mode, set FLSHE bit in SYSCR2 to 1.

[After change]

Table 20.1 MD Pin Setting and Operating Mode

Pin	Reset state	On-chip ROM valid mode*1	User program mode*2	User boot mode	Boot mode	Programmer mode
$\overline{RES}$	0	1	1	1	1	1
MD0*3	0/1	0/1	0/1	1	0/1	0
MD1	0/1	1	1	0	1	0
MD2	0/1	1	1	0	0	0

Notes: 1 On-chip ROM valid mode indicates mode 6 and mode 7. For details, see section 3, MCU Operating Modes.

2 To transit to User program mode, set FLSHE bit in SYSCR2 to 1.

3 In case of On-chip ROM valid mode, User program mode and Boot mode, when the MD0 pin sets to 0, the mode will be Expanded mode, otherwise, when the pin sets to 1, the mode will be Single chip mode. However, in case of User boot mode, there is no Expanded mode

20.4.3 User Boot Mode

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[Before change]

The area that can be executed in the steps of the user procedure program (on-chip RAM, user MAT, and external space) is shown in section 20.4.4, Procedure Program and Storable Area for Programming Data.

[After change]

The area that can be executed in the steps of the user procedure program (on-chip RAM and user MAT) is shown in section 20.4.4, Procedure Program and Storable Area for Programming Data.

20.4.4 Procedure Program and Storable Area for Programming Data

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[Before change]

Table 20.9 (3) Useable Area for Programming in User Boot Mode

	Storable/Executable Area			Selected MAT		
Item	On-Chip RAM	User Boot MAT	External Space (Expanded Mode)	User MAT	User Boot MAT	Embedded Program Storage Area
Storage Area for Program Data	○	×*1	○	—	—	—
Operation for Selection of On-chip Program to be Downloaded	○	○	○		○	
Operation for Writing H'A5 to FKEY	○	○	○		○	
Execution of Writing SCO=1 to FCCS (Download)	○	×	×			○
Operation for FKEY Clear	○	○	○		○	
Determination of Download Result	○	○	○		○	
Operation for Download Error	○	○	○		○	
Operation for Settings of Initial Parameter	○	○	○		○	

[After change]

Table 20.9 (3) Useable Area for Programming in User Boot Mode

	Storable/Executable Area		Selected MAT		
Item	**On-Chip RAM**	**User Boot MAT**	**User MAT**	**User Boot MAT**	**Embedded Program Storage Area**
Storage Area for Program Data	○	×*1	—	—	—
Operation for Selection of On-chip Program to be Downloaded	○	○		○	
Operation for Writing H'A5 to FKEY	○	○		○	
Execution of Writing SCO=1 to FCCS (Download)	○	×			○
Operation for FKEY Clear	○	○		○	
Determination of Download Result	○	○		○	
Operation for Download Error	○	○		○	
Operation for Settings of Initial Parameter	○	○		○	

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[Before change]

	Storable/Executable Area			Selected MAT		
Item	**On-Chip RAM**	**User Boot MAT**	**External Space (Expanded Mode)**	**User MAT**	**User Boot MAT**	**Embedded Program Storage Area**
Execution of Initialization	○	×	×		○	
Determination of Initialization Result	○	○	○		○	
Operation for Initialization Error	○	○	○		○	
NMI Handling Routine	○	×	○		○	
Operation for Interrupt Inhibit	○	○	○		○	
Switching MATs by FMATS	○	×	×	○		
Operation for Writing H'5A to FKEY	○	×	○	○		
Operation for Settings of Program Parameter	○	×	○	○		
Execution of Programming	○	×	×	○		
Determination of Program Result	○	×	○	○		
Operation for Program Error	○	×*2	○	○		
Operation for FKEY Clear	○	×	○	○		
Switching MATs by FMATS	○	×	×		○	

Notes: 1 Transferring the data to the on-chip RAM enables this area to be used.

2 Switching FMATS by a program in the on-chip RAM enables this area to be used.

[After change]

	Storable/Executable Area		Selected MAT		
Item	On-Chip RAM	User Boot MAT	User MAT	User Boot MAT	Embedded Program Storage Area
Execution of Initialization	○	×		○	
Determination of Initialization Result	○	○		○	
Operation for Initialization Error	○	○		○	
NMI Handling Routine	○	×		○	
Operation for Interrupt Inhibit	○	○		○	
Switching MATs by FMATS	○	×	○		
Operation for Writing H'5A to FKEY	○	×	○		
Operation for Settings of Program Parameter	○	×	○		
Execution of Programming	○	×	○		
Determination of Program Result	○	×	○		
Operation for Program Error	○	×*2	○		
Operation for FKEY Clear	○	×	○		
Switching MATs by FMATS	○	×		○	

Notes: 1 Transferring the data to the on-chip RAM enables this area to be used.

2 Switching FMATS by a program in the on-chip RAM enables this area to be used.

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[Before change]

Table 20.9 (4) Useable Area for Erasure in User Boot Mode

	Storable/Executable Area			Selected MAT		
Item	**On-Chip RAM**	**User Boot MAT**	**External Space (Expanded Mode)**	**User MAT**	**User Boot MAT**	**Embedded Program Storage Area**
Operation for Selection of On-chip Program to be Downloaded	○	○	○		○	
Operation for Writing H'A5 to FKEY	○	○	○		○	
Execution of Writing SCO=1 to FCCS (Download)	○	×	×			○
Operation for FKEY Clear	○	○	○		○	
Determination of Download Result	○	○	○		○	
Operation for Download Error	○	○	○		○	
Operation for Settings of Initial Parameter	○	○	○		○	
Execution of Initialization	○	×	×		○	
Determination of Initialization Result	○	○	○		○	
Operation for Initialization Error	○	○	○		○	
NMI Handling Routine	○	×	○		○	
Operation for Interrupt Inhibit	○	○	○		○	
Switching MATs by FMATS	○	×	×	○		
Operation for Writing H'5A to FKEY	○	×	○	○		

[After change]

Table 20.9 (4) Useable Area for Erasure in User Boot Mode

	Storable/Executable Area		Selected MAT		
Item	On-Chip RAM	User Boot MAT	User MAT	User Boot MAT	Embedded Program Storage Area
Operation for Selection of On-chip Program to be Downloaded	○	○		○	
Operation for Writing H'A5 to FKEY	○	○		○	
Execution of Writing SCO=1 to FCCS (Download)	○	×			○
Operation for FKEY Clear	○	○		○	
Determination of Download Result	○	○		○	
Operation for Download Error	○	○		○	
Operation for Settings of Initial Parameter	○	○		○	
Execution of Initialization	○	×		○	
Determination of Initialization Result	○	○		○	
Operation for Initialization Error	○	○		○	
NMI Handling Routine	○	×		○	
Operation for Interrupt Inhibit	○	○		○	
Switching MATs by FMATS	○	×	○		
Operation for Writing H'5A to FKEY	○	×	○		

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[Before change]

Item	Storable/Executable Area: On-Chip RAM	Storable/Executable Area: User Boot MAT	Storable/Executable Area: External Space (Expanded Mode)	Storable/Executable Area: User MAT	Selected MAT: User Boot MAT	Selected MAT: Embedded Program Storage Area
Operation for Settings of Erasure Parameter	○	×	○	○		
Execution of Erasure	○	×	×	○		
Determination of Erasure Result	○	×	○	○		
Operation for Erasure Error	○	×*	○	○		
Operation for FKEY Clear	○	×	○	○		
Switching MATs by FMATS	○	×	×		○	

Note: Switching FMATS by a program in the on-chip RAM enables this area to be used.

[After change]

	Storable/Executable Area			Selected MAT	
Item	On-Chip RAM	User Boot MAT	User MAT	User Boot MAT	Embedded Program Storage Area
Operation for Settings of Erasure Parameter	○	×	○		
Execution of Erasure	○	×	○		
Determination of Erasure Result	○	×	○		
Operation for Erasure Error	○	×*	○		
Operation for FKEY Clear	○	×	○		
Switching MATs by FMATS	○	×		○	

Note: Switching FMATS by a program in the on-chip RAM enables this area to be used.