Date: Sep. 07, 2011

# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-SH7-A817A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | The error correction and addition about LCD controller (LCDC) | | Information Category | Technical Notification | | |
| Applicable Product | SH7763 Group | Lot No.<br>ALL | Reference Document | SH7763 Hardware Manual (REJ09B0256-0200) | | |

We would like to inform you of the following error correction and addition to the description of the LCD controller (LCDC) in the applicable products.

1. 37.4.6 Power-Supply Control Sequence, Paragraph 2

[Error]

Figures 37.4 to 37.7 are timing charts that show outlines of power-supply control sequences and table 37.6 is a summary of available power-supply control sequence periods.

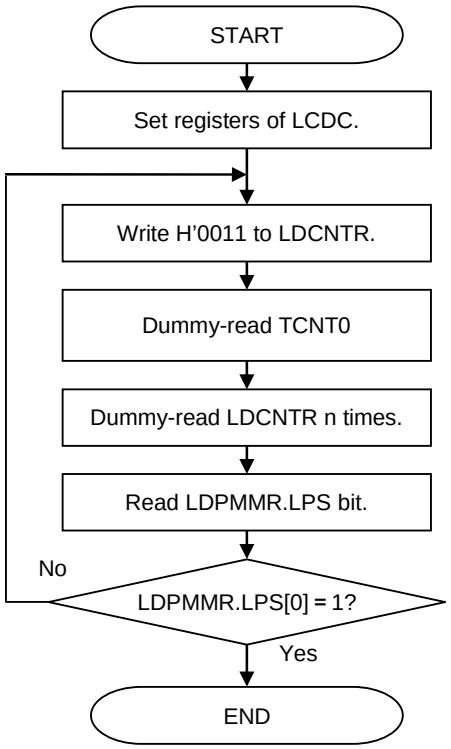
[Correction]

Figure 37.4 gives the flowcharts for power-supply control sequences, figures 37.5 to 37.8 are timing charts that show outlines of power-supply control sequences, and table 37.6 is a summary of available power-supply control sequence periods.

2. Added Figure 37.4

Figure 37.4 to 37.23 are re-numbered to Figure 37.5 to 37.24 respectively, then add new Figure 37.4.

(1) Power-on sequence (when EXTAL is selected as the input clock)

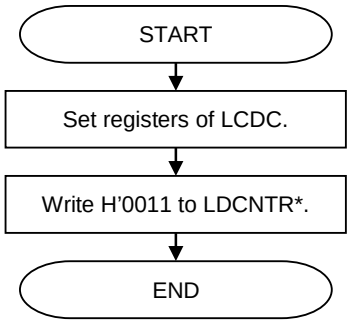



DON2 and DON are set to 1.

Dummy-read TMU/TCNT0 register 1 time.

The number of dummy-read. n= N/2 × P/L +2
N: Setting for divisor (1, 2, 3, 4, 6, 8, 12, 24, 32)
P: Pφfrequency (MHz), L: External LCD input frequency (MHz)
E.g. A case where N: 3, P: Pφ=50MHz, L: LCDCLK=50MHz
3/2 × 50MHz/50MHz + 2 =3.5 =4 (round up to discard the fractional part)

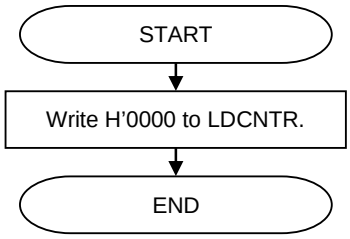
(2) Power-on sequence (when the peripheral clock is selected as the input clock)




DON2 and DON are set to 1.

Note: * To access other registers of the LCDC after writing to LDCNTR, dummy-read TMU/TCNT0 register once beforehand.

(3) Power-off sequence




DON2 and DON are set to 0.

Note: After the power-off sequence, the procedure described in section 37.6.1 Procedure for Halting Access to Display Data Storage VRAM (DDR-SDRAM in Area 3) is required before selecting self-refreshing for the display data storage VRAM (DDR-SDRAM in area 3) or making a transition to standby mode or module standby.

Figure 37.4 Flowchart for Power-Supply Control Sequences

- End of report -