

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A816A/E	Rev.	1.00
Title	The error correction and addition about LCD controller (LCDC)		Information Category	Technical Notification		
Applicable Product	SH7764 Group	Lot No.	Reference Document	SH7764 Group Hardware Manual (REJ09B0360-0200)		
		ALL				

We would like to inform you of the following error correction and addition to the description of the LCD controller (LCDC) in the applicable products.

1. 22.4.5 Power-Supply Control Sequence, Paragraph 2

[Error]

Figures 22.4 to 22.7 are timing charts that show outlines of power-supply control sequences and table 22.5 is a summary of available power-supply control sequence periods.

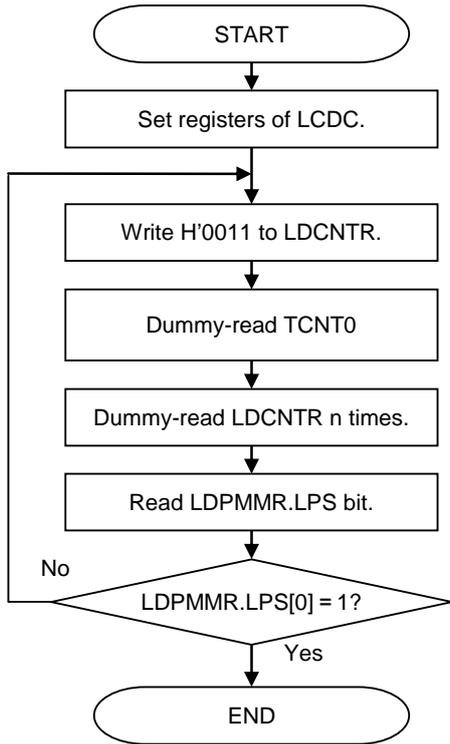
[Correction]

Figure 22.4 gives the flowcharts for power-supply control sequences, figures 22.5 to 22.8 are timing charts that show outlines of power-supply control sequences, and table 22.5 is a summary of available power-supply control sequence periods.

2. Added Figure 22.4

Figure 22.4 to 22.22 are re-numbered to Figure 22.5 to 22.23 respectively, then add new Figure 22.4.

(1) Power-on sequence (when EXTAL is selected as the input clock)



DON2 and DON are set to 1.

Dummy-read TMU/TCNT0 register 1 time.

The number of dummy-read. $n = N/2 \times P/L + 2$

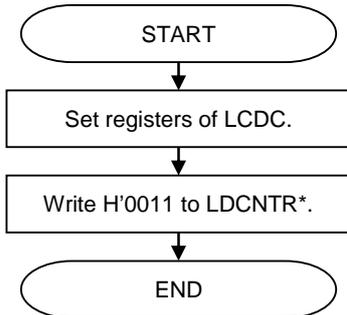
N: Setting for divisor (1, 2, 3, 4, 6, 8, 12, 24, 32)

P: Pφfrequency (MHz), L: External LCD input frequency (MHz)

E.g. A case where N: 3, P: Pφ=50MHz, L: LCDCLK=50MHz

$3/2 \times 50\text{MHz}/50\text{MHz} + 2 = 3.5 = 4$ (round up to discard the fractional part)

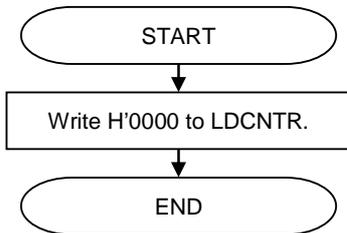
(2) Power-on sequence (when the peripheral clock is selected as the input clock)



DON2 and DON are set to 1.

Note: * To access other registers of the LCDC after writing to LDCNTR, dummy-read TMU/TCNT0 register once beforehand.

(3) Power-off sequence



DON2 and DON are set to 0.

Note: After the power-off sequence, the procedure described in section 22.6.1 Procedure for Halting Access to Display Data Storage VRAM (SDRAM in Area 1 or 2) is required before selecting self-refreshing for the display data storage VRAM (SDRAM in area 1 or 2) or making a transition to standby mode or module standby.

Figure 22.4 Flowchart for Power-Supply Control Sequences

- End of report -