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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A859A/E	Rev.	1.00
Title	Errata to User's Manual Regarding CAN Module		Information Category	Technical Notification		
Applicable Product	SH7450 Group, SH7451 Group SH7455 Group, SH7456 Group	Lot No.	Reference Document	SH7450 Group, SH7451 Group User's Manual: Hardware REV.1.10 SH7455 Group, SH7456 Group User's Manual: Hardware REV.1.10		

This document describes corrections to the chapter "CAN module" in the User's Manuals: Hardware of the above groups.
The corrections are indicated in red in the list below.
Page and section numbers are based on the SH7450 Group. Refer to the table on the last page for the corresponding pages and chapters in other groups.

- Page 26-57

The description in 26.3.20 BLIF (Bus Lock Detect Flag) Bit is corrected as follows:

Before correction

The BLIF bit is set to "1" if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.
After the bit is set to "1", redetection takes place under either of the following conditions:

• After this bit is set to "0" from "1", recessive bits are detected.

• After this bit is set to "0" from "1", the CAN module enters CAN reset mode or CAN halt mode and then enters CAN operation mode again.

Corrections

The BLIF bit is set to "1" if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.
After the bit is set to "1", bus lock can be detected again after either of the following conditions is satisfied:

• After this bit is set to "0" from "1", recessive bits are detected (bus lock is resolved).

• After this bit is set to "0" from "1", the CAN module enters CAN reset mode and then enters CAN operation mode again (internal reset).

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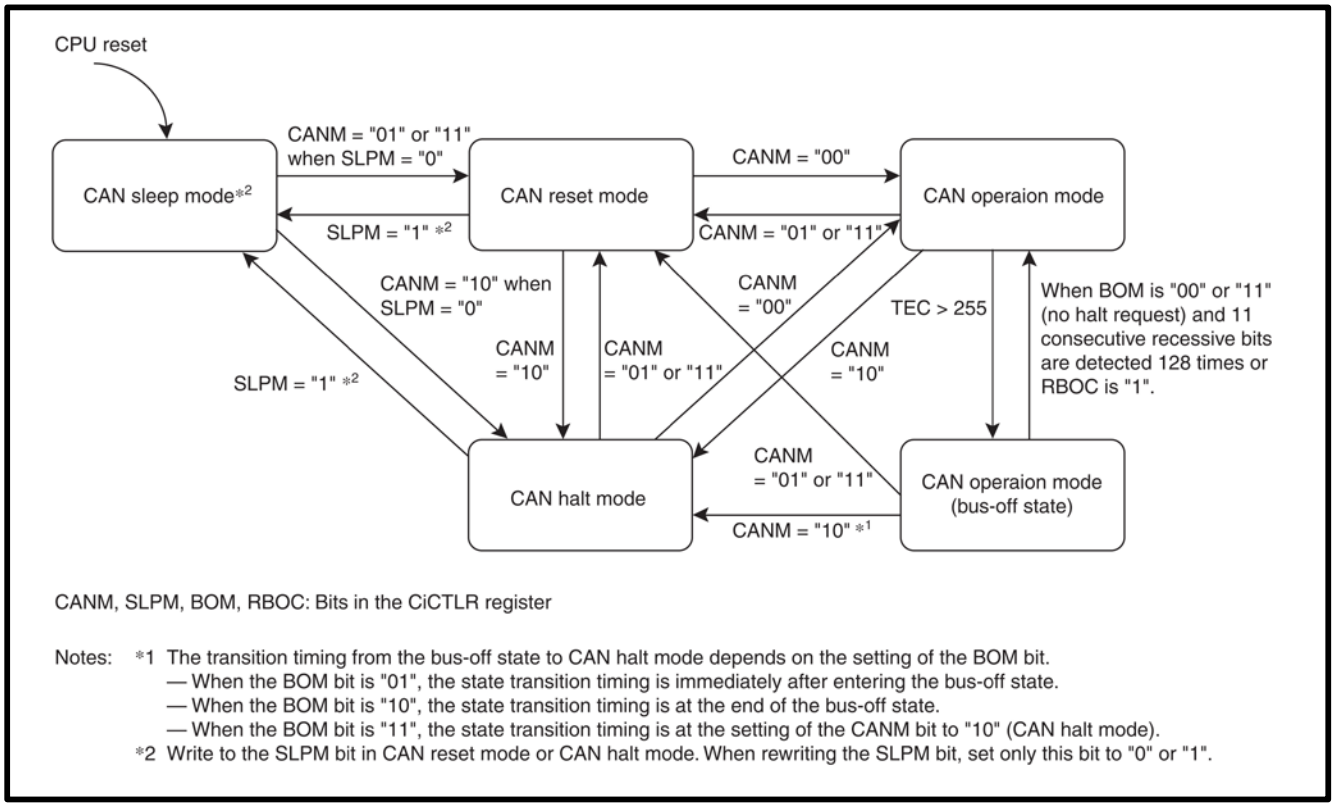
The description in Figure 26.9 Transition between CAN Operating Modes is corrected as follows:

Before correction

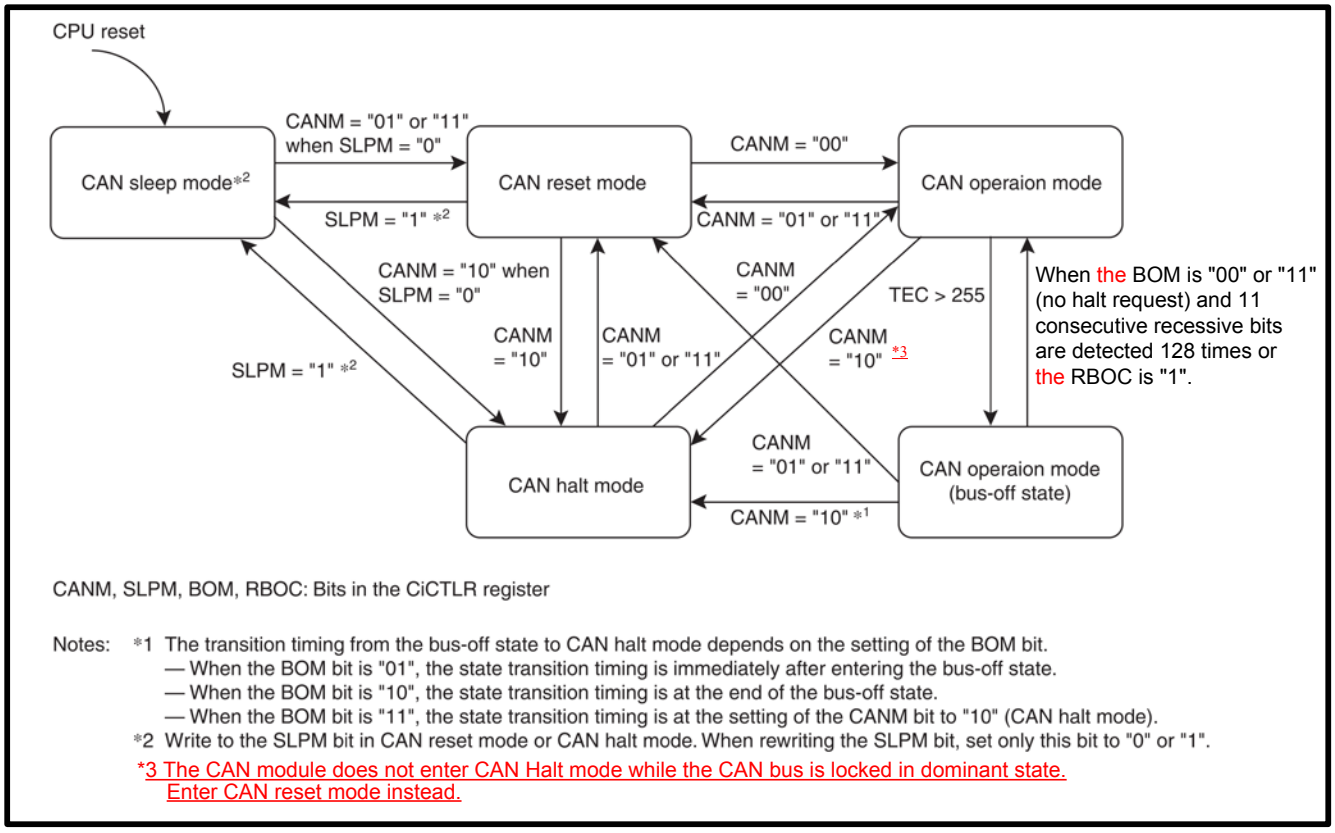


CANM, SLPM, BOM, RBOC: Bits in the CiCTLR register

Notes: *1 The transition timing from the bus-off state to CAN halt mode depends on the setting of the BOM bit.
— When the BOM bit is "01", the state transition timing is immediately after entering the bus-off state.
— When the BOM bit is "10", the state transition timing is at the end of the bus-off state.
— When the BOM bit is "11", the state transition timing is at the setting of the CANM bit to "10" (CAN halt mode).
*2 Write to the SLPM bit in CAN reset mode or CAN halt mode. When rewriting the SLPM bit, set only this bit to "0" or "1".

Figure 26.9 Transition between CAN Operating Modes (i = 0 to 4)

Corrections



CANM, SLPM, BOM, RBOC: Bits in the CiCTLR register

Notes: *1 The transition timing from the bus-off state to CAN halt mode depends on the setting of the BOM bit.
— When the BOM bit is "01", the state transition timing is immediately after entering the bus-off state.
— When the BOM bit is "10", the state transition timing is at the end of the bus-off state.
— When the BOM bit is "11", the state transition timing is at the setting of the CANM bit to "10" (CAN halt mode).
*2 Write to the SLPM bit in CAN reset mode or CAN halt mode. When rewriting the SLPM bit, set only this bit to "0" or "1".
*3 The CAN module does not enter CAN Halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

Figure 26.9 Transition between CAN Operating Modes (i = 0 to 4)

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Table 26.9 CAN Operation in CAN Reset Mode and CAN Halt Mode is corrected as follows:

Before correction

Table 26.9 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-Off
CAN reset mode (forcible transition) CANM = "11"	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM = "01"	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission*1*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception*2*3	CAN module enters CAN halt mode after waiting for the end of message transmission*1*4	[When the BOM bit is "00"] A halt request from a program will be acknowledged only after bus-off recovery. [When the BOM bit is "01"] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "10"] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "11"] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

Legend: BOM bit: Bit in CiCTLR register (i = 0 to 4)

Notes: *1 If several messages are requested to be transmitted, mode transition occurs after the completion of the first transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.

*2 If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF bit in the CiEIFR register.

*3 If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN mode transits to CAN halt mode.

*4 If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN mode transits to the requested CAN mode.

Corrections

Table 26.9 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-Off
CAN reset mode (forcible transition) CANM = "11"	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM = "01"	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission*1*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception*2*3	CAN module enters CAN halt mode after waiting for the end of message transmission*1*2*4	[When the BOM bit is "00"] A halt request from a program will be acknowledged only after bus-off recovery. [When the BOM bit is "01"] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "10"] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is "11"] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

Legend: BOM bit: Bit in CiCTLR register (i = 0 to 4)

Notes: *1 If several messages are requested to be transmitted, mode transition occurs after the completion of the first transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.

*2 If the CAN bus is locked in the dominant state, the program can detect this state by monitoring the BLIF bit in the CiEIFR register. The CAN module does not enter CAN Halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

*3 If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

*4 If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

<Reference Documents>

Applicable Product	Manual and Document Number	Page Number, Figure/Title Number		
		BLIF	Figure 26.9	Table 26.9
SH7450 Group, SH7451 Group	SH7450 Group, SH7451 Group User's Manual: Hardware Rev.1.10 (R01UH0286EJ0110)	Page 26-57 26.3.20	Page 26-72 Figure 26.9	Page 26-74 Table 26.9
SH7455 Group, SH7456 Group	SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10 (R01UH0030EJ0110)	Page 26-56 26.3.20	Page 26-71 Figure 26.9	Page 26-73 Table 26.9