Date: Jul. 14, 2020

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A0230A/E	Rev.	1.00
Title	Errata to User's Manual: Hardware Regarding the I^2C-bus Interface (RIIC)		Information Category	Technical Notification		
Applicable Product	RX110 Group, RX111 Group, RX113 Group, RX23T Group, RX634 Group	Lot No. All	Reference Document	User's Manual: Hardware for applicable products (see the table at the last page)		

This document describes corrections to the "I^2C-bus Interface (RIIC)" chapter in User's Manual: Hardware for the applicable products.
Page and section numbers are based on those of the manual for the RX110 Group. Refer to the table on the last page for the corresponding page and section numbers in the other groups.

• Page 632 of 968

The first paragraph of the description for the NACKE bit in section 24.2.6, I^2C-bus Function Enable Register (ICFER) is corrected as follows.

Before correction

This bit is used to specify whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1.

After correction

This bit is used to specify whether to continue or discontinue the data transfer when NACK is received in transmit mode. Normally, set this bit to 1.

• Page 640 of 968

The second paragraph of the description for the AL flag in section 24.2.10, I^2C-bus Status Register 2 (ICSR2) is corrected as follows.

Before correction

The RIIC can also set the flag to indicate the detection of loss of arbitration during NACK transmission in master mode or during data transmission in slave mode.

After correction

The RIIC can also detect loss of arbitration during NACK transmission in receive mode or during data transmission in slave mode.

- Page 642 of 968

The note for the TDRE flag in section 24.2.10, I^2C-bus Status Register 2 (ICSR2) is corrected as follows.

Before correction

Note: When the NACKF flag is set to 1 while the ICFER.NACKE bit is 1, the RIIC suspends data transmission/ reception. Here, if the TDRE flag is 0 (next transmit data has been written), data is transferred to the ICDRS register and the ICDRT register becomes empty at the rising edge of the ninth clock cycle, but the TDRE flag is not set to 1.

After correction

Note: The NACKF flag becoming 1 while the ICFER.NACKE bit is 1 suspends data transmission and reception by the RIIC. Even if the next data for transmission has already been written to the ICDRT register (the TDRE flag is 0), the data in the ICDRT register is retained but not transferred to the ICDRS register. At this point, the TDRE flag does not become 1.

- Page 673 of 968

The first paragraph of section 24.7.3, Device-ID Address Detection is corrected as follows.

Before correction

The RIIC module has a facility for detecting device-ID addresses conformant with the I^2C-bus specification (Rev. 03). When the RIIC receives 1111 100b as the first byte after a start condition or restart condition was issued with the ICSER.DIDE bit set to 1, the RIIC recognizes the address as a device ID, sets the ICSR1.DID flag to 1 on the rising edge of the eighth SCL clock cycle when the following R/W# bit is 0, and then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, the RIIC sets the corresponding ICSR1.AASy flag (y = 0 to 2) to 1.

After correction

The RIIC module has a function to detect device-ID addresses complying with the I^2C-bus specification. When the RIIC receives 1111 100b as the first seven bits of the first byte following a start condition or a restart condition while the ICSER.DIDE bit is set to 1, the RIIC recognizes the address as a device-ID address, sets the ICSR1.DID flag to 1 on the rising edge of the ninth SCL when the following R/W# bit is 0, and then compares the second and following bytes with its own slave address. If the received address matches the value in the slave address register, the RIIC sets the corresponding ICSR1.AASy flag (y = 0 to 2) to 1.

- Page 674 of 968

Figure 24.28 in section 24.7.3, Device-ID Address Detection is corrected as follows.

Before correction

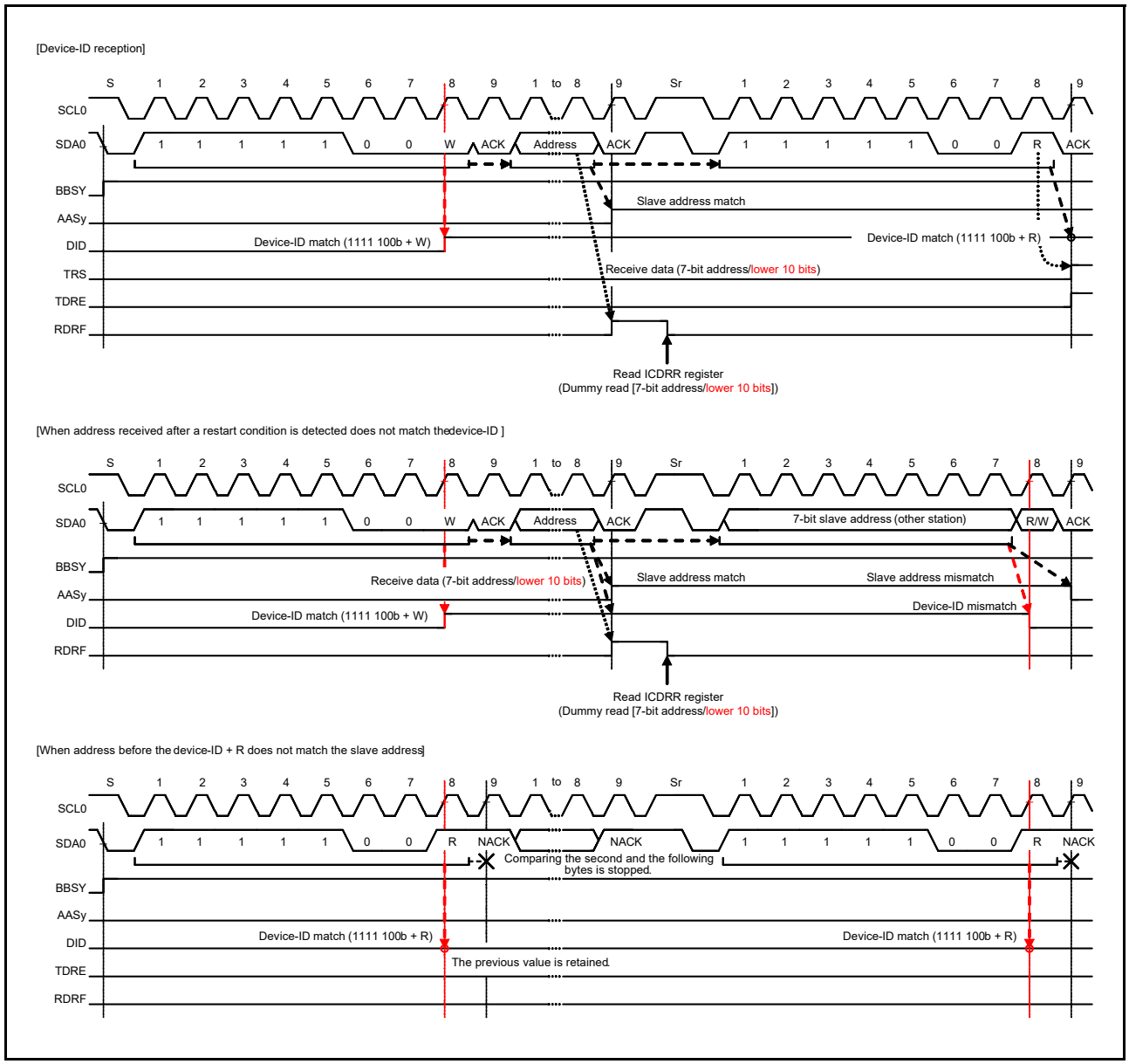

Figure 24.28 AASy/DID Flag Set/Clear Timing during Reception of Device-ID

After correction

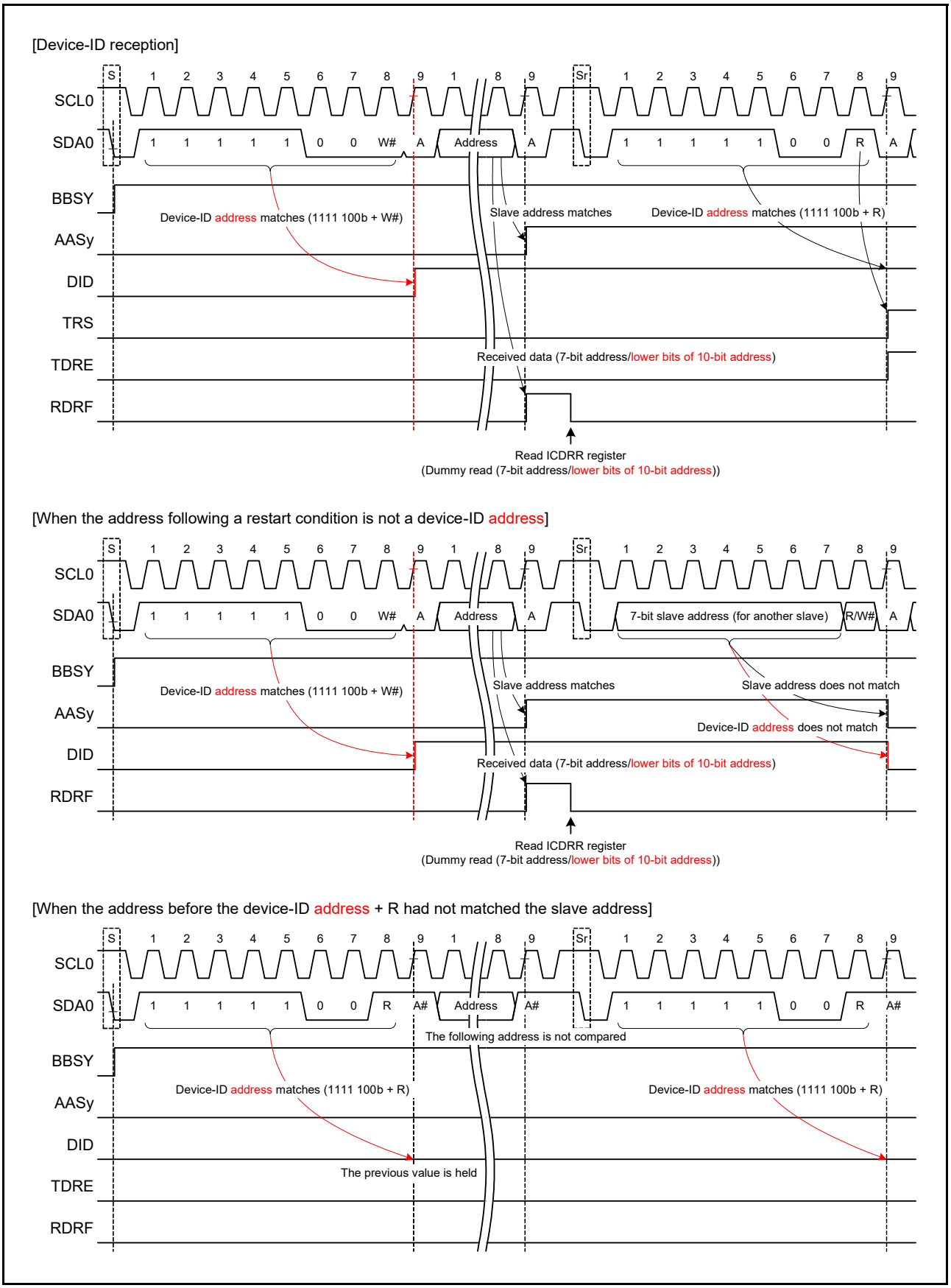

Figure 24.28 Set/Clear Timing of the AASy and DID Flags during Reception of Device-ID Address

- Page 677 of 968

The second paragraph in section 24.8.2, NACK Reception Transfer Suspension Function is corrected as follows.

Before correction

If the transfer operation is suspended by this function (ICSR2.NACKF flag is 1), transmit operation and receive operation are discontinued. To restore transmit/receive operation, be sure to set the NACKF flag to 0. In master transmit mode, after setting the NACKF flag to 0, issue a restart condition, or issue a stop condition and then issue a start condition again.

After correction

If the data transmission is suspended (ICSR2.NACKF flag is 1) by this function, the following data transmission and data reception are not started. To resume data transfer, set the NACKF flag to 0. In master transmit mode, restart data transfer by setting the NACKF flag to 0 after generating a restart condition, or restart data transfer from a start condition after generating a stop condition then setting the NACKF flag to 0.

- Page 677 of 968

Figure 24.31 in section 24.8.2, NACK Reception Transfer Suspension Function is corrected as follows.

Before correction

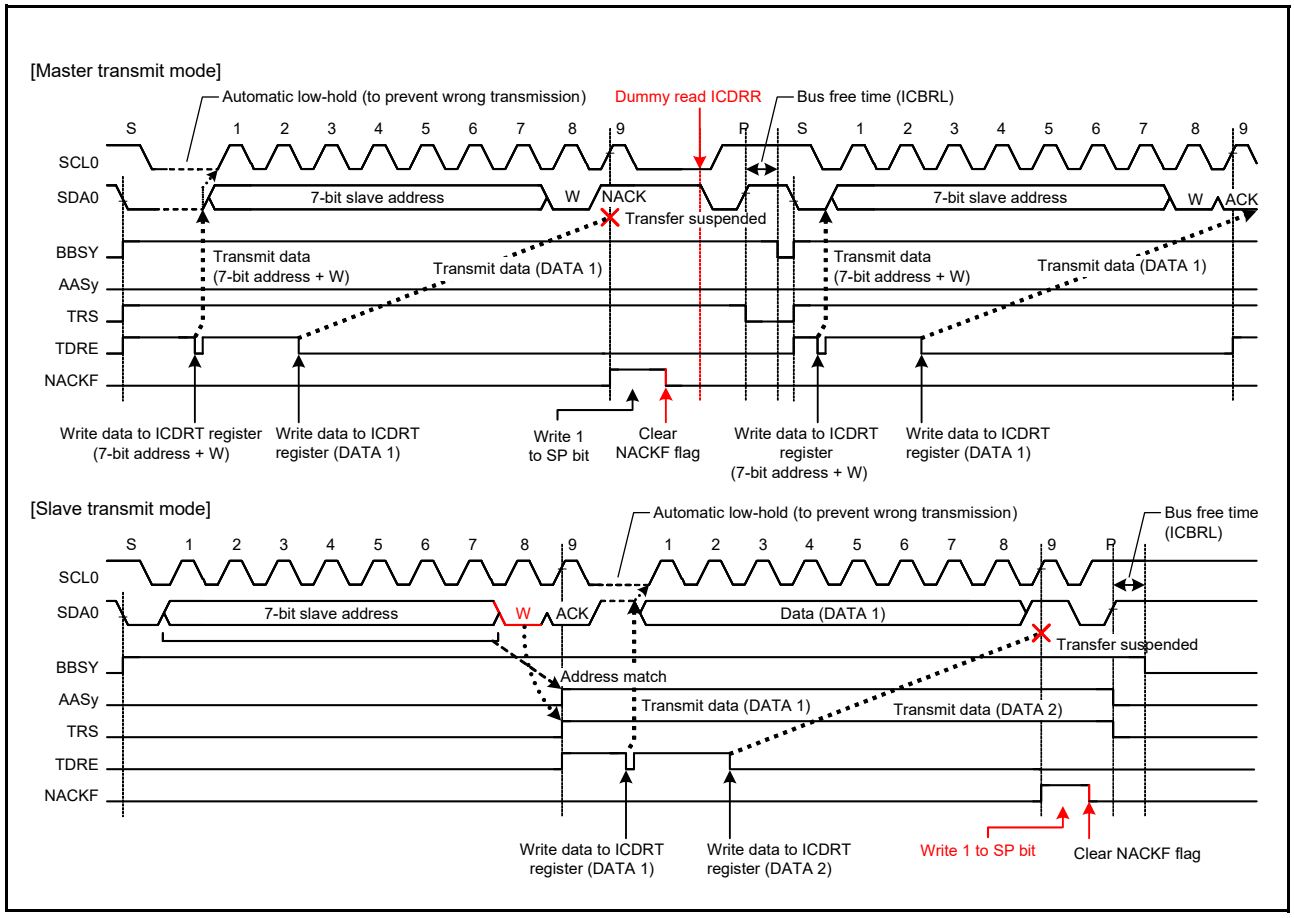

Figure 24.31 Suspension of Data Transfer When NACK is Received (NACKE = 1)

After correction

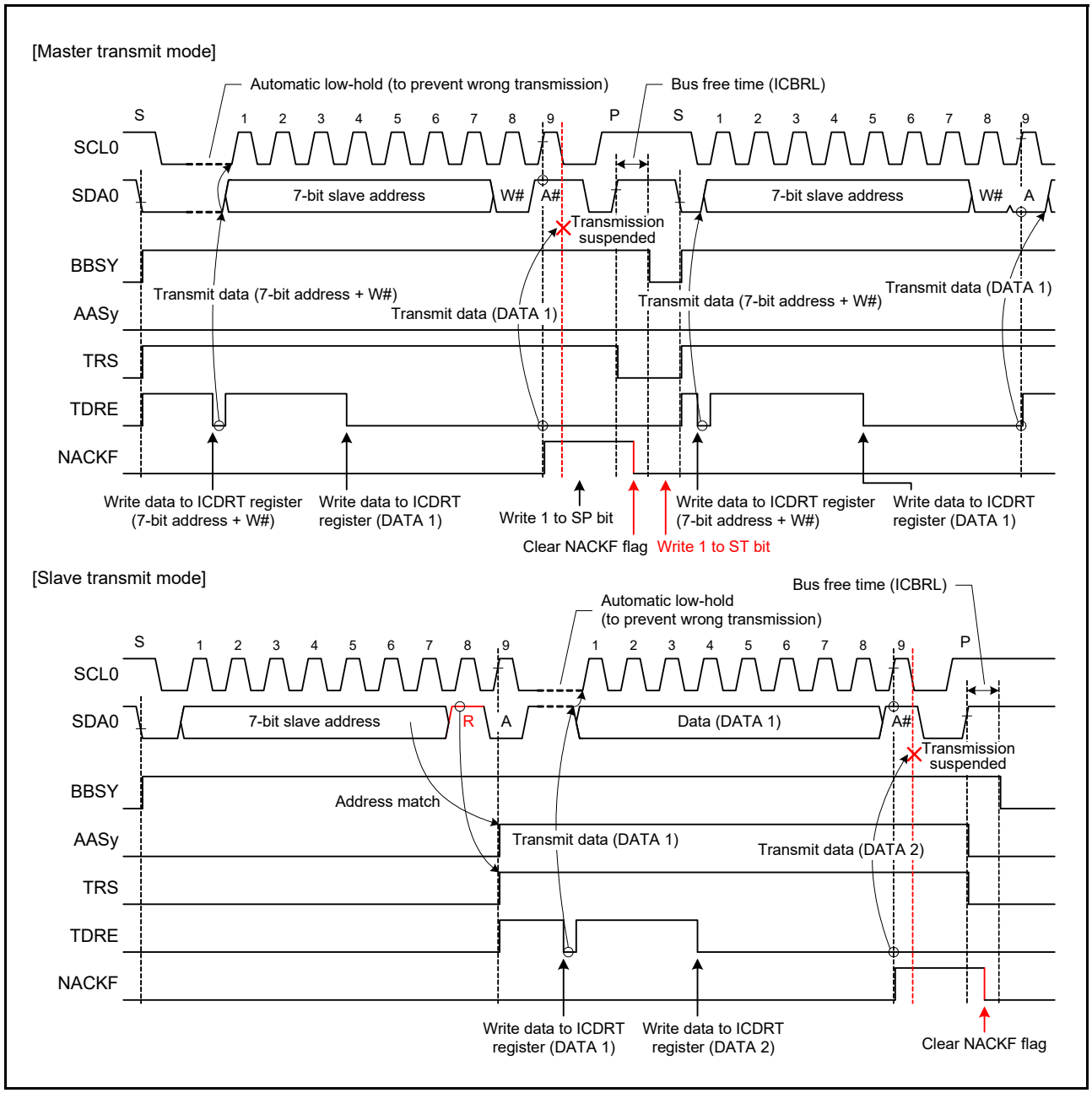

Figure 24.31 Suspension of Data Transmission When NACK is Received (NACKE = 1)

- Page 687 of 968

The third paragraph in section 24.11.2, Extra SCL Clock Cycle Output Function is modified as follows.

Before correction

When the ICCR1.CLO bit is set to 1 in master mode, a single cycle of the SCL clock at the frequency corresponding to the transfer rate settings (settings of the ICMR1.CKS[2:0] bits, and of registers ICBRH and ICBRL) is output as an extra clock cycle. After output of this single cycle of the SCL clock, the CLO bit is automatically set to 0. Therefore, further extra clock cycles can be output consecutively by writing 1 to the CLO bit after confirming the CLO bit to be 0.

After correction

When the ICCR1.CLO bit is set to 1, an additional clock pulse at the frequency set by the ICMR1.CKS[2:0] bits and the ICBRH and ICBRL registers is output from the SCL0 pin. After output of this clock pulse, the CLO bit automatically becomes 0. The SCL0 pin is held low when the ICCR2.BBSY flag is 1 and held high when the BBSY flag is 0. Consecutive additional clock pulses can be output by writing 1 to the CLO bit after confirming the CLO bit to be 0.

- Page 687 of 968

The second sentence in the fifth paragraph of section 24.11.2, Extra SCL Clock Cycle Output Function is deleted as follows.

Before correction

Use this facility with the ICFER.MALE bit (master arbitration-lost detection disabled) set to 0. If the MALE bit is set to 1 (master arbitration-lost detection enabled), arbitration is lost when the value of the ICCR1.SDAO bit does not match the state of the SDA0 line, so take care on this point.

After correction

Use this function with the ICFER.MALE bit set to 0 (master arbitration-lost detection is disabled).

• Page 687 of 968

Figure 24.40 in section 24.11.2, Extra SCL Clock Cycle Output Function is corrected as follows.

Before correction

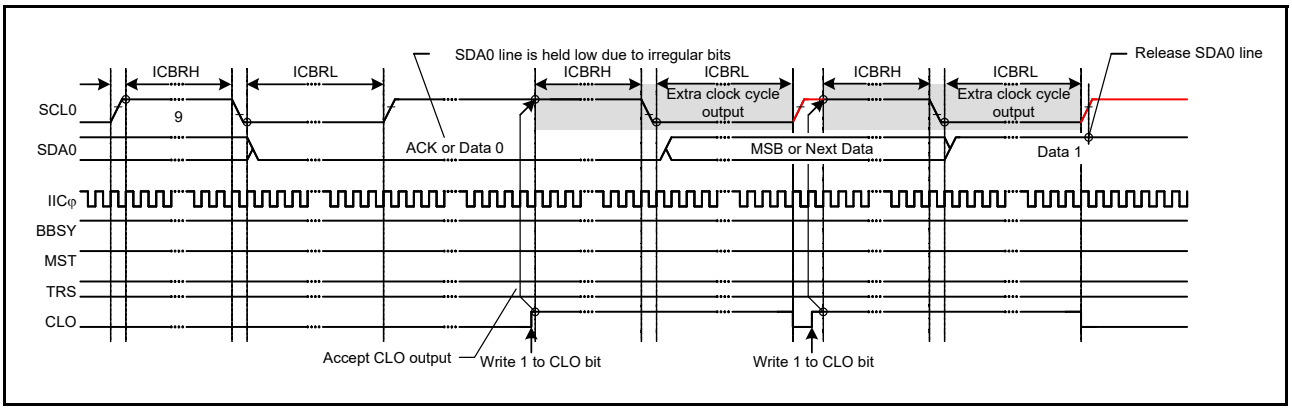

Figure 24.40 Extra SCL Clock Cycle Output Function (CLO Bit)

After correction

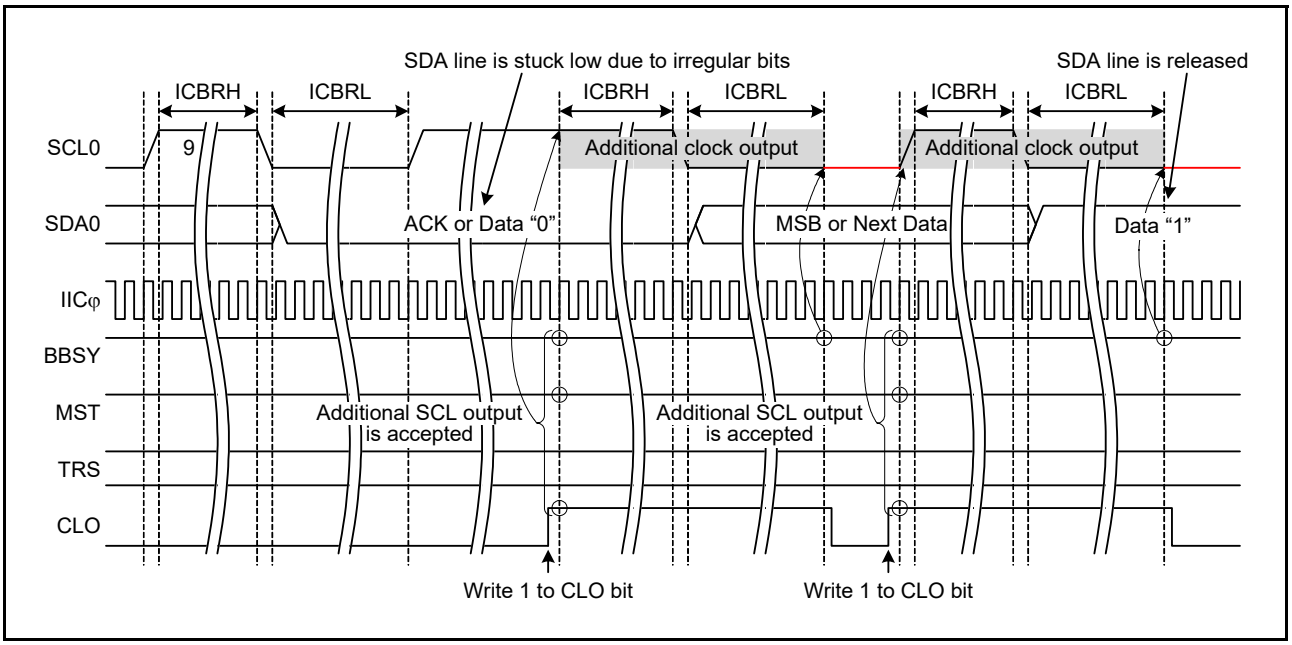

Figure 24.40 Additional SCL Output Function (CLO Bit)

• Page 692 of 968

Table 24.8 in section 24.14, Resets and Register and Function States When Issuing Each Condition is corrected as follows.

Before correction

Table 24.8 Register and Function States When Issuing Each Reset or Condition

		MCU Reset	RIIC Reset (ICE = 0, IICRST = 1)	Internal Reset (ICE = 1, IICRST = 1)	Start Condition/ Restart Condition Detection	Stop Condition Detection
ICCR1	ICE, IICRST	At a reset	Retained	Retained	Retained	Retained
	SCLO, SDAO		At a reset	At a reset		
	Others			Retained		
ICCR2	BBSY	At a reset	At a reset	Retained	Retained	Retained
	ST			At a reset	At a reset	Retained
	Others					At a reset
ICMR1	BC[2:0]	At a reset	At a reset	At a reset	At a reset	Retained
	Others			Retained	Retained	
ICMR2		At a reset	At a reset	Retained	Retained	Retained
ICMR3		At a reset	At a reset	Retained	Retained	Retained
ICFER		At a reset	At a reset	Retained	Retained	Retained
ICSER		At a reset	At a reset	Retained	Retained	Retained
ICIER		At a reset	At a reset	Retained	Retained	Retained
ICSR1		At a reset	At a reset	At a reset	Retained	At a reset
ICSR2	TDRE, TEND	At a reset	At a reset	At a reset	Retained	At a reset
	START				Retained	
	STOP				Retained	Retained
	Others				Retained	Retained
SARL0, SARL1, SARL2, SARU0, SARU1, SARU2		At a reset	At a reset	Retained	Retained	Retained
ICBRH, ICBRL		At a reset	At a reset	Retained	Retained	Retained
ICDRT		At a reset	At a reset	Retained	Retained	Retained
ICDRR		At a reset	At a reset	Retained	Retained	Retained
ICDRS		At a reset	At a reset	At a reset	Retained	Retained
Timeout function		At a reset	At a reset	Operation	Operation	Operation
Bus free time measurement		At a reset	At a reset	Operation	Operation	Operation

After correction

Table 24.8 Reset States of Registers and Functions When a Reset is Applied or a Condition is Detected

		MCU Reset	RIIC Reset (ICE = 0, IICRST = 1)	Internal Reset (ICE = 1, IICRST = 1)	Start Condition/ Restart Condition Detection	Stop Condition Detection
ICCR1	SDAO, SCLO	To be reset	To be reset	To be reset	Retained	Retained
	IICRST, ICE		Retained	Retained		
	Others		To be reset			
ICCR2	ST, RS	To be reset	To be reset	To be reset	To be reset	Retained
	SP					To be reset
	TRS				See note 1	
	MST				See note 1	
	BBSY			Retained	Becomes 1	
ICMR1	BC[2:0]	To be reset	To be reset	To be reset	To be reset	Retained
	Others			Retained	Retained	
ICMR2		To be reset	To be reset	Retained	Retained	Retained
ICMR3	ACKBT	To be reset	To be reset	Retained	Retained	To be reset
	Others					Retained
ICFER		To be reset	To be reset	Retained	Retained	Retained
ICSER		To be reset	To be reset	Retained	Retained	Retained
ICIER		To be reset	To be reset	Retained	Retained	Retained
ICSR1		To be reset	To be reset	To be reset	Retained	To be reset
ICSR2	START	To be reset	To be reset	To be reset	Becomes 1	To be reset
	STOP				Retained	Becomes 1
	TEND					To be reset
	TDRE				See note 1	
	Others				Retained	Retained
SARL0, SARL1, SARL2, SARU0, SARU1, SARU2		To be reset	To be reset	Retained	Retained	Retained
ICBRH, ICBRL		To be reset	To be reset	Retained	Retained	Retained
ICDRT		To be reset	To be reset	Retained	Retained	Retained
ICDRR		To be reset	To be reset	Retained	Retained	Retained
ICDRS		To be reset	To be reset	To be reset	Retained	Retained
Timeout function		To be reset	To be reset	To be reset	Operation	Operation
Bus free time measurement		To be reset	To be reset	Operation	Operation	Operation

Note 1. This bit is not reset. This bit becomes 0 or 1 in accordance with the conditions.

Reference Documents

Applicable Products	Manual Title (Document Number)
RX110 Group	RX110 Group User's Manual: Hardware Rev.1.20 (R01UH0421EJ0120)
RX111 Group	RX111 Group User's Manual: Hardware Rev.1.30 (R01UH0365EJ0130)
RX113 Group	RX113 Group User's Manual: Hardware Rev.1.10 (R01UH0448EJ0110)
RX23T Group	RX23T Group User's Manual: Hardware Rev.1.10 (R01UH0520EJ0110)
RX634 Group	RX634 Group User's Manual: Hardware Rev.1.00 (R01UH0495EJ0100)

Page Number, Section/Figure/Table Number

Item	Page Number, Section/Figure/Table Number				
	RX110 Group	RX111 Group	RX113 Group	RX23T Group	RX634 Group
Descriptions of the ICFER.NACKE bit	Page 632 24.2.6	Page 885 27.2.6	Page 967 30.2.6	Page 756 26.2.6	Page 1142 33.2.6
Descriptions of the ICSR2.AL flag	Page 640 24.2.10	Page 893 27.2.10	Page 975 30.2.10	Page 764 26.2.10	Page 1150 33.2.10
Note for the ICSR2.TDRE flag	Page 642 24.2.10	Page 895 27.2.10	Page 977 30.2.10	Page 766 26.2.10	Page 1152 33.2.10
Description for the device-ID address detection	Page 673 24.7.3	Page 926 27.7.3	Page 1008 30.7.3	Page 795 26.7.3	Page 1182 33.7.3
Figure of the device-ID address detection	Page 674 Figure 24.28	Page 927 Figure 27.28	Page 1009 Figure 30.28	Page 796 Figure 26.28	Page 1183 Figure 33.28
Descriptions for NACK reception transfer suspension	Page 677 24.8.2	Page 930 27.8.2	Page 1012 30.8.2	Page 799 26.8.2	Page 1186 33.8.2
Figure of NACK reception transfer suspension	Page 677 Figure 24.31	Page 930 Figure 27.31	Page 1012 Figure 30.31	Page 799 Figure 26.31	Page 1186 Figure 33.31
The third paragraph of the extra SCL output function	Page 687 24.11.2	Page 940 27.11.2	Page 1022 30.11.2	Page 809 26.11.2	Page 1196 33.11.2
The fifth paragraph of the extra SCL output function	Page 687 24.11.2	Page 940 27.11.2	Page 1022 30.11.2	Page 809 26.11.2	Page 1196 33.11.2
Figure of the extra SCL output function	Page 687 Figure 24.40	Page 940 Figure 27.40	Page 1022 Figure 30.40	Page 809 Figure 26.40	Page 1196 Figure 33.40
Table of the reset states	Page 692 Table 24.8	Page 945 Table 27.8	Page 1027 Table 30.8	Page 814 Table 26.7	Page 1201 Table 33.8