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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A0244A/E	Rev.	1.00
Title	Errata to the Section on Electrical Characteristics in the RX66N Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX66N Group	Lot No. All	Reference Document	RX66N Group User's Manual: Hardware Rev.1.00 (R01UH0825EJ0100)		

This document describes corrections to the section on Electrical Characteristics in the RX66N Group User's Manual: Hardware, Rev.1.00.

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The frequency of ICLK described in Conditions 2 of Table 61.26, Bus Timing is corrected as follows.

Before correction

Table 61.26 Bus Timing

Conditions 1: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF,
High-drive output is selected by the driving ability control register.

Conditions 2: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, 60 MHz < BCLK = SDCLK ≤ 80 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5,
C = 15 pF for the SDCLK pin, C = 30 pF for other pins.
To control the drive capacity when using the SDRAM: set the PFBCR3.SDCLKDRV bit in external bus control register 1 to 1 to select the drive capacity of the SDCLK pin, and set the SDRAM pins other than the SDCLK pin as high-speed-interface driving outputs.

After correction

Table 61.26 Bus Timing

Conditions 1: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Conditions 2: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = 60 to 120 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, 60 MHz < BCLK = SDCLK ≤ 80 MHz,
$T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC,
C = 15 pF for the SDCLK pin, C = 30 pF for other pins.
To control the drive capacity when using the SDRAM: set the PFBCR3.SDCLKDRV bit in external bus control register 1 to 1 to select the drive capacity of the SDCLK pin, and set the SDRAM pins other than the SDCLK pin as high-speed-interface driving outputs.

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The MTIOC1A pin is added to Figure 61.41, MTU Clock Input Timing as follows.

Before correction

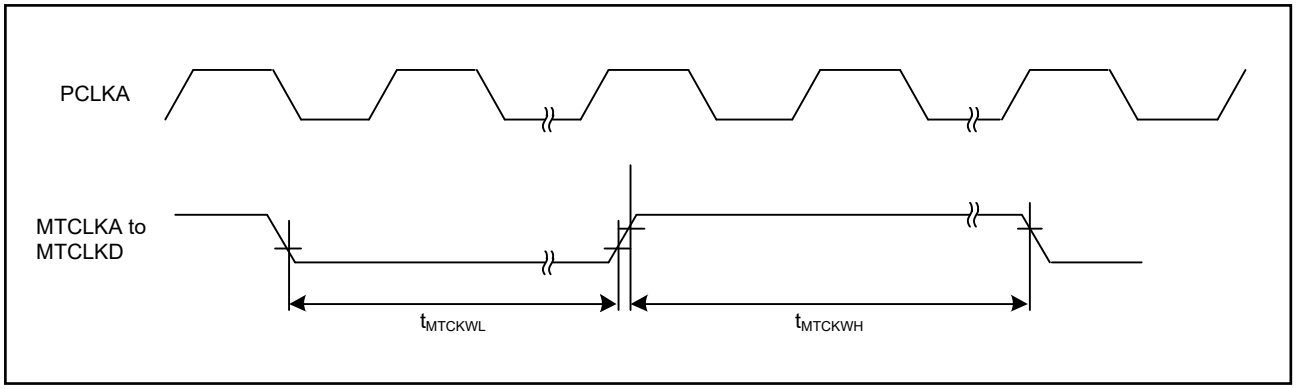

Figure 61.41 MTU Clock Input Timing

After correction

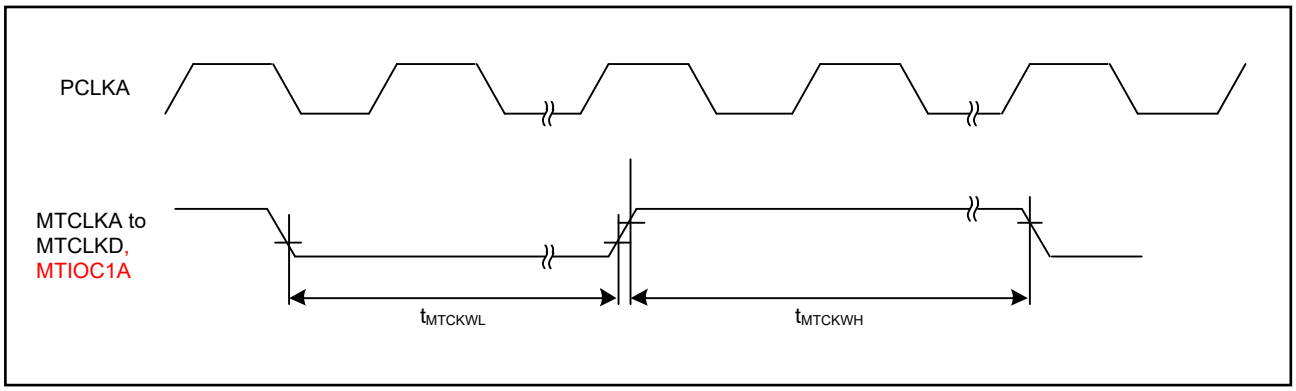

Figure 61.41 MTU Clock Input Timing

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Figure 61.51, Output Disable Time of POEG in Response to the Oscillation Stop Detection is corrected as follows.

Before correction

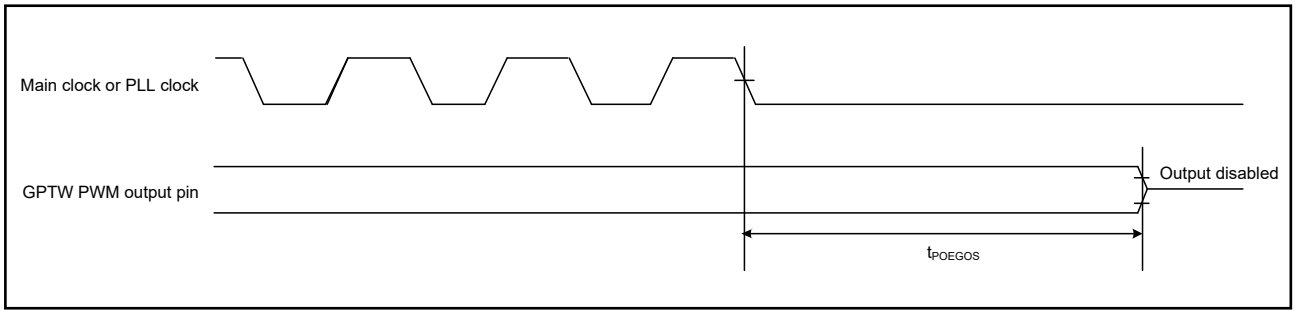

Figure 61.51 Output Disable Time of POEG in Response to the Oscillation Stop Detection

After correction

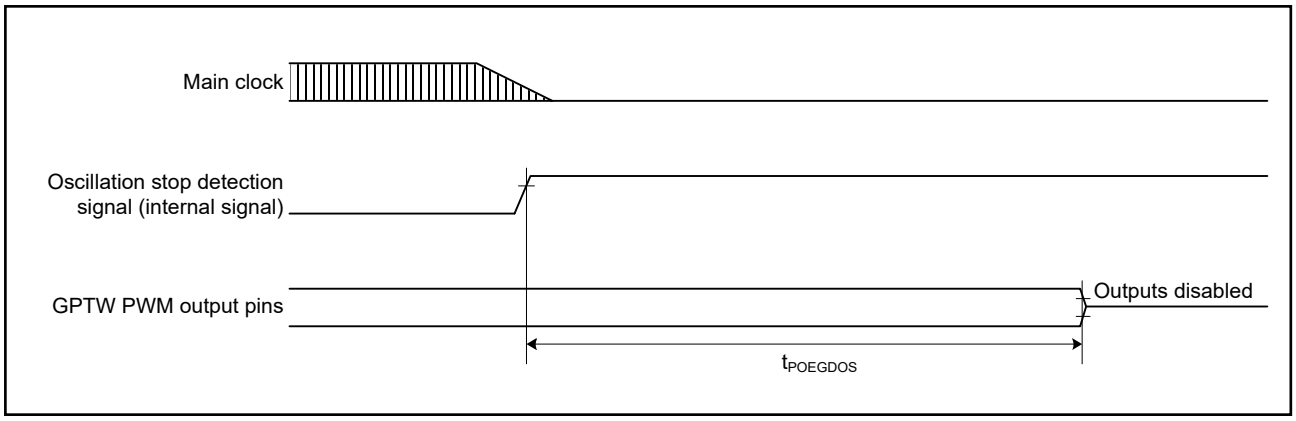

Figure 61.51 Output Disable Time of POEG in Response to the Oscillation Stop Detection

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The following figure is added to illustrate the input and output timing of the simple IIC bus interface.

After correction

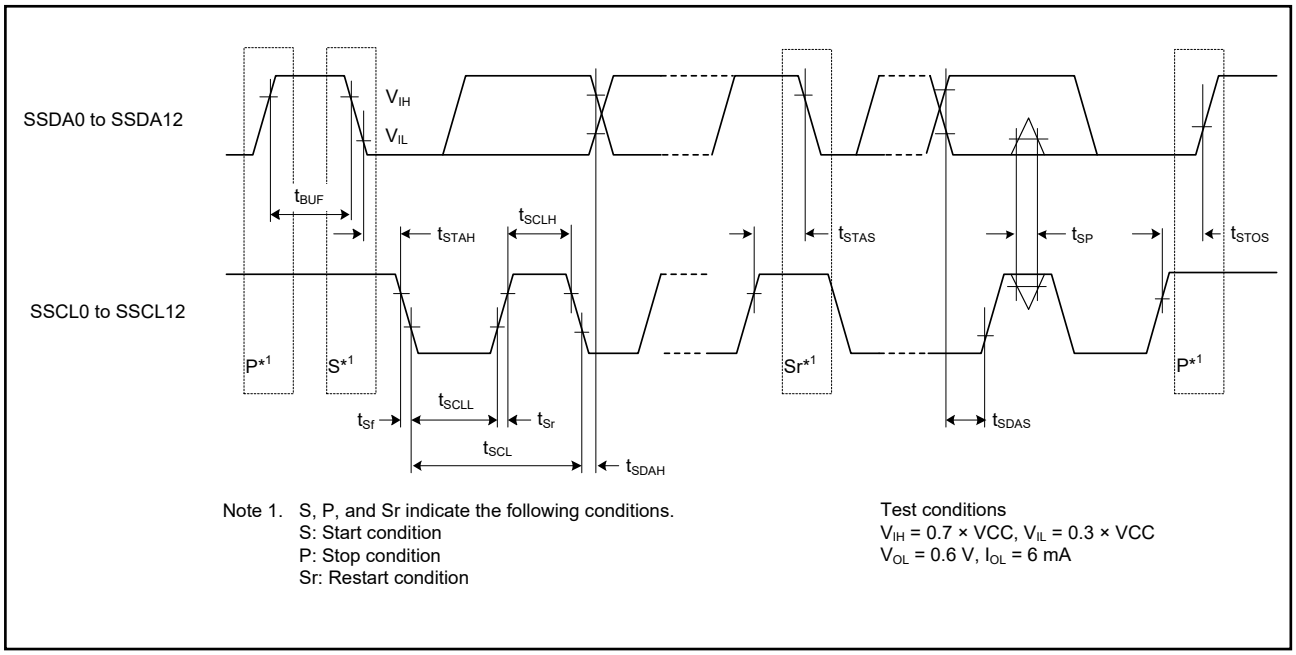

Figure 61.xx Simple IIC Bus Interface Input/Output Timing