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Product Category	MPU/MCU		Document No.	TN-RX*-A0205A/E	Rev.	1.00
Title	Errata to RX66T Group User's Manual: Hardware Rev.1.00		Information Category	Technical Notification		
Applicable Product	RX66T Group	Lot No. All	Reference Document	RX66T Group User's Manual: Hardware Rev.1.00 (R01UH0749EJ0100)		

This document describes corrections to the RX66T Group User's Manual: Hardware, Rev.1.00.

The corrections are indicated in red in the list below.

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The CoreMark score in "Features" section is corrected as follows.

Before correction

■ **32-bit RXv3 CPU core**

- Max. operating frequency: 160 MHz
  Capable of 816 Core Mark in operation at 160 MHz

After correction

■ **32-bit RXv3 CPU core**

- Maximum operating frequency: 160 MHz
  Capable of 928 CoreMark in operation at 160 MHz

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Description in “Driving Ability Switching” column of P36 and P37 is corrected as follows.

Before correction

Table 20.5 Port Functions

Port	Pin	Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant
(Omitted)					
PORT3	P30 to P35	✓	✓	Normal drive/high drive	—
	P36, P37	✓	✓	—	—
(Omitted)					

After correction

Table 20.5 Port Functions

Port	Pin	Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant
(Omitted)					
PORT3	P30 to P35	✓	✓	Normal drive/high drive	—
	P36, P37	✓	✓	Fixed to normal output	—
(Omitted)					

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Bit name and expressions of the description column for the bit description table in 24.2.5, General PWM Timer Start Source Select Register (GTSSR) are modified as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b0	SSGTRGAR	GTETRGA Rising Source Count Start Enable	0: Disables count start at rising of the GTETRGA input 1: Enables count start at rising of the GTETRGA input	R/W
b1	SSGTRGAF	GTETRGA Falling Source Count Start Enable	0: Disables count start at falling of the GTETRGA input 1: Enables count start at falling of the GTETRGA input	R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	SSCARBL	A Pin at Rising and B Pin 0 Source Count Start Enable	0: Disables count start at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0. 1: Enables count start at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0.	R/W
b9	SSCARBH	A Pin at Rising and B Pin 1 Source Count Start Enable	0: Disables count start at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1. 1: Enables count start at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1.	R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

After correction

Bit	Symbol	Bit Name	Description	R/W
b0	SSGTRGAR	GTETRGA Signal Edge Select	b1 b0 0 0: The GTETRGA signal is not used as a trigger to start counting. 0 1: The counter starts at a rising edge of the GTETRGA signal. 1 0: The counter starts at a falling edge of the GTETRGA signal. 1 1: The counter starts at both edges of the GTETRGA signal.	R/W
b1	SSGTRGAF			R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	SSCARBL	GTIOCnA Signal Rising Edge Applying Condition Select	b9 b8 0 0: Rising edge of the GTIOCnA signal is not used as a trigger to start counting. 0 1: The counter starts at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven low. 1 0: The counter starts at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven high. 1 1: The counter starts at a rising edge of the GTIOCnA signal.	R/W
b9	SSCARBH			R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

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Bit name and expressions of the description column for the bit description table in 24.2.6, General PWM Timer Stop Source Select Register (GTPSR) are modified as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b0	PSGTRGAR	GTETRGA Rising Source Count Stop Enable	0: Disables count stop at rising of the GTETRGA input 1: Enables count stop at rising of the GTETRGA input	R/W
b1	PSGTRGAF	GTETRGA Falling Source Count Stop Enable	0: Disables count stop at falling of the GTETRGA input 1: Enables count stop at falling of the GTETRGA input	R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	PSCARBL	A Pin at Rising and B Pin 0 Source Count Stop Enable	0: Disables count stop at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0. 1: Enables count stop at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0.	R/W
b9	PSCARBH	A Pin at Rising and B Pin 1 Source Count Stop Enable	0: Disables count stop at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1. 1: Enables count stop at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1.	R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

After correction

Bit	Symbol	Bit Name	Description	R/W
b0	PSGTRGAR	GTETRGA Signal Edge Select	b1 b0 0 0: The GTETRGA signal is not used as a trigger to stop counting. 0 1: The counter stops at a rising edge of the GTETRGA signal. 1 0: The counter stops at a falling edge of the GTETRGA signal. 1 1: The counter stops at both edges of the GTETRGA signal.	R/W
b1	PSGTRGAF			R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	PSCARBL	GTIOCnA Signal Rising Edge Applying Condition Select	b9 b8 0 0: Rising edge of the GTIOCnA signal is not used as a trigger to stop counting. 0 1: The counter stops at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven low. 1 0: The counter stops at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven high. 1 1: The counter stops at a rising edge of the GTIOCnA signal.	R/W
b9	PSCARBH			R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

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Bit name and expressions of the description column for the bit description table in 24.2.7, General PWM Timer Clear Source Select Register (GTCSR) are modified as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b0	CSGTRGAR	GTETRGA Rising Source Counter Clear Enable	0: Disables counter clear at rising of the GTETRGA input 1: Enables counter clear at rising of the GTETRGA input	R/W
b1	CSGTRGAF	GTETRGA Falling Source Counter Clear Enable	0: Disables counter clear at falling of the GTETRGA input 1: Enables counter clear at falling of the GTETRGA input	R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	CSCARBL	A Pin at Rising and B Pin 0 Source Counter Clear Enable	0: Disables counter clear at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0. 1: Enables counter clear at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0.	R/W
b9	CSCARBH	A Pin at Rising and B Pin 1 Source Counter Clear Enable	0: Disables counter clear at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1. 1: Enables counter clear at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1.	R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

After correction

Bit	Symbol	Bit Name	Description	R/W
b0	CSGTRGAR	GTETRGA Signal Edge Select	b1 b0 0 0: The GTETRGA signal is not used as a trigger to clear the counter. 0 1: The counter is cleared at a rising edge of the GTETRGA signal. 1 0: The counter is cleared at a falling edge of the GTETRGA signal. 1 1: The counter is cleared at both edges of the GTETRGA signal.	R/W
b1	CSGTRGAF			R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	CSCARBL	GTIOCnA Signal Rising Edge Applying Condition Select	b9 b8 0 0: Rising edge of the GTIOCnA signal is not used as a trigger to clear the counter. 0 1: The counter is cleared at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven low. 1 0: The counter is cleared at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven high. 1 1: The counter is cleared at a rising edge of the GTIOCnA signal.	R/W
b9	CSCARBH			R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

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Bit name and expressions of the description column for the bit description table in 24.2.8, General PWM Timer Count-Up Source Select Register (GTUPSR) are modified as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b0	USGTRGAR	GTETRGA Rising Source Count-Up Enable	0: Disables count-up at rising of the GTETRGA input 1: Enables count-up at rising of the GTETRGA input	R/W
b1	USGTRGAF	GTETRGA Falling Source Count-Up Enable	0: Disables count-up at falling of the GTETRGA input 1: Enables count-up at falling of the GTETRGA input	R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	USCARBL	A Pin at Rising and B Pin 0 Source Count-Up Enable	0: Disables count-up at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0. 1: Enables count-up at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0.	R/W
b9	USCARBH	A Pin at Rising and B Pin 1 Source Count-Up Enable	0: Disables count-up at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1. 1: Enables count-up at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1.	R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

After correction

Bit	Symbol	Bit Name	Description	R/W
b0	USGTRGAR	GTETRGA Signal Edge Select	b1 b0 0 0: The GTETRGA signal is not used as a trigger to increment the counter. 0 1: The counter is incremented at a rising edge of the GTETRGA signal. 1 0: The counter is incremented at a falling edge of the GTETRGA signal. 1 1: The counter is incremented at both edges of the GTETRGA signal.	R/W
b1	USGTRGAF			R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	USCARBL	GTIOCnA Signal Rising Edge Applying Condition Select	b9 b8 0 0: Rising edge of the GTIOCnA signal is not used as a trigger to increment the counter. 0 1: The counter is incremented at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven low. 1 0: The counter is incremented at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven high. 1 1: The counter is incremented at a rising edge of the GTIOCnA signal.	R/W
b9	USCARBH			R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

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Bit name and expressions of the description column for the bit description table in 24.2.9, General PWM Timer Count-Down Source Select Register (GTDNSR) are modified as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b0	DSGTRGAR	GTETRGA Rising Source Count-Down Enable	0: Disables count-down at rising of the GTETRGA input 1: Enables count-down at rising of the GTETRGA input	R/W
b1	DSGTRGAF	GTETRGA Falling Source Count-Down Enable	0: Disables count-down at falling of the GTETRGA input 1: Enables count-down at falling of the GTETRGA input	R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	DSCARBL	A Pin at Rising and B Pin 0 Source Count-Down Enable	0: Disables count-down at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0. 1: Enables count-down at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0.	R/W
b9	DSCARBH	A Pin at Rising and B Pin 1 Source Count-Down Enable	0: Disables count-down at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1. 1: Enables count-down at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1.	R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

After correction

Bit	Symbol	Bit Name	Description	R/W
b0	DSGTRGAR	GTETRGA Signal Edge Select	b1 b0 0 0: The GTETRGA signal is not used as a trigger to decrement the counter. 0 1: The counter is decremented at a rising edge of the GTETRGA signal. 1 0: The counter is decremented at a falling edge of the GTETRGA signal. 1 1: The counter is decremented at both edges of the GTETRGA signal.	R/W
b1	DSGTRGAF			R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	DSCARBL	GTIOCnA Signal Rising Edge Applying Condition Select	b9 b8 0 0: Rising edge of the GTIOCnA signal is not used as a trigger to decrement the counter. 0 1: The counter is decremented at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven low. 1 0: The counter is decremented at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven high. 1 1: The counter is decremented at a rising edge of the GTIOCnA signal.	R/W
b9	DSCARBH			R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

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Bit name and expressions of the description column for the bit description table in 24.2.10, General PWM Timer Input Capture Source Select Register A (GTICASR) are modified as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b0	ASGTRGAR	GTETRGA Rising Source GTCCRA Input Capture Enable	0: Disables GTCCRA input capture at rising of the GTETRGA input 1: Enables GTCCRA input capture at rising of the GTETRGA input	R/W
b1	ASGTRGAF	GTETRGA Falling Source GTCCRA Input Capture Enable	0: Disables GTCCRA input capture at falling of the GTETRGA input 1: Enables GTCCRA input capture at falling of the GTETRGA input	R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	ASCARBL	A Pin at Rising and B Pin 0 Source GTCCRA Input Capture Enable	0: Disables GTCCRA input capture at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0. 1: Enables GTCCRA input capture at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0.	R/W
b9	ASCARBH	A Pin at Rising and B Pin 1 Source GTCCRA Input Capture Enable	0: Disables GTCCRA input capture at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1. 1: Enables GTCCRA input capture at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1.	R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

After correction

Bit	Symbol	Bit Name	Description	R/W
b0	ASGTRGAR	GTETRGA Signal Edge Select	b1 b0 0 0: The GTETRGA signal is not used as a trigger to capture the counter value in the GTCCRA register. 0 1: The counter value is captured in the GTCCRA register at a rising edge of the GTETRGA signal. 1 0: The counter value is captured in the GTCCRA register at a falling edge of the GTETRGA signal. 1 1: The counter value is captured in the GTCCRA register at both edges of the GTETRGA signal.	R/W
b1	ASGTRGAF			R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	ASCARBL	GTIOCnA Signal Rising Edge Applying Condition Select	b9 b8 0 0: Rising edge of the GTIOCnA signal is not used as a trigger to capture the counter value in the GTCCRA register. 0 1: The counter value is captured in the GTCCRA register at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven low. 1 0: The counter value is captured in the GTCCRA register at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven high. 1 1: The counter value is captured in the GTCCRA register at a rising edge of the GTIOCnA signal.	R/W
b9	ASCARBH			R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

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Bit name and expressions of the description column for the bit description table in 24.2.11, General PWM Timer Input Capture Source Select Register B (GTICBSR) are modified as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b0	BSGTRGAR	GTETRGA Rising Source GTCCRB Input Capture Enable	0: Disables GTCCRB input capture at rising of the GTETRGA input 1: Enables GTCCRB input capture at rising of the GTETRGA input	R/W
b1	BSGTRGAF	GTETRGA Falling Source GTCCRB Input Capture Enable	0: Disables GTCCRB input capture at falling of the GTETRGA input 1: Enables GTCCRB input capture at falling of the GTETRGA input	R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	BSCARBL	A Pin at Rising and B Pin 0 Source GTCCRB Input Capture Enable	0: Disables GTCCRB input capture at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0. 1: Enables GTCCRB input capture at rising of the GTIOCnA pin input while the GTIOCnB pin input is 0.	R/W
b9	BSCARBH	A Pin at Rising and B Pin 1 Source GTCCRB Input Capture Enable	0: Disables GTCCRB input capture at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1. 1: Enables GTCCRB input capture at rising of the GTIOCnA pin input while the GTIOCnB pin input is 1.	R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

After correction

Bit	Symbol	Bit Name	Description	R/W
b0	BSGTRGAR	GTETRGA Signal Edge Select	b1 b0 0 0: The GTETRGA signal is not used as a trigger to capture the counter value in the GTCCRB register. 0 1: The counter value is captured in the GTCCRB register at a rising edge of the GTETRGA signal. 1 0: The counter value is captured in the GTCCRB register at a falling edge of the GTETRGA signal. 1 1: The counter value is captured in the GTCCRB register at both edges of the GTETRGA signal.	R/W
b1	BSGTRGAF			R/W
(Omitted: Descriptions for b7 and b6, b5 and b4, and b3 and b2 are similar to those for b1 and b0)				
b8	BSCARBL	GTIOCnA Signal Rising Edge Applying Condition Select	b9 b8 0 0: Rising edge of the GTIOCnA signal is not used as a trigger to capture the counter value in the GTCCRB register. 0 1: The counter value is captured in the GTCCRB register at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven low. 1 0: The counter value is captured in the GTCCRB register at a rising edge of the GTIOCnA signal while the GTIOCnB pin is driven high. 1 1: The counter value is captured in the GTCCRB register at a rising edge of the GTIOCnA signal.	R/W
b9	BSCARBH			R/W
(Omitted: Descriptions for b15 and b14, b13 and b12, and b11 and b10 are similar to those for b9 and b8)				
(Omitted: b31 to b16 are not modified)				

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The first paragraph of the descriptions for the ANSB0n bit in 38.2.6 (1) S12AD.ADANSB0 is modified as follows.

Before correction

ANSB0n Bit (A/D Conversion Channel Select) (n = 00 to 07)

The ANSB0n bit selects analog input channels for A/D conversion from among AN000 to AN007 in group B when group scan mode is selected. The S12AD.ADANSB0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD.ADANSA0 and ADANSA1 registers and the S12AD.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

After correction

ANSB0n Bit (A/D Conversion Channel Select) (n = 00 to 07)

The ANSB0n bit selects analog input channels for A/D conversion from among AN000 to AN007 in group B when group scan mode is selected. The S12AD.ADANSB0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the S12AD.ADANSA0 register), the channels specified in group C (the S12AD.ADANSC0 register), and the channels corresponding to group A, selected with the S12AD.ADCSR.DBLANS[4:0] bits in double trigger mode should be excluded as the channels to be selected and the number of channels to be set.

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The first paragraph of the descriptions for the ANSB0n bit in 38.2.6 (2) S12AD1.ADANSB0 is modified as follows.

Before correction

ANSB0n Bit (A/D Conversion Channel Select) (n = 00 to 07)

The ANSB0n bit selects analog input channels for A/D conversion from among AN100 to AN107 in group B when group scan mode is selected. The S12AD1.ADANSB0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD1.ADANSA0 and ADANSA1 registers and the S12AD1.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

After correction

ANSB0n Bit (A/D Conversion Channel Select) (n = 00 to 07)

The ANSB0n bit selects analog input channels for A/D conversion from among AN100 to AN107 in group B when group scan mode is selected. The S12AD1.ADANSB0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the S12AD1.ADANSA0 register), the channels specified in group C (the S12AD1.ADANSC0 register), and the channels corresponding to group A, selected with the S12AD1.ADCSR.DBLANS[4:0] bits in double trigger mode should be excluded as the channels to be selected and the number of channels to be set.

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The first paragraph of the descriptions for the ANSB0n bit in 38.2.6 (3) S12AD2.ADANSB0 is modified as follows.

Before correction

ANSB0n Bit (A/D Conversion Channel Select) (n = 00 to 11)

The ANSB0n bit selects analog input channels for A/D conversion from among AN200 to AN211 in group B when group scan mode is selected. The S12AD2.ADANSB0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD2.ADANSA0 and ADANSA1 registers and the S12AD2.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

After correction

ANSB0n Bit (A/D Conversion Channel Select) (n = 00 to 11)

The ANSB0n bit selects analog input channels for A/D conversion from among AN200 to AN211 in group B when group scan mode is selected. The S12AD2.ADANSB0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the S12AD2.ADANSA0 and S12AD2.ADANSA1 registers), the channels specified in group C (the S12AD2.ADANSC0 and S12AD2.ADANSC1 registers), and the channels corresponding to group A, selected with the S12AD2.ADCSR.DBLANS[4:0] bits in double trigger mode should be excluded as the channels to be selected and the number of channels to be set.

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The first paragraph of the descriptions for the ANSB1n bit in section 38.2.7, A/D Channel Select Register B1 (ADANSB1) is modified as follows.

Before correction

ANSB1n Bit (A/D Conversion Channel Select) (n = 00, 01)

The ANSB1n bit selects analog input channels for A/D conversion from among AN216 to AN217 in group B when group scan mode is selected. The S12AD2.ADANSB1 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD2.ADANSA0 and ADANSA1 registers and the S12AD2.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

After correction

ANSB1n Bit (A/D Conversion Channel Select) (n = 00, 01)

The ANSB1n bit selects analog input channels for A/D conversion from among AN216 to AN217 in group B when group scan mode is selected. The S12AD2.ADANSB1 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the S12AD2.ADANSA0 and S12AD2.ADANSA1 registers), the channels specified in group C (the S12AD2.ADANSC0 and S12AD2.ADANSC1 registers), and the channels corresponding to group A, selected with the S12AD2.ADCSR.DBLANS[4:0] bits in double trigger mode should be excluded as the channels to be selected and the number of channels to be set.

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The first paragraph of the descriptions for the ANSC0n bit in 38.2.8 (1) S12AD.ADANSC0 is modified as follows.

Before correction

ANSC0n Bit (A/D Conversion Channel Select) (n = 00 to 07)

The ANSC0n bit selects analog input channels for A/D conversion from among AN000 to AN007 in group C when group scan mode is selected. The S12AD.ADANSC0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD.ADANSA0 and ADANSA1 registers and the S12AD.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

After correction

ANSC0n Bit (A/D Conversion Channel Select) (n = 00 to 07)

The ANSC0n bit selects analog input channels for A/D conversion from among AN000 to AN007 in group C when group scan mode is selected. The S12AD.ADANSC0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the S12AD.ADANSA0 register), the channels specified in group B (the S12AD.ADANSB0 register), and the channels corresponding to group A, selected with the S12AD.ADCSR.DBLANS[4:0] bits in double trigger mode should be excluded as the channels to be selected and the number of channels to be set.

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The first paragraph of the descriptions for the ANSC0n bit in 38.2.8 (2) S12AD1.ADANSC0 is modified as follows.

Before correction

ANSC0n Bit (A/D Conversion Channel Select) (n = 00 to 07)

The ANSC0n bit selects analog input channels for A/D conversion from among AN100 to AN107 in group C when group scan mode is selected. The S12AD1.ADANSC0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD1.ADANSA0 and ADANSA1 registers and the S12AD1.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

After correction

ANSC0n Bit (A/D Conversion Channel Select) (n = 00 to 07)

The ANSC0n bit selects analog input channels for A/D conversion from among AN100 to AN107 in group C when group scan mode is selected. The S12AD1.ADANSC0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the S12AD1.ADANSA0 register), the channels specified in group B (the S12AD1.ADANSB0 register), and the channels corresponding to group A, selected with the S12AD1.ADCSR.DBLANS[4:0] bits in double trigger mode should be excluded as the channels to be selected and the number of channels to be set.

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The first paragraph of the descriptions for the ANSC0n bit in 38.2.8 (3) S12AD2.ADANSC0 is modified as follows.

Before correction

ANSC0n Bit (A/D Conversion Channel Select) (n = 00 to 11)

The ANSC0n bit selects analog input channels for A/D conversion from among AN200 to AN211 in group C when group scan mode is selected. The S12AD2.ADANSC0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected by the S12AD2.ADANSA0 and ADANSA1 registers, the S12AD2.ADANSB0 and ADANSB1 registers, or the S12AD2.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded from the channels to be selected and the number of channels to be set.

After correction

ANSC0n Bit (A/D Conversion Channel Select) (n = 00 to 11)

The ANSC0n bit selects analog input channels for A/D conversion from among AN200 to AN211 in group C when group scan mode is selected. The S12AD2.ADANSC0 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the S12AD2.ADANSA0 and S12AD2.ADANSA1 registers), the channels specified in group B (the S12AD2.ADANSB0 and S12AD2.ADANSB1 registers), and the channels corresponding to group A, selected with the S12AD2.ADCSR.DBLANS[4:0] bits in double trigger mode should be excluded as the channels to be selected and the number of channels to be set.

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The first paragraph of the descriptions for the ANSC1n bit in section 38.2.9, A/D Channel Select Register C1 (ADANSC1) is modified as follows.

Before correction

ANSC1n Bit (A/D Conversion Channel Select) (n = 00, 01)

The ANSC1n bit selects analog input channels for A/D conversion from among AN216 to AN217 in group C when group scan mode is selected. The S12AD2.ADANSC1 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the S12AD2.ADANSA0 and ADANSA1 registers, the S12AD2.ADANSB0 and ADANSB1 registers, or the S12AD2.ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

After correction

ANSC1n Bit (A/D Conversion Channel Select) (n = 00, 01)

The ANSC1n bit selects analog input channels for A/D conversion from among AN216 to AN217 in group C when group scan mode is selected. The S12AD2.ADANSC1 register is used for group scan mode only; not used for any other modes. The channels specified in group A (the S12AD2.ADANSA0 and S12AD2.ADANSA1 registers), the channels specified in group B (the S12AD2.ADANSB0 and S12AD2.ADANSB1 registers), and the channels corresponding to group A, selected with the S12AD2.ADCSR.DBLANS[4:0] bits in double trigger mode should be excluded as the channels to be selected and the number of channels to be set.

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Table 45.3, Recommended Operating Conditions (2) is added as follows.

After correction

Table 45.3 Recommended Operating Conditions (2)

Item	Symbol	Value
Decoupling capacitance to stabilize the internal voltage	C_{VCL}	0.47 µF ± 30%*1

Note 1. Use a multilayer ceramic capacitor whose nominal capacitance is 0.47 µF and a capacitance tolerance is ±30% or better.

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The output voltage of the VCL pin is added to Table 45.4, DC Characteristics (2) as follows.

After correction

Table 45.4 DC Characteristics (2)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output voltage of the VCL pin	V_{CL}	—	1.25	—	V	

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Descriptions of total output current in Table 45.11, Permissible Output Currents are modified as follows.

Before correction

Item		Symbol	Min.	Typ.	Max.	Unit
(Omitted)						mA
Permissible low-level output current (total)	Total of all output pins (except for RIIC pins, P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65)	ΣI_{OL}	—	—	110	
	Total of pins P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65		—	—	110	
(Omitted)						
Permissible high-level output current (total)	Total of all output pins (except for P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65)	ΣI_{OH}	—	—	–35	
	Total of pins P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65		—	—	–35	

After correction

Item		Symbol	Min.	Typ.	Max.	Unit
(Omitted)						mA
Permissible low-level output current (total)	Total of all output pins	ΣI_{OL}	—	—	110	
(Omitted)						
Permissible high-level output current (total)	Total of all output pins	ΣI_{OH}	—	—	–35	

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Figure 45.14 is corrected as follows.

Before correction

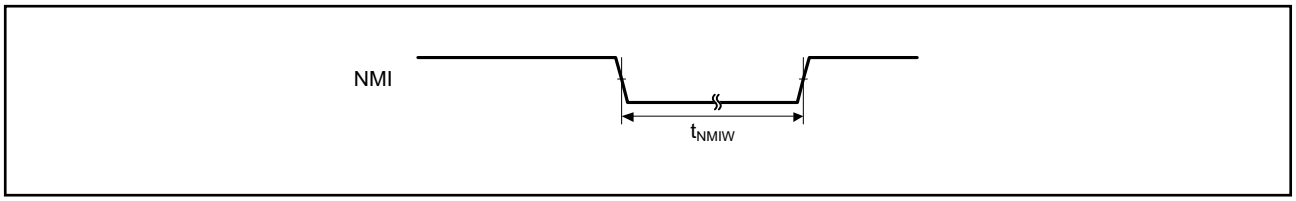

Figure 45.14 NMI Interrupt Input Timing

After correction

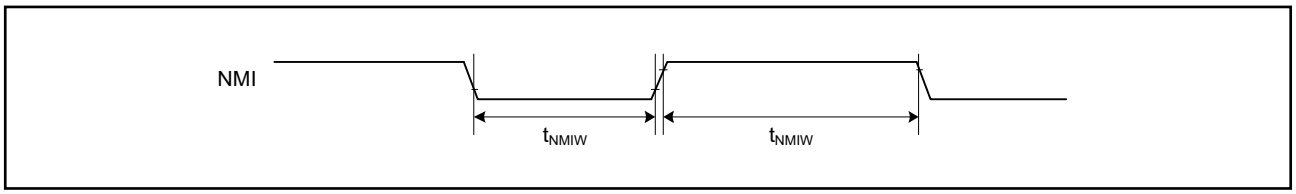

Figure 45.14 NMI Interrupt Input Timing

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Figure 45.15 is corrected as follows.

Before correction

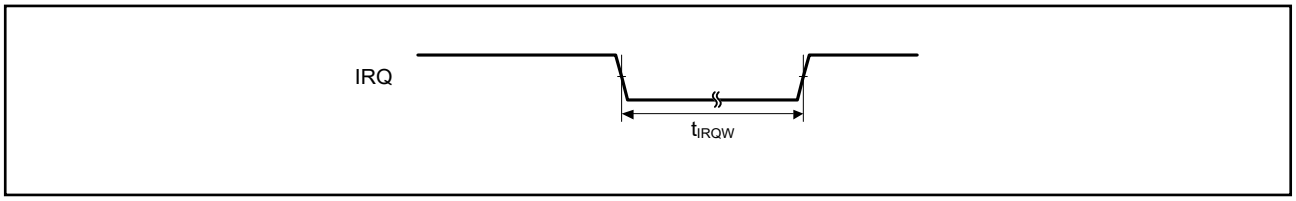

Figure 45.15 IRQ Interrupt Input Timing

After correction

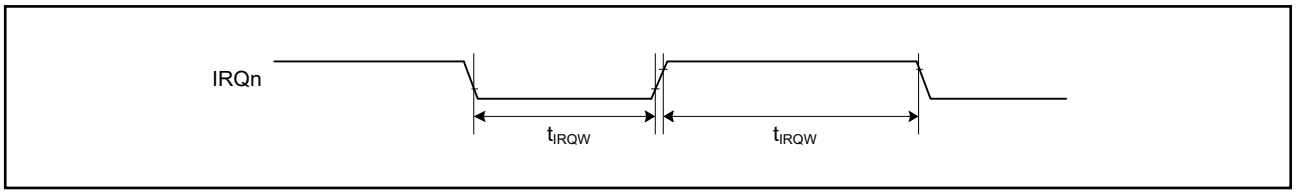

Figure 45.15 IRQ Interrupt Input Timing

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Maximum value for t_{POEGDC} in Table 45.30, POE and POEG Timing is corrected and some expressions are modified as follows.

Before correction

Item			Symbol	Min.	typ.	Max.	Unit*1	Test Conditions
POE	POEn# input pulse width (n = 0, 4, and 8 to 14)		t_{POEW}	(Omitted)				
	Time to control disabling of the output	Detection of input level	t_{POEDI}					
		Comparison of output levels	t_{POEDO}					
		Detection by a comparator	t_{POEDC}					
		Disabling software by a register setting	t_{POEDS}					
		Oscillation stop detection	t_{POEDOS}					
POEG	GTETRGn input pulse width (n = A to D)		t_{POEGW}					
	Time to control disabling of the output (with the detection flag in use)	Detection of input level	t_{POEGDI}					
		Detection of disabling of the output from the GPTW (due to a deadtime error or simultaneous driving of outputs to the high or low level)	t_{POEGDE}					
		Detection by a comparator	t_{POEGDC}	—	—	3 PCLKB + 0.5	μs	Figure 45.36 The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by comparator C.
		Disabling software by a register setting	t_{POEGDS}	(Omitted)				
		Oscillation stop detection	$t_{POEGDOS}$					
	Time to control disabling of the output (direct control by detection signals)	Detection of input level	$t_{POEGDDI}$					
		Detection of comparator level	$t_{POEGDDC}$					

After correction

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POE	POEn# input pulse width (n = 0, 4, and 8 to 14)		t_{POEW}	(Omitted)				
	Output disable time	Transition of the POEn# signal level	t_{POEDI}					
		Simultaneous conduction of output pins	t_{POEDO}					
		Detection of comparator outputs	t_{POEDC}					
		Register setting	t_{POEDS}					
		Oscillation stop detection	t_{POEDOS}					
POEG	GTETRGn input pulse width (n = A to D)		t_{POEGW}					
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}					
		Detection of the output stopping signal from GPTW (deadtime error, simultaneous high output, or simultaneous low output)	t_{POEGDE}					
		Edge detection signal from a comparator	t_{POEGDC}	—	—	4 PCLKB + 0.5	µs	Figure 45.36 The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by comparator C.
		Register setting	t_{POEGDS}	(Omitted)				
		Oscillation stop detection	$t_{POEGDOS}$					
		Input level detection of the GTETRGn pin (direct path)	$t_{POEGDDI}$					
		Level detection signal from a comparator	$t_{POEGDDC}$					

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Figure 45.28 is corrected as follows.

Before correction

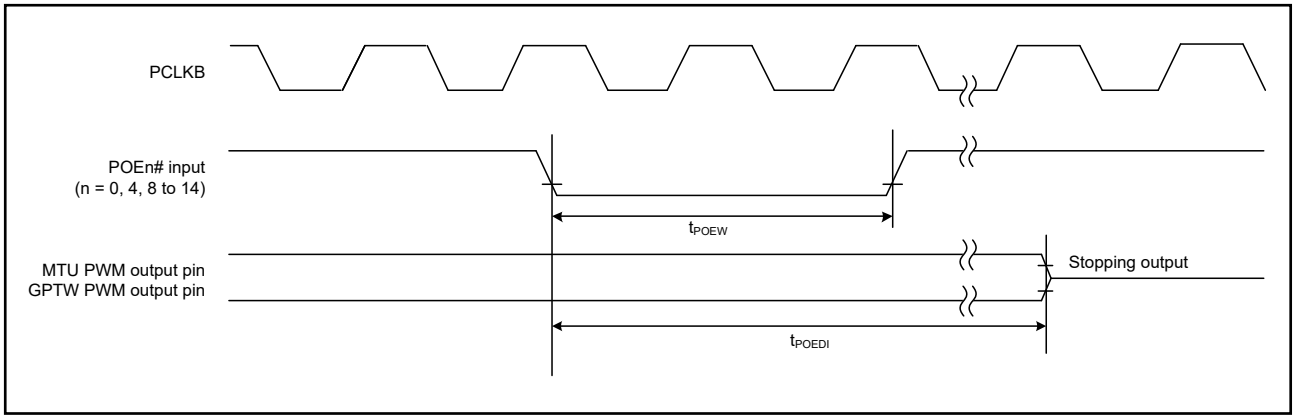

Figure 45.28 Time to Control Disabling of the Output when the POE Input Level is Detected

After correction

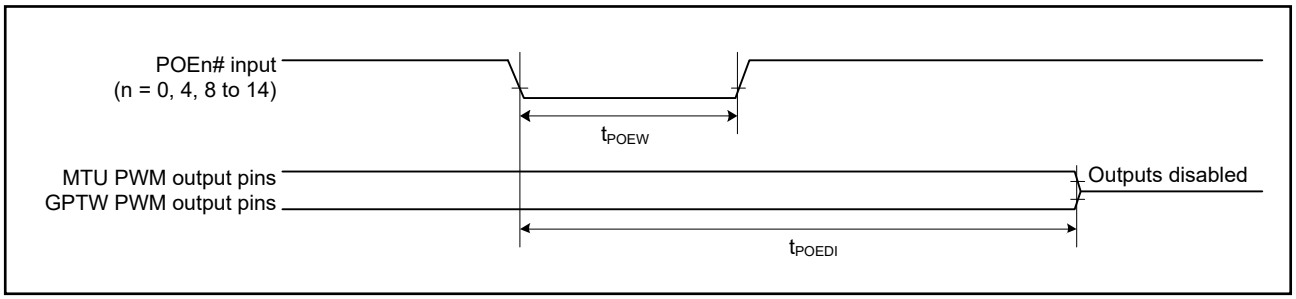

Figure 45.28 Output Disable Time for POE in Response to Transition of the POEn# Signal Level

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Figure 45.29 is corrected as follows.

Before correction

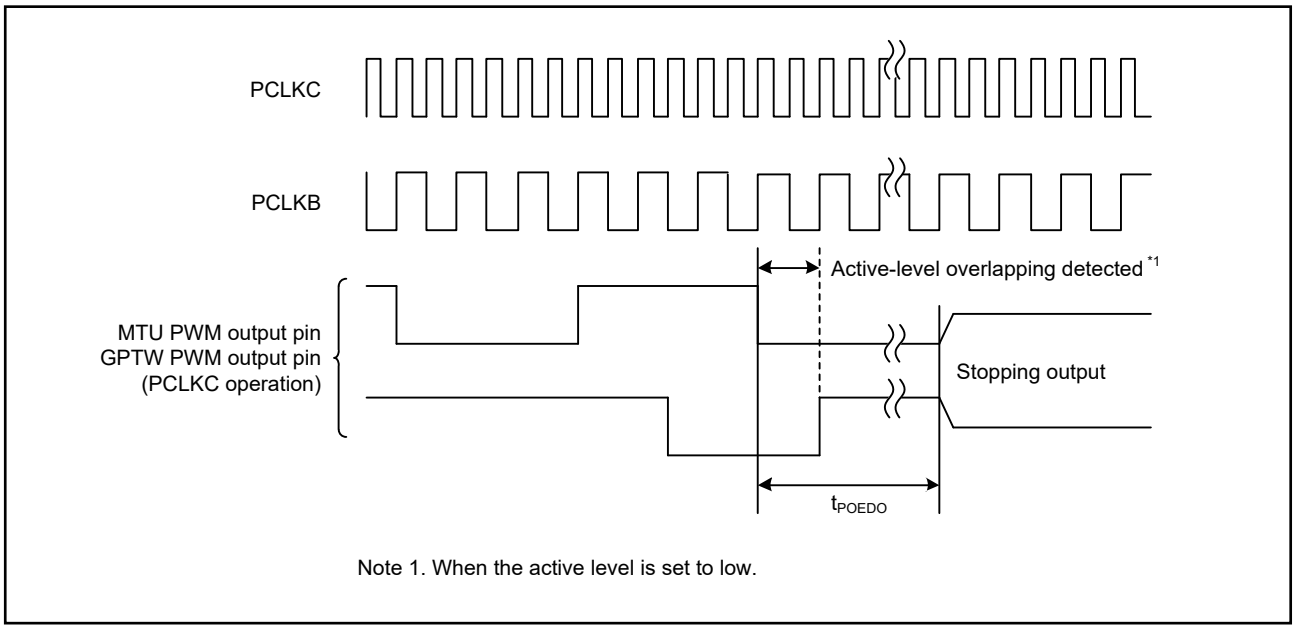

Figure 45.29 Time to Control Disabling of the Output in Response to POE Output Level Comparison

After correction

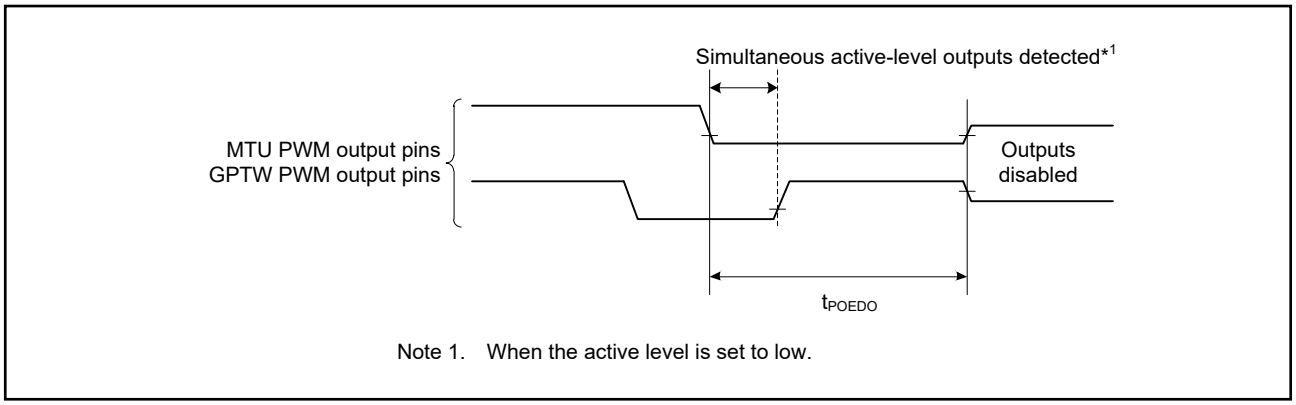

Figure 45.29 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

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Figure 45.30 is corrected as follows.

Before correction

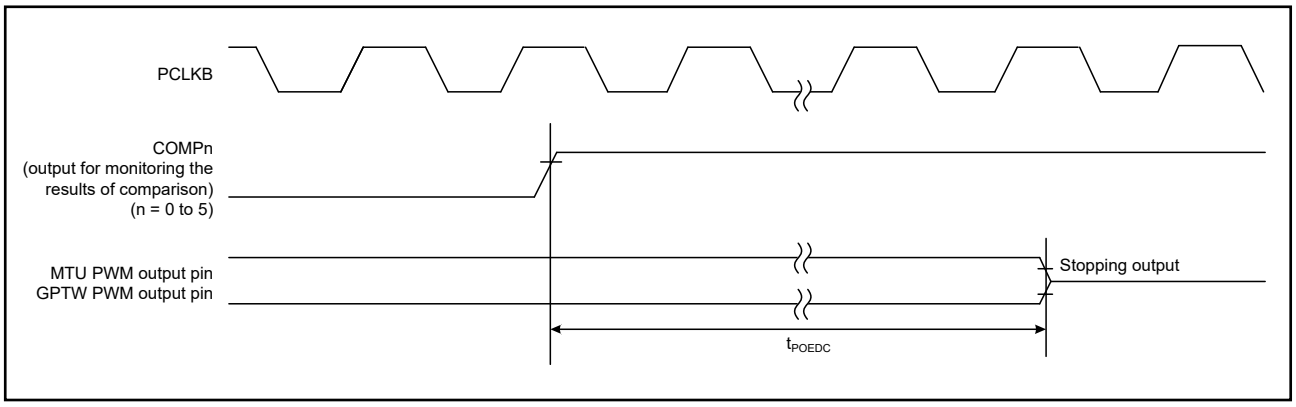

Figure 45.30 Time to Control Disabling of the Output Due to Detection by the POE Comparator

After correction

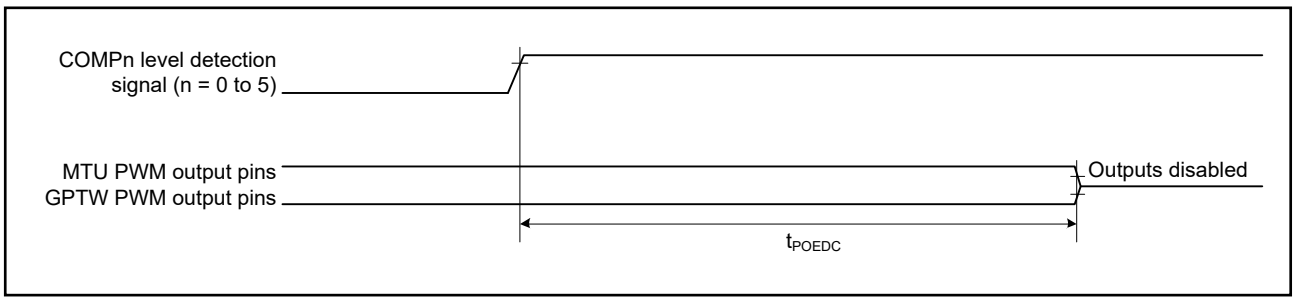

Figure 45.30 Output Disable Time for POE in Response to Detection of the Comparator Outputs

• Page 2266 of 2314

Figure 45.31 is corrected as follows.

Before correction

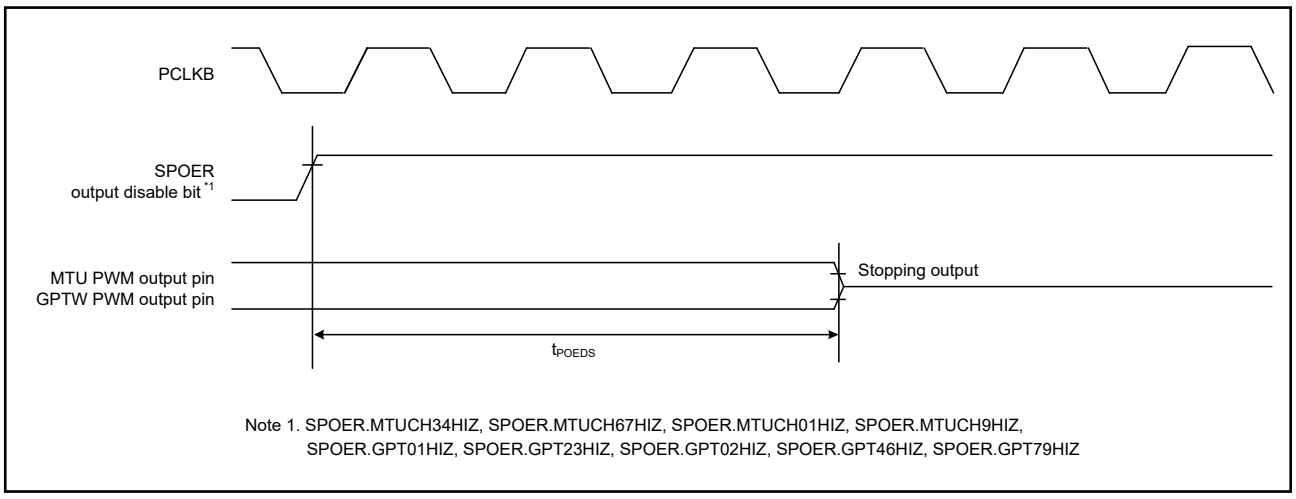

Figure 45.31 Time to Control Disabling of the Output when Software Disables Output by Setting the Given POE Register

After correction

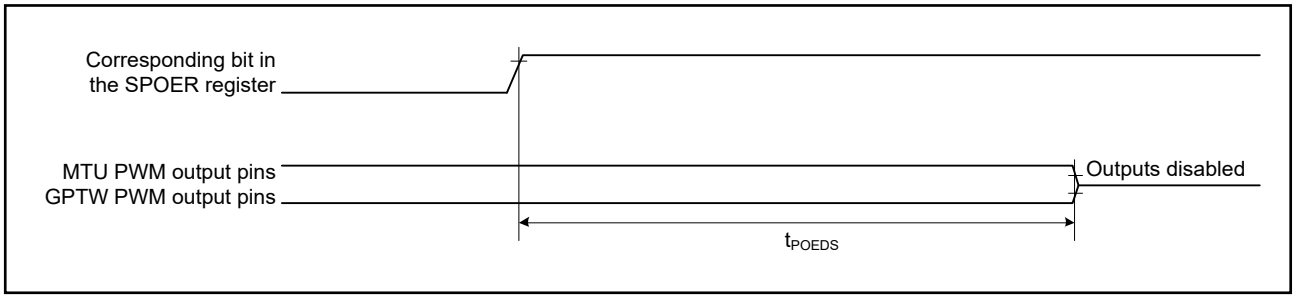

Figure 45.31 Output Disable Time for POE in Response to the Register Setting

• Page 2266 of 2314

Figure 45.32 is corrected as follows.

Before correction

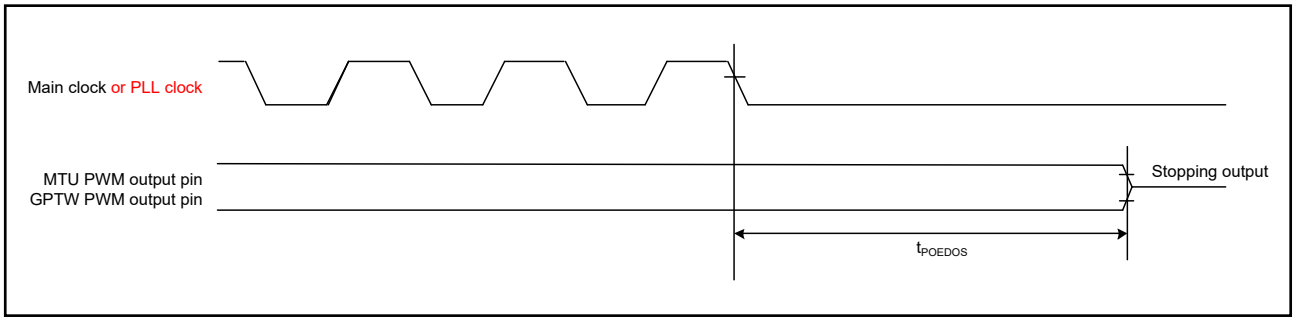

Figure 45.32 Time to Control Disabling of the Output when Disabling is Due to Detecting Stopping of Oscillation by POE

After correction

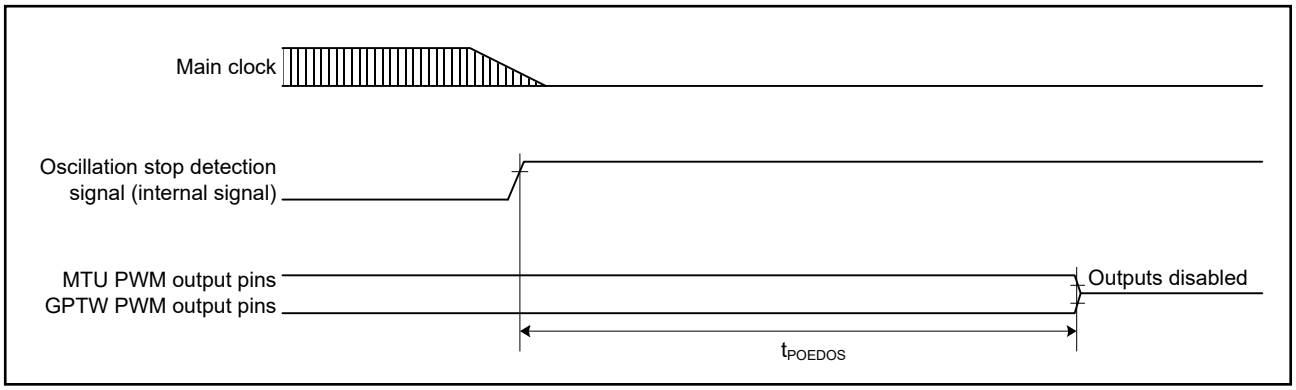

Figure 45.32 Output Disable Time for POE in Response to the Oscillation Stop Detection

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Figure 45.34 is corrected as follows.

Before correction

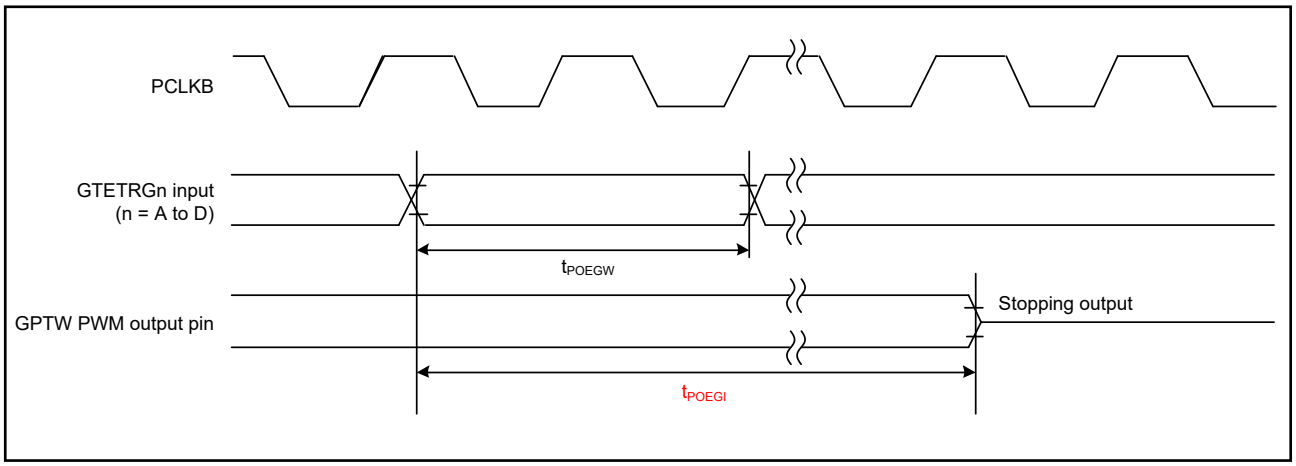

Figure 45.34 Time to Control Disabling of the Output from the POEG in Response to the Port Input Detection Flag

After correction

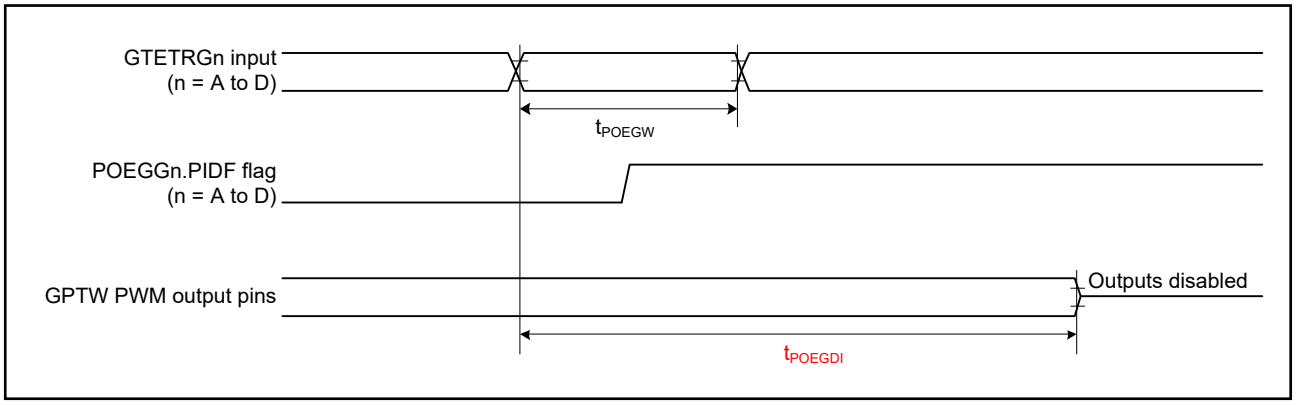

Figure 45.34 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRGn pin

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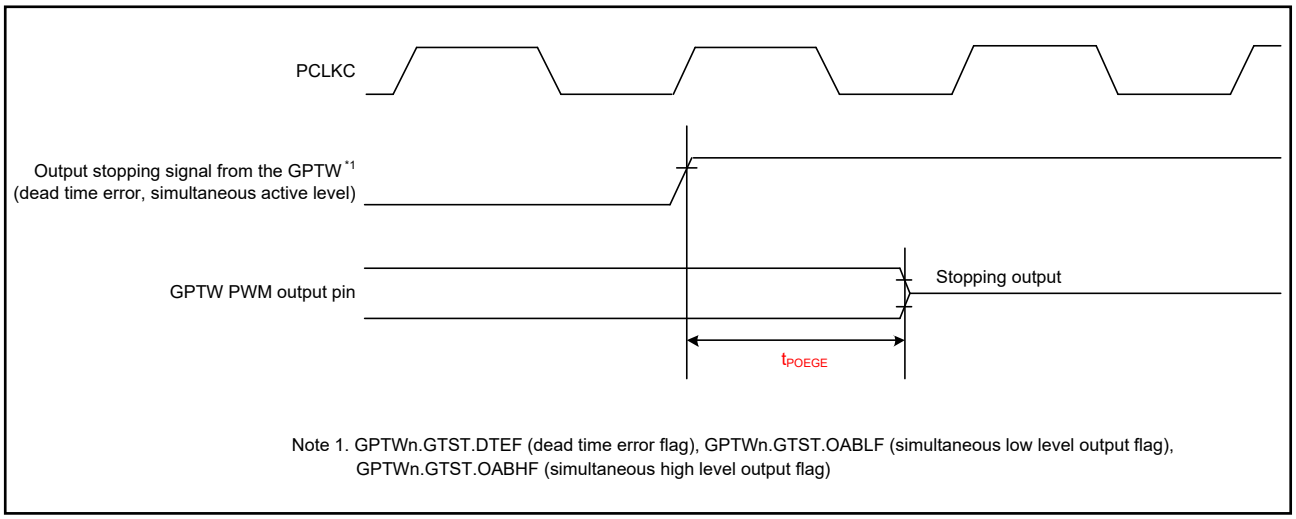
Figure 45.35 is corrected as follows.

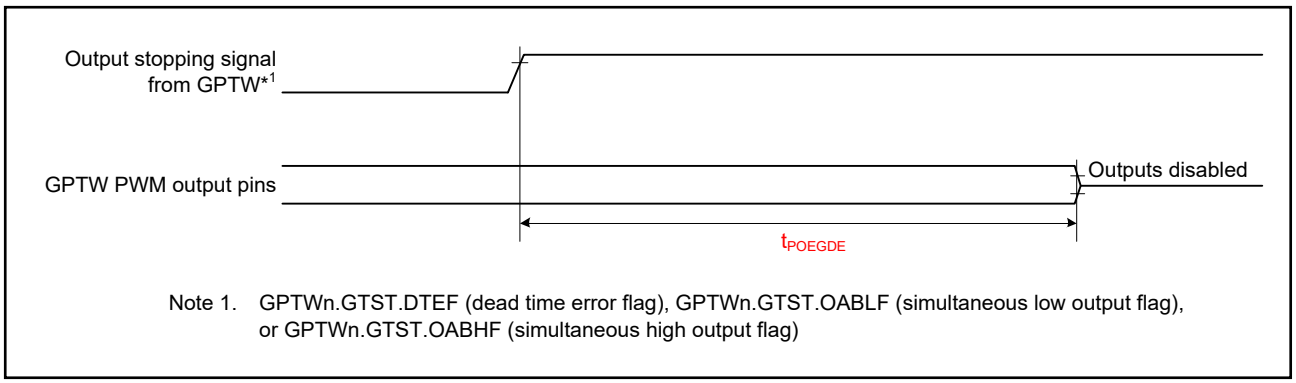
Before correction



Note 1. GPTWn.GTST.DTEF (dead time error flag), GPTWn.GTST.OABLF (simultaneous low level output flag), GPTWn.GTST.OABHF (simultaneous high level output flag)

Figure 45.35 Time to Control Disabling of the Output from POEG in Response to Detection of the Disabling Signal from GPTW

After correction



Note 1. GPTWn.GTST.DTEF (dead time error flag), GPTWn.GTST.OABLF (simultaneous low output flag), or GPTWn.GTST.OABHF (simultaneous high output flag)

Figure 45.35 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPTW

• Page 2268 of 2314

Figure 45.36 is corrected as follows.

Before correction

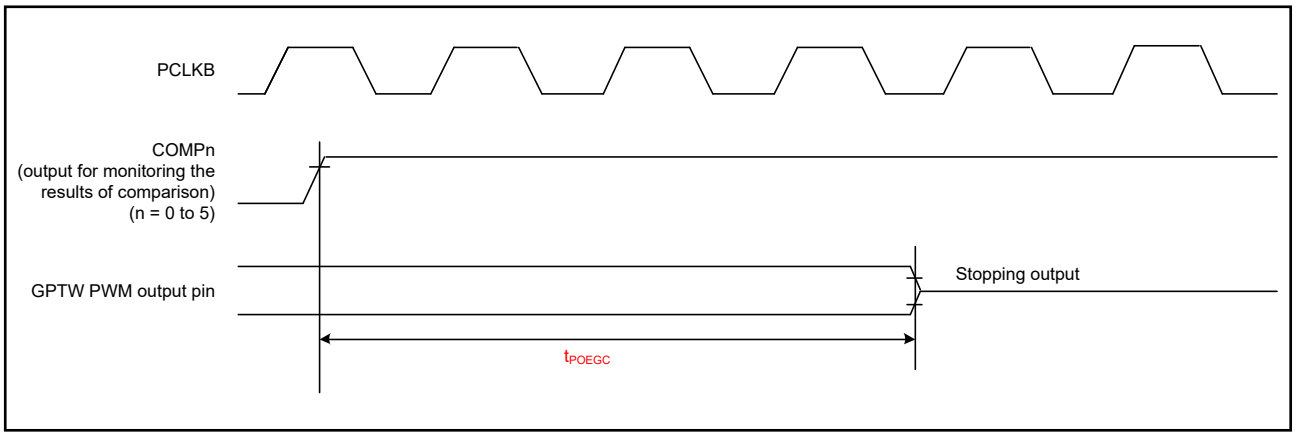


Figure 45.36 Time to Control Disabling of the Output from the POEG in Response to Edge Detection by the Comparator

After correction

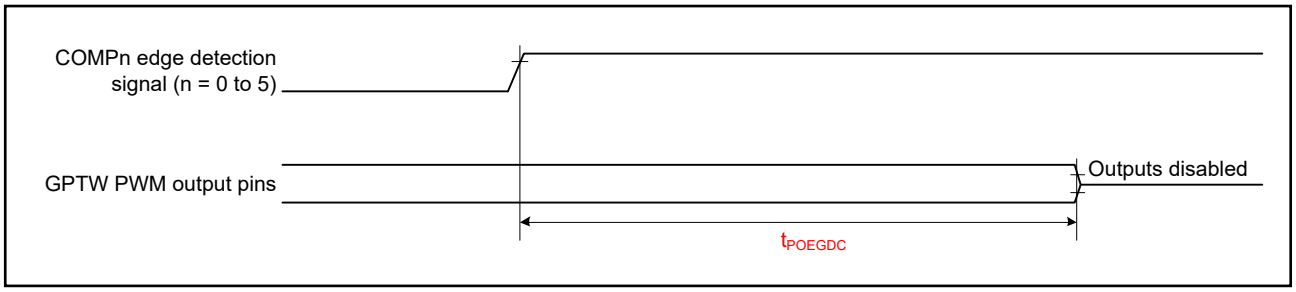


Figure 45.36 Output Disable Time for POEG in Response to Edge Detection Signal from a Comparator

• Page 2268 of 2314

Figure 45.37 is corrected as follows.

Before correction

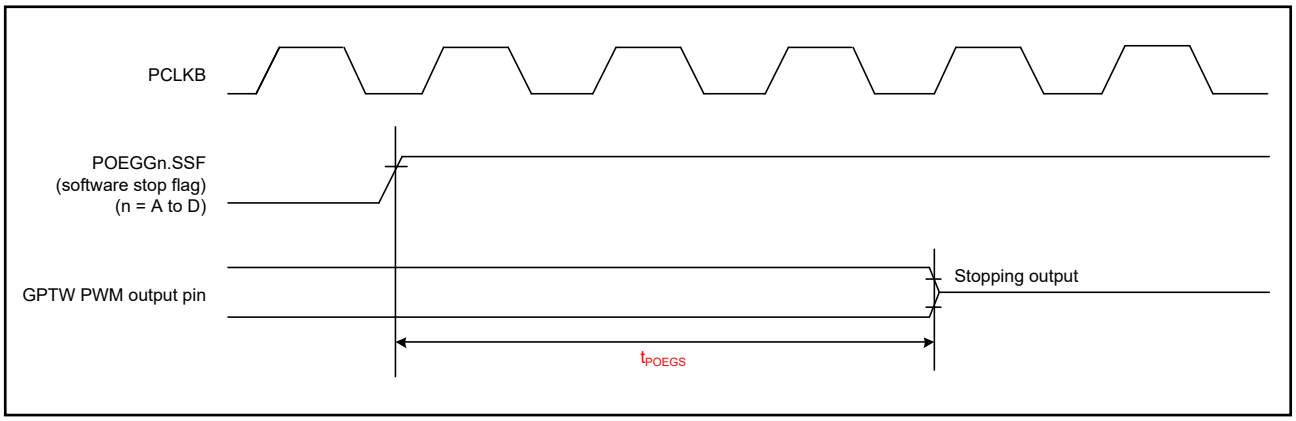


Figure 45.37 Time to Control Disabling of the Output in Response to Detecting Stopping of Oscillation by POEG

After correction

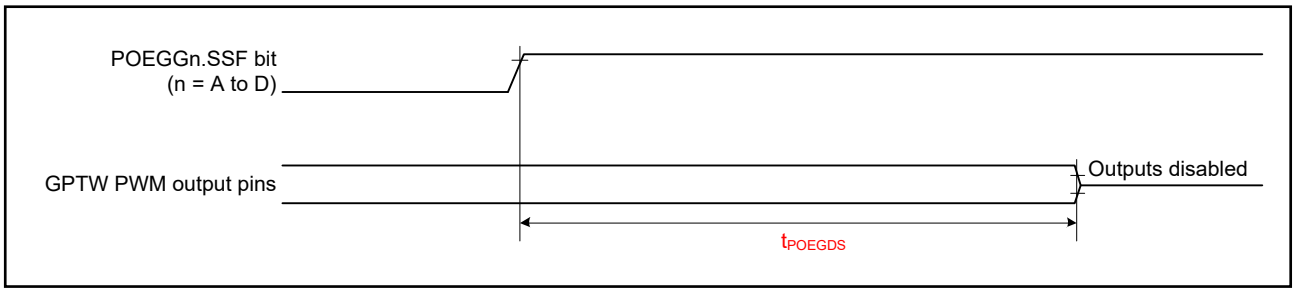


Figure 45.37 Output Disable Time for POEG in Response to the Register Setting

• Page 2268 of 2314

Figure 45.38 is corrected as follows.

Before correction

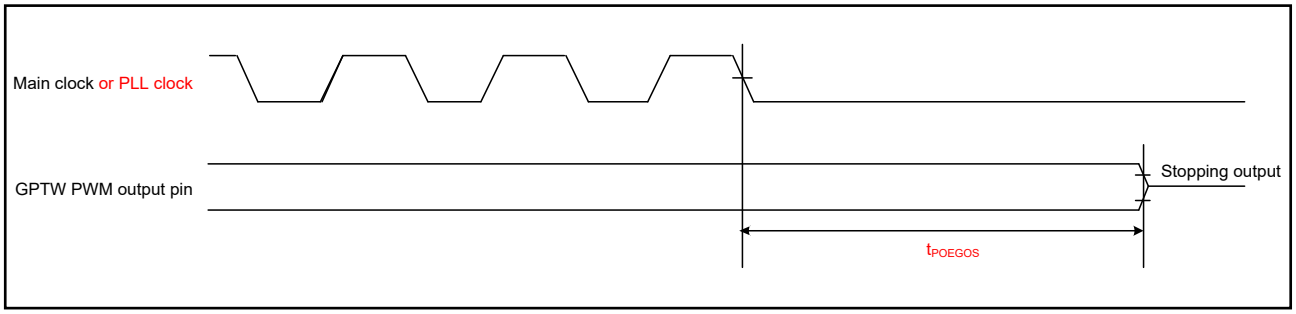


Figure 45.38 Time to Control Disabling of the Output when Disabling POEG oscillation

After correction

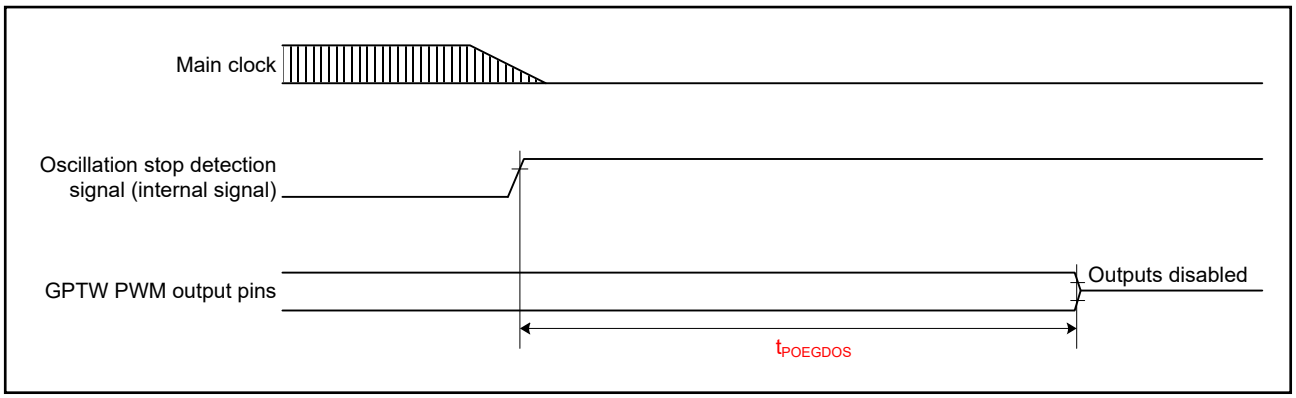


Figure 45.38 Output Disable Time of POEG in Response to the Oscillation Stop Detection

• Page 2269 of 2314

Figure 45.39 is corrected as follows.

Before correction

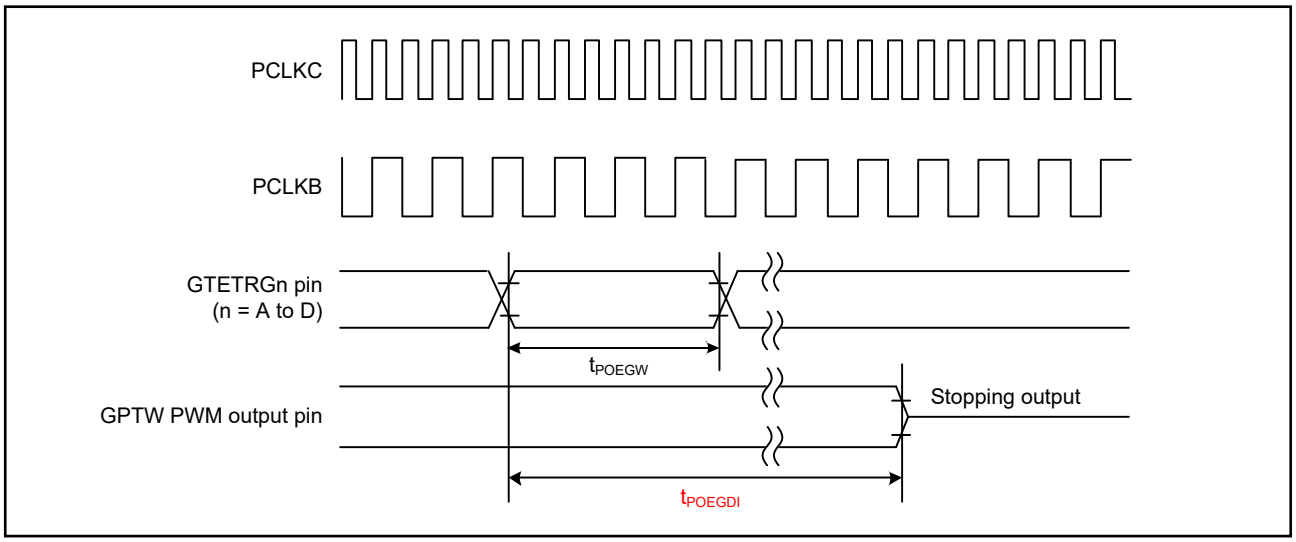


Figure 45.39 Time to Control Disabling of the Output from POEG under Direct Control by Input Level Detection Signal

After correction

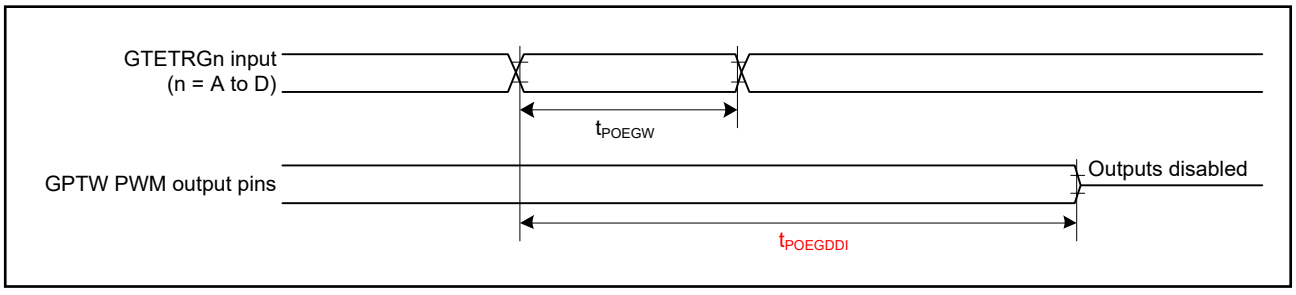


Figure 45.39 Output Disable Time for POEG in Direct Response to the Input Level Detection of the GTETRGn pin

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Figure 45.40 is corrected as follows.

Before correction

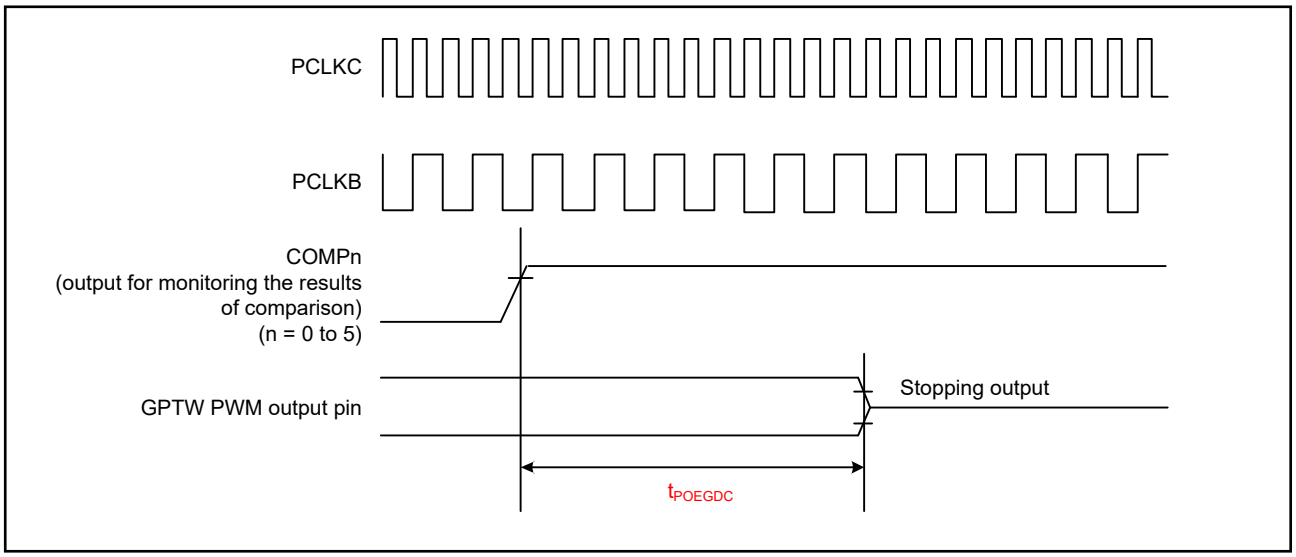

Figure 45.40 Time to Control Disabling of the Output from POEG under Direct Control in Response to Detecting the Comparator Level

After correction

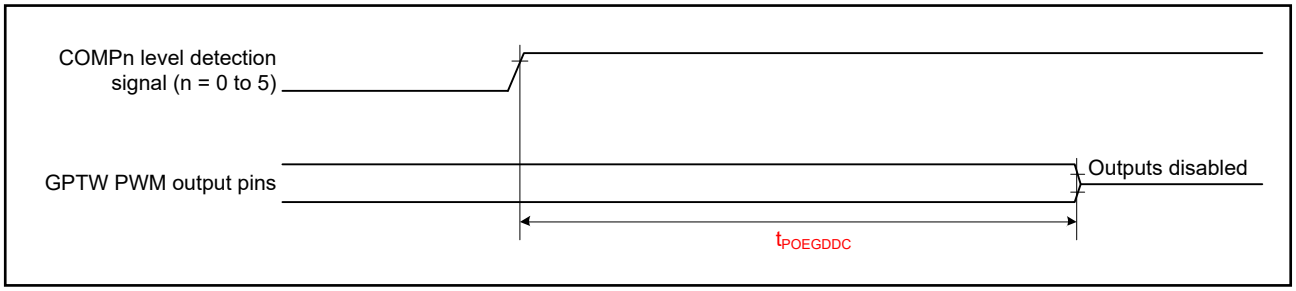

Figure 45.40 Output Disable Time for POEG in Response to Level Detection Signal from a Comparator

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Units in Table 45.35, RSPI Timing are corrected as follows.

Before correction

Item			Symbol	Min.*1	Max.*1	Unit*1	Test Conditions
RSPI	(Omitted)						
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	Figure 45.47
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—	t_{SPcyc}	
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—	t_{SPcyc}	
	(Omitted)						

After correction

Item			Symbol	Min.*1	Max.*1	Unit*1	Test Conditions
RSPI	(Omitted)						
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	Figure 45.47
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—	ns	
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—	ns	
	(Omitted)						

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A line of “Output load conditions” of conditions in Table 45.37, RIIC Timing is deleted as follows.

Before correction

Table 45.37 RIIC Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

After correction

Table 45.37 RIIC Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

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A line of "Output load conditions" of conditions in Table 45.38, Simple IIC Timing is deleted as follows.

Before correction

Table 45.38 Simple IIC Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

After correction

Table 45.38 Simple IIC Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

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The conversion time in Table 45.42, 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (1) is corrected as follows.

Before correction

Table 45.42 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (1)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, 4.5 V ≤ AVCC0 = AVCC1 = AVCC2 ≤ 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 60 MHz*1

Item		Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)						
Conversion time*2 (Operation at PCLKD = 60 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	(Omitted)				μs	(Omitted)
	AN216 to AN217	1.10	—	—		• Sampling time: 39 PCLKD
(Omitted)						

After correction

Table 45.42 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (1)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, 4.5 V ≤ AVCC0 = AVCC1 = AVCC2 ≤ 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 60 MHz*1,
Source impedance = 1.0 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)						
Conversion time*2 (Operation at PCLKD = 60 MHz)	(Omitted)				μs	(Omitted)
	AN216 to AN217	1.05	—	—		• Sampling time: 39 PCLKD
(Omitted)						

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The conversion time in Table 45.43, 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (2) is corrected as follows.

Before correction

Table 45.43 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (2)

Conditions: VCC = 2.7 to 4.5 V, VCC_USB = 2.7 to 4.5 V, 3.0 V ≤ AVCC0 = AVCC1 = AVCC2 < 4.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 40 MHz

Item			Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)							
Conversion time*1 (Operation at PCLKD = 40 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	AN000 to AN002, AN100 to AN102	(Omitted)				μs	(Omitted)
		Channel-dedicated sample-and-hold circuits not in use	1.15	—	—		• Sampling time: 21 PCLKD
	AN003 to AN006, AN103 to AN106		1.15	—	—		• Sampling time: 21 PCLKD
	(Omitted)						(Omitted)
	AN216 to AN217		1.30	—	—		• Sampling time: 27 PCLKD
(Omitted)							

After correction

Table 45.43 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (2)

Conditions: VCC = 2.7 to 4.5 V, VCC_USB = 2.7 to 4.5 V, 3.0 V ≤ AVCC0 = AVCC1 = AVCC2 < 4.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 40 MHz,
Source impedance = 1.0 kΩ

Item			Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)							
Conversion time*1 (Operation at PCLKD = 40 MHz)	AN000 to AN002, AN100 to AN102	(Omitted)				μs	(Omitted)
		Channel-dedicated sample-and-hold circuits not in use	1.13	—	—		• Sampling time: 21 PCLKD
	AN003 to AN006, AN103 to AN106		1.13	—	—		• Sampling time: 21 PCLKD
	(Omitted)						(Omitted)
	AN216 to AN217		1.28	—	—		• Sampling time: 27 PCLKD
(Omitted)							

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The expression and symbol for output voltage in Table 45.45, Programmable Gain Amplifier Characteristics (single-ended input) are corrected as follows.

Before correction

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)						
Single-ended output voltage range	V_{OSR}	0.10 × AVCCn	—	0.90 × AVCCn	V	G = 2.000 to 3.636
		0.15 × AVCCn	—	0.85 × AVCCn		G = 4.000 to 6.667
		0.20 × AVCCn	—	0.80 × AVCCn		G = 8.000 to 20.000
(Omitted)						

After correction

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)						
Output voltage range	V_{OR}	0.10 × AVCCn	—	0.90 × AVCCn	V	G = 2.000 to 3.636
		0.15 × AVCCn	—	0.85 × AVCCn		G = 4.000 to 6.667
		0.20 × AVCCn	—	0.80 × AVCCn		G = 8.000 to 20.000
(Omitted)						

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The expression and symbol for output voltage in Table 45.46, Programmable Gain Amplifier Characteristics (pseudo-differential input) are corrected as follows.

Before correction

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)						
Differential output voltage range	V_{ODR}	0.22 × AVCC	—	0.78 × AVCC	V	
(Omitted)						

After correction

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
(Omitted)						
Output voltage range	V_{OR}	0.22 × AVCC	—	0.78 × AVCC	V	
(Omitted)						