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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-RX*-A069A/E	Rev.	1.00
Title	Errata to RX630, RX63N, RX631, and RX63T Groups User's Manuals Regarding CAN Module		Information Category	Technical Notification		
Applicable Product	RX630 Group RX63N Group, RX631 Group RX63T Group	Lot No. All	Reference Document	RX630 Group User's Manual: Hardware Rev.1.50 (R01UH0040EJ0150) RX63N Group, RX631 Group User's Manual: Hardware Rev.1.60 (R01UH0041EJ0160) RX63T Group User's Manual: Hardware Rev.2.00 (R01UH0238EJ0200)		

This document describes corrections to the chapter "CAN module" in the User's Manuals: Hardware of the above groups.
The corrections are indicated in red in the list below.

Page and section numbers are based on the RX630 Group. Refer to the table on the last page for the corresponding pages and chapters in other groups.

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The description of BLIF Flag in 34.2.19 is corrected as follows:

Before correction

The BLIF bit is set to 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.
After the BLIF bit is set to 1, 32 consecutive dominant bits are detected again under either of the following conditions:

- After this bit is set to 0 from 1, recessive bits are detected
- After this bit is set to 0 from 1, the CAN module enters CAN reset mode or CAN halt mode and then enters CAN operation mode again.

Corrections

The BLIF flag becomes 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.
After the BLIF flag becomes 1, bus lock can be detected again after either of the following conditions is satisfied:

- After this flag is set to 0 from 1, recessive bits are detected (bus lock is resolved).
- After this flag is set to 0 from 1, the CAN module enters CAN reset mode and then enters CAN operation mode again (internal reset).

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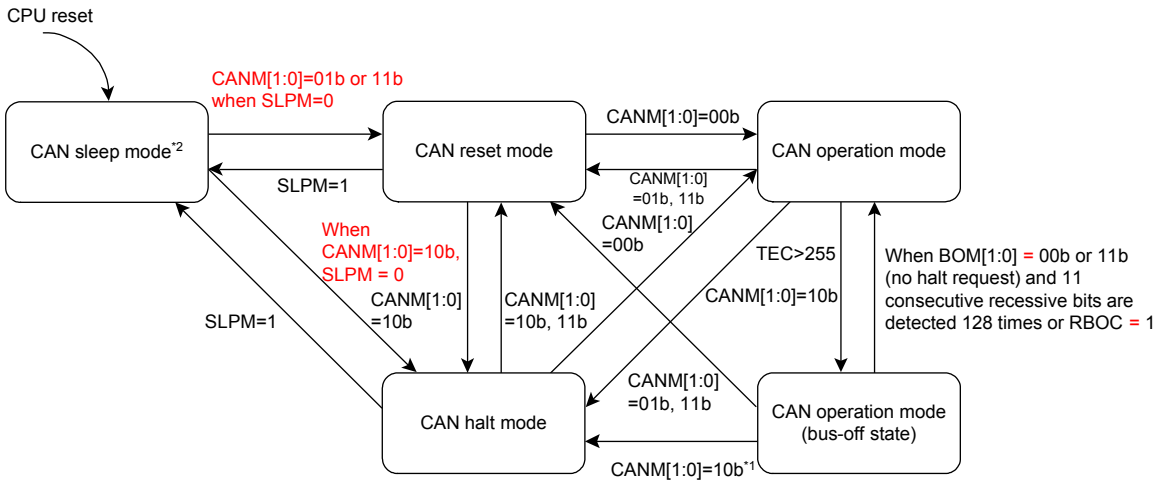
Figure 34.9 is corrected as follows:

Before correction

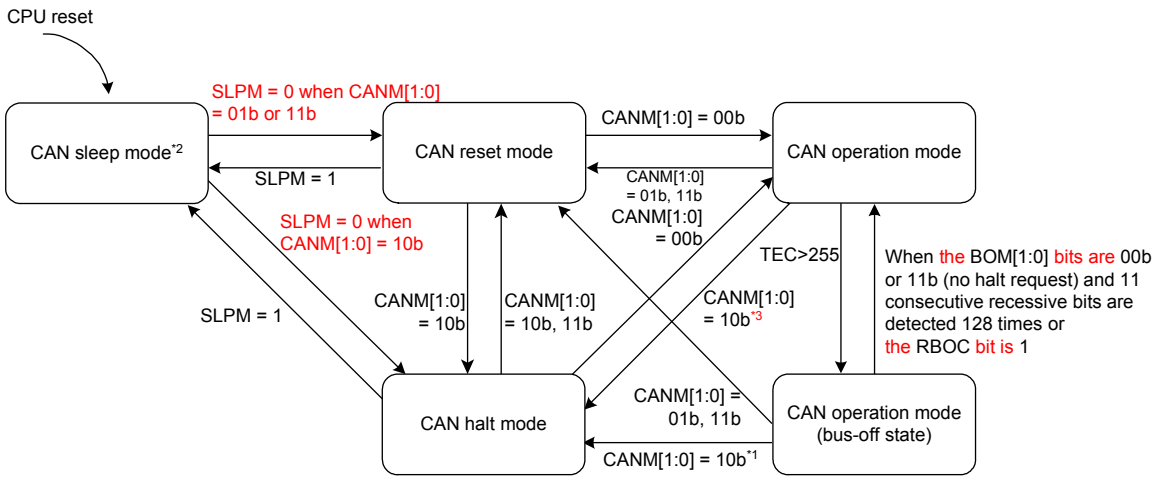


CANM, SLPM, BOM, RBOC: Bits in CTLR

Note 1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the C TLR.BOM[1:0] bits.
When the CTLR.BOM[1:0] bits are 01b, the state transition timing is immediately after entering the bus-off state.
When the CTLR.BOM[1:0] bits are 10b, the state transition timing is at the end of the bus-off state.
When the CTLR.BOM[1:0] bits are 11b, the state transition timing is at the setting of the C TLR.CANM[1:0] bits to 10b (CAN halt mode).
Note 2. Change the CTLR.SLPM bit to set or cancel CAN sleep mode.

Figure 34.9 Transition between CAN Operating Modes

Corrections



CANM, SLPM, BOM, RBOC: Bits in CTLR

Note 1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the CTLR.BOM[1:0] bits.
- When the CTLR.BOM[1:0] bits are 01b, the state transition timing is immediately after entering the bus-off state.
- When the CTLR.BOM[1:0] bits are 10b, the state transition timing is at the end of the bus-off state.
- When the CTLR.BOM[1:0] bits are 11b, the state transition timing is at the setting of the CTLR.CANM[1:0] bits to 10b (CAN halt mode).
Note 2. Change the CTLR.SLPM bit to set or cancel CAN sleep mode.
Note 3. The CAN module does not enter CAN halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

Figure 34.9 Transition between CAN Operating Modes

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Table 34.8 is corrected as follows:

Before correction

Table 34.8 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-off
CAN reset mode (forcible transition) CANM[1:0] = 11b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM[1:0] = 01b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission.*1,*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception.*2,*3	CAN module enters CAN halt mode after waiting for the end of message transmission.*1,*4	[When the BOM[1:0] bits are 00b] A halt request from a program will be accepted only after bus-off recovery. [When the BOM[1:0] bits are 01b] CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 10b] CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 11b] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

BOM[1:0] bits: Bits in CTLR

Note 1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.

Note 2. If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF bit in EIFR.

Note 3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module transits to CAN halt mode.

Note 4. If a CAN bus error or arbitration-lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module transits to the requested CAN mode.

Corrections

Table 34.8 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-off
CAN reset mode (forcible transition) CANM[1:0] = 11b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM[1:0] = 01b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission.*1,*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception.*2,*3	CAN module enters CAN halt mode after waiting for the end of message transmission.*1,*2,*4	[When the BOM[1:0] bits are 00b] A halt request from a program will be accepted only after bus-off recovery. [When the BOM[1:0] bits are 01b] CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 10b] CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM[1:0] bits are 11b] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

CANM[1:0], BOM[1:0]: Bits in CTLR

Note 1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first message transmission. In a case that the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.

Note 2. If the CAN bus is locked in dominant state, the program can detect this state by monitoring the EIFR.BLIF flag. The CAN module does not enter CAN halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

Note 3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

Note 4. If a CAN bus error or arbitration-lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

<Reference Documents>

Applicable Product	Manual and Document Number	Page Number, Figure/Title Number		
		BLIF Bit	Figure X.34	Table X.8
RX630 Group	RX630 Group User's Manual: Hardware Rev.1.50 (R01UH0040EJ0150)	Page 1249 34.2.19	Page 1254 Figure 34.9	Page 1256 Table 34.8
RX63N Group RX631 Group	RX63N Group, RX631 Group User's Manual: Hardware Rev.1.60 (R01UH0041EJ0160)	Page 1513 37.2.19	Page 1518 Figure 37.9	Page 1520 Table 37.8
RX63T Group	RX63T Group User's Manual: Hardware Rev.2.00 (R01UH0238EJ0200)	Page 1333 31.2.19	Page 1338 Figure 31.9	Page 1340 Table 31.8