Date: Aug. 8, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A0268A/E	Rev.	1.00
Title	Errata to the RX26T Group User's Manual: Hardware Rev.1.01		Information Category	Technical Notification		
Applicable Product	RX26T Group	Lot No. All	Reference Document	RX26T Group User's Manual: Hardware Rev.1.01 (R01UH0979EJ0101)		

This document describes corrections to the RX26T Group User's Manual: Hardware Rev.1.01.

- Page 1018 of 2908

The descriptions for the CSCMSC[2:0] bits in section 24.2.7, General PWM Timer Clear Source Select Register (GTCSR), are modified as follows.

Before correction

CSCMSC[2:0] Bits (Compare Match/Input Capture/Synchronous Counter Clearing Source Counter Clear Enable)

Select whether to enable or disable for the counter clear of the GTCNT counter by compare match/input capture/ synchronous counter clearing group.
Since the compare match by the register that is performing the buffer operation (including the wave mode specific case) does not occur, the counter clear enable setting that makes the target register of the buffer operation the compare match factor is invalid.
In complementary PWM mode, the counter clear enable setting for compare match of the GTCCRB register, GTCCRE register, and GTCCRF register is invalid even when the buffer operation is not performed.

After correction

CSCMSC[2:0] Bits (Compare Match/Input Capture/Synchronous Counter Clearing Source Counter Clear Enable)

Select whether to enable or disable for the counter clear of the GTCNT counter by compare match/input capture/ synchronous counter clearing group. When counter clearing in response to a match in comparison or input capture is enabled, either can be used as a source for synchronous clearing by inter channel cooperation as described in section 24.3.8.3, Synchronous Clear Operation by Inter Channel Cooperation. When counter clearing by input capture is enabled while the setting of the CSCMSC[2:0] bits is 001b or 010b, the same sources for input capture as one set in the GTICmSR (m = A, B) register must be set as the counter clearing sources in the GTCSR register. Note that input capture on other channels cannot be used as the source to drive counter clearing, that is, the GTICASR.ASOC or GTICBSR.BSOC bit cannot be set to 1.
Since the compare match by the register that is performing the buffer operation (including the wave mode specific case) does not occur, the counter clear enable setting that makes the target register of the buffer operation the compare match factor is invalid.
In complementary PWM mode, the counter clear enable setting for compare match of the GTCCRB register, GTCCRE register, and GTCCRF register is invalid even when the buffer operation is not performed.

• Page 1031 and 1033 of 2908

The CPSCD bit in section 24.2.12, General PWM Timer Control Register (GTCR), is deleted.

Before correction

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	CKEG[1:0]		TPCS[3:0]				—	—	—	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSCEN	—	—	CPSCD	SSCGRP[1:0]		SCGTIOC	ICDS	—	—	—	—	—	—	—	CST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
			(Omitted)	
b11, b10	SSCGRP[1:0]	Synchronous Set/Clear Group Select	b11 b10 0 0: Select synchronous set/clear group A 0 1: Select synchronous set/clear group B 1 0: Select synchronous set/clear group C 1 1: Select synchronous set/clear group D	R/W *1
b12	CPSCD	Complementary PWM Mode Synchronous Clear Disable *2	0: Enable synchronous counter clear by other channel other than trough in complementary PWM mode 1: Disable synchronous counter clear by other channel other than trough in complementary PWM mode	R/W *1
b14, b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	SSCEN	Synchronous Set/Clear Enable	0: Disable Synchronous set/clear of the GTCNT counter 1: Enable Synchronous set/clear of the GTCNT counter	R/W *1
			(Omitted)	

CPSCD Bit (Complementary PWM Mode Synchronous Clear Disable)

This bit selects disable or enable of counter clear when synchronous clear from other channel occurs except trough in complementary PWM mode.

The slave channel is also controlled by setting the CPSCD bit of the master channel.

After correction

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	CKEG[1:0]		TPCS[3:0]				—	—	—	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSCEN	—	—	—	SSCGRP[1:0]		SCGTIOC	ICDS	—	—	—	—	—	—	—	CST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
			(Omitted)	
b11, b10	SSCGRP[1:0]	Synchronous Set/Clear Group Select	b11 b10 0 0: Select synchronous set/clear group A 0 1: Select synchronous set/clear group B 1 0: Select synchronous set/clear group C 1 1: Select synchronous set/clear group D	R/W *1
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	SSCEN	Synchronous Set/Clear Enable	0: Disable Synchronous set/clear of the GTCNT counter 1: Enable Synchronous set/clear of the GTCNT counter	R/W *1
			(Omitted)	

- Page 1032 of 2908

An additional condition for clearing of the CST bit in section 24.2.12, General PWM Timer Control Register (GTCR), is included as follows.

Before correction

CST Bit (Count Start)

(Omitted)

[Clearing conditions]

- When 1 is written to a bit related to a channel number for the GTSTP register while the GTPSR.CSTOP bit is set to 1
- When an ELC event input, an external trigger, or a condition for the GTIOCnA pin input and GTIOCnB pin input, which is enabled as a count stop source by the GTPSR register, is generated
- 0 is written by software

After correction

CST Bit (Count Start)

(Omitted)

[Clearing conditions]

- When 1 is written to a bit related to a channel number for the GTSTP register while the GTPSR.CSTOP bit is set to 1
- When an ELC event input, an external trigger, or a condition for the GTIOCnA pin input and GTIOCnB pin input, which is enabled as a count stop source by the GTPSR register, is generated
- A cycle-counting operation is completed while the GTPC.ASTP bit is 1
- 0 is written by software

- Page 1091 of 2908

The descriptions of the SPCD bit in section 24.2.42, General PWM Timer Operation Enable Bit Simultaneous Control Register (GTSECR), are corrected as follows.

Before correction

SPCD Bit (Cycle Count Function Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTPC.PCEN bit in the channels set to 1 by the GTSECSR register, and cycle count function is disabled.

Simultaneous setting of SPCE and SPCD bits to 1 is prohibited.

After correction

SPCD Bit (Cycle Count Function Simultaneous Disable)

Writing 1 to this bit simultaneously sets any GTPC.PCEN bits to 0 for channels with simultaneous control enabled by the setting (1) in the GTSECSR register and disables the cycle-counting function.

Simultaneous setting of SPCE and SPCD bits to 1 is prohibited.

- Page 1119 of 2908

The descriptions of the third line in Table 24.11, The GTPR Buffer Transfer Timing in Complementary PWM Mode, are corrected as follows.

Before correction

Table 24.11 The GTPR Buffer Transfer Timing in Complementary PWM Mode

Mode	Complementary PWM mode 1	Complementary PWM mode 2	Complementary PWM mode 3 Complementary PWM mode 4
		(Omitted)	
GTPBR register ↓ GTPR register	At the end of crest • Synchronous clear	At the end of trough • Synchronous clear	At the end of crest At the end of trough • Synchronous clear

After correction

Table 24.11 The GTPR Buffer Transfer Timing in Complementary PWM Mode

Mode	Complementary PWM mode 1	Complementary PWM mode 2	Complementary PWM mode 3 Complementary PWM mode 4
		(Omitted)	
GTPBR register ↓ GTPR register	At the end of crest • Counter clearing in an up-counting middle or crest section, including counter clearing enabled by setting the GTCSR.CP1CCE bit	At the end of trough • Counter clearing in a down-counting middle or trough section	At the end of crest At the end of trough • Counter clearing

• Page 1179 of 2908

The descriptions of the sixth and seventh lines in Table 24.17, Immediate Single Buffer Transfer from the GTCCRD Register in Complementary PWM Mode 4 (1), are corrected as follows.

Before correction

Table 24.17 Immediate Single Buffer Transfer from the GTCCRD Register in Complementary PWM Mode 4 (1)

Operation Section	Compare Match State	Immediate Transfer Destination Register	
		GTCCRC	GTCCRA
(Omitted)			
Up-counting crest section	(Omitted)		
	After up-counting compare match	Before down-counting compare match • In the case of GTCCRD < GPTWn+2.GTCNT GTCCRD • In the case of GTCCRD ≤ GPTWn+2.GTCNT GPTWn+2.GTCNT Negative-phase OFF After down-counting dead time start No transfer	No transfer
Down-counting crest section	Before down-counting compare match	Up-counting dead time period • In the case of GTCCRD > GPTWn+1.GTCNT GTCCRD • In the case of GTCCRD ≤ GPTWn+1.GTCNT GPTWn+1.GTCNT Negative-phase OFF After up-counting compare match • In the case of GTCCRD < GPTWn.GTCNT GTCCRD • In the case of GTCCRD ≥ GPTWn.GTCNT GPTWn.GTCNT Positive-phase OFF	No transfer
	(Omitted)		

After correction

Table 24.17 Immediate Single Buffer Transfer from the GTCCRD Register in Complementary PWM Mode 4 (1)

Operation Section	Compare Match State	Immediate Transfer Destination Register	
		GTCCRC	GTCCRA
(Omitted)			
Up-counting crest section	(Omitted)		
	After up-counting compare match	Before down-counting compare match • In the case of GTCCRD < GPTWn+2.GTCNT GTCCRD • In the case of GTCCRD ≥ GPTWn+2.GTCNT GPTWn+2.GTCNT Negative-phase OFF After down-counting dead time start No transfer	No transfer
Down-counting crest section	Before down-counting compare match	Up-counting dead time period • In the case of GTCCRD < GPTWn+1.GTCNT GTCCRD • In the case of GTCCRD ≥ GPTWn+1.GTCNT GPTWn+1.GTCNT Negative-phase OFF After up-counting compare match • In the case of GTCCRD < GPTWn.GTCNT GTCCRD • In the case of GTCCRD ≥ GPTWn.GTCNT GPTWn.GTCNT Positive-phase OFF	No transfer
	(Omitted)		

• Page 1298 and 1300 of 2908

The following subsections are added to section 24.10, Usage Notes.

24.10.3 Range of Settings for the GTPBR and GTPDBR Registers in the Complementary PWM Mode

When buffer transfer with the use of the GTPR register is to proceed at the end of a crest section in complementary PWM mode 1, 3, or 4, set the GTPBR and GTPDBR registers so that the GTPR register is within the following range after the transfer.

The range consists of values no less than the GTCNT counter value of the master channel at the end of a crest section, that is, the GTPR register before the transfer – the GTDVU register (GTPBR register ≥ GTPR register – GTDVU register, GTPDBR register ≥ GTPBR register – GTDVU register)

When buffer transfer with the use of the GTPR register is to proceed at the end of a trough section or on counter clearing, no restriction applies to the ranges of settings for the GTPBR and GTPDBR registers.

24.10.7 Note on Counter Clearing in the Complementary PWM Mode

Counter clearing at the end of a trough section or the end of the initial output section must be avoided in the complementary PWM mode. This can be achieved by using synchronous clearing in response to a match in comparison in another channel set as the source of the trigger, as described in section 24.3.8.3, Synchronous Clear Operation by Inter Channel Cooperation. When using counter clearing other than as stated above, adjust the timing of the operations to avoid counter clearing at the end of a trough section or the end of the initial output section.

24.10.8 Note on Disabling PWM Initial Output After Synchronous Clearing in the Complementary PWM Mode

When initial output on the GTIOCnA and GTIOCnB pins after synchronous clearing in a trough section in the complementary PWM mode has been disabled by setting the GTIOR.CPSCIR bit to 1, the respective values set in the compare match registers (the GTCCRA, GTCCRC, GTCCRD,GTCCRE, and GTCCRF registers) must be more than twice that of the GTDVU register.

• Page 1597 of 2908

The descriptions for the event link function in Table 33.1, RSCI Specifications (3/3), are corrected as follows.

Before correction

Table 33.1 RSCI Specifications (3/3)

Item	Description
Event link function	Error (receive error or error signal detection) event output
	Receive data full event output
	Transmit data empty event output
	Transmit end event output
	Receive data match event output
	Receive data unmatch event output
	Active edge detection event output

After correction

Table 33.1 RSCI Specifications (3/3)

Item	Description
Event link function	Error (receive error or error signal detection) event output
	Receive data full event output
	Transmit data empty event output
	Transmit end event output

• Page 1810 of 2908

Table 33.49, RSCI Event Link Signal List in section 33.18, Event Linking, is corrected as follows.

Before correction

Table 33.49 RSCI Event Link Signal List

Function	Pulse/Level	Pulse Width	Active Level	Synchronize Clock
Error event	Pulse	1 cycle	High	PCLK
Receive data full event	Pulse	1 cycle	High	PCLK
Receive data match event	Pulse	1 cycle	High	PCLK
Transmit data empty event	Pulse	1 cycle	High	PCLK
Transmit end event	Pulse	1 cycle	High	PCLK
Receive data unmatch event	Pulse	1 cycle	High	PCLK
Active edge detect event	Pulse	1 cycle	High	PCLK

After correction

Table 33.49 RSCI Event Link Signal List

Function	Pulse/Level	Pulse Width	Active Level	Synchronize Clock
Error event	Pulse	1 cycle	High	PCLK
Receive data full event	Pulse	1 cycle	High	PCLK
Transmit data empty event	Pulse	1 cycle	High	PCLK
Transmit end event	Pulse	1 cycle	High	PCLK

• Page 1811 of 2908

The following descriptions (5) to (7) in section 33.18, Event Linking, are deleted.

(5) Receive Data Match Event Output

- Indicates the match the comparison data (SCR4.CMPD[8:0] bits) with receive data that is one frame of data has been received, when SCR0.DCME bit is set to 1 in asynchronous mode (including multi-processor mode).

(6) Receive Data Unmatch Event Output

- Indicates the unmatch the comparison data (SCR4.CMPD[8:0] bits) with receive data that is one frame of data has been received, when SCR0.DCME bit is set to 1 in asynchronous mode (including multi-processor mode).

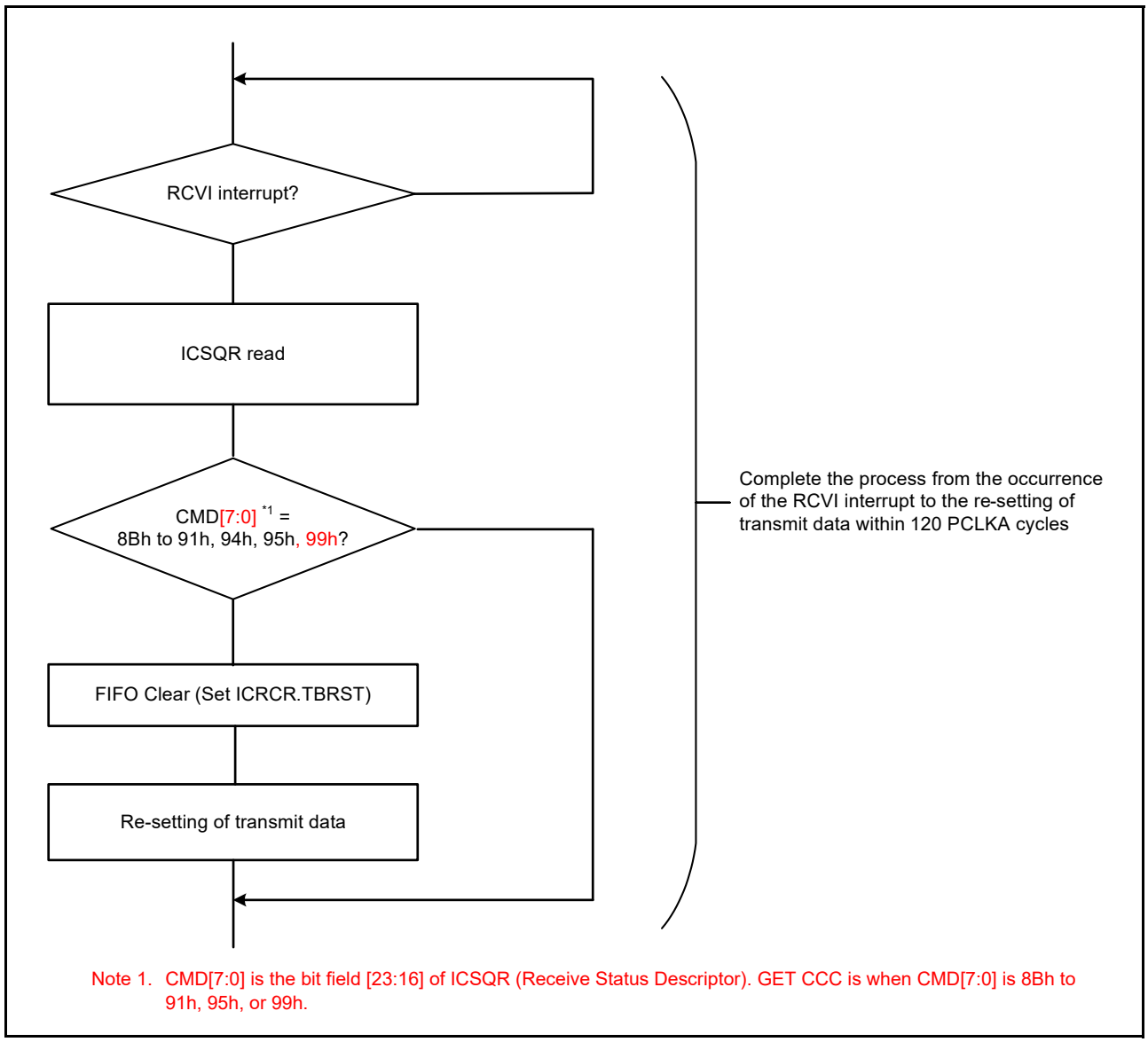
(7) Active Edge Detection Event Output

- In extended serial mode, when XCR1.BRME bit is 1, it indicates that a valid edge has been detected in the RXD input signal.

• Page 2015 of 2908

Figure 35.48 in section 35.4.6.5, I3C Target Transmission Flow (FIFO Buffer Transfer), is corrected as follows.

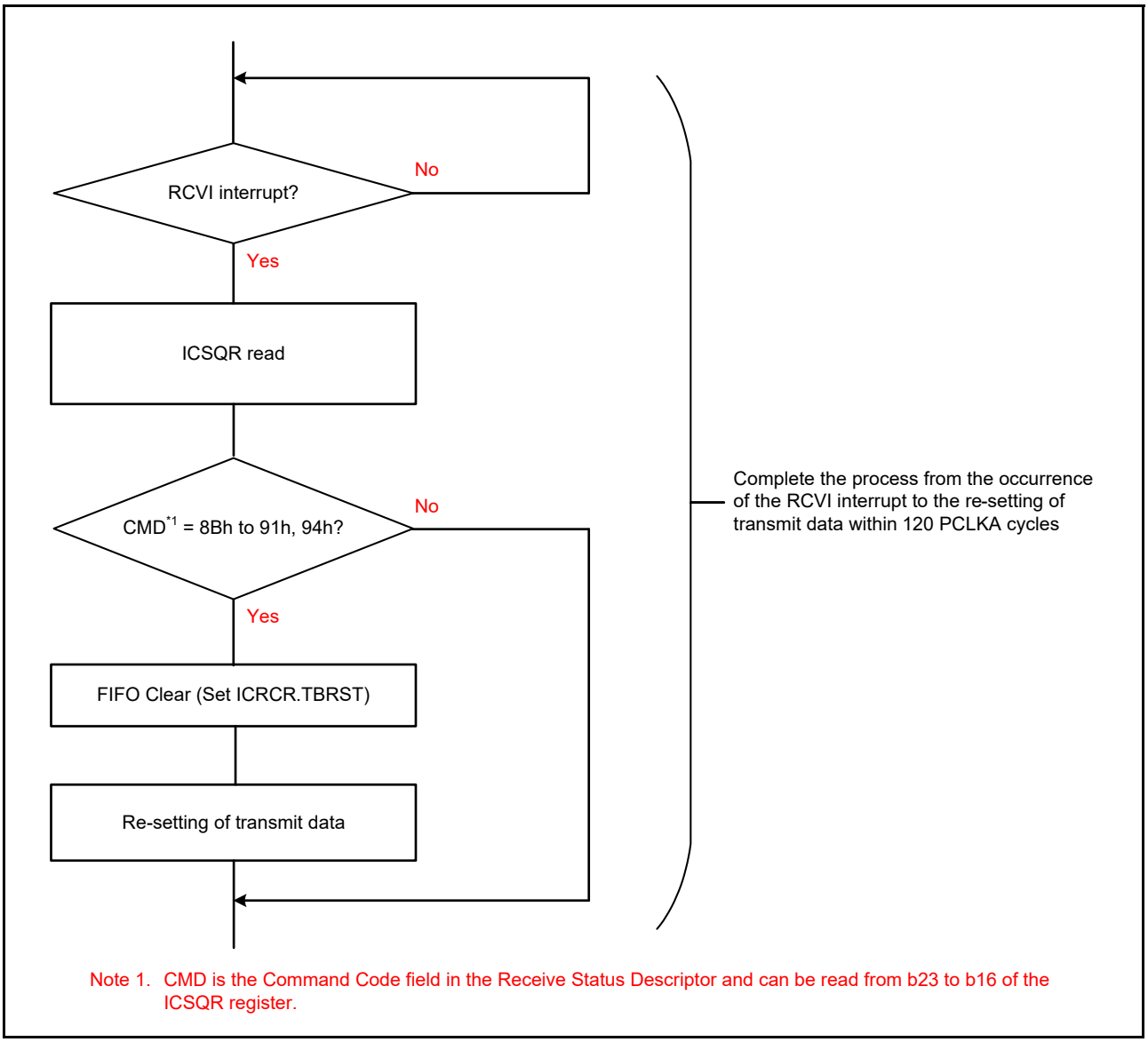
Before correction



Note 1. CMD[7:0] is the bit field [23:16] of ICSQR (Receive Status Descriptor). GET CCC is when CMD[7:0] is 8Bh to 91h, 95h, or 99h.

Figure 35.48 I3C Target Receives GET CCC Command while Data Exists by Writing from the ICDR Register to the Transmit Buffer

After correction



Note 1. CMD is the Command Code field in the Receive Status Descriptor and can be read from b23 to b16 of the ICSQR register.

Figure 35.48 I3C Target Receives GET CCC Command while Data Exists by Writing from the ICDR Register to the Transmit Buffer