Date: Apr. 18, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A0265A/E	Rev.	1.00
Title	Errata to the RX23W Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX23W Group	Lot No. All	Reference Document	RX23W Group User's Manual: Hardware Rev.1.10 (R01UH0823EJ0110)		

This document describes corrections to the DC characteristics for P30, P31, and PB5 in the RX23W Group User's Manual: Hardware, Rev.1.10.

- Page 53 of 1852

Number of the 5-V tolerant pins in Table 1.1, Outline of Specifications (2/5) is corrected as follows.

Before correction

Table 1.1 Outline of Specifications (2/5)

Classification	Module/Function	Description
		(Omitted)
I/O ports	General I/O ports	85-pin/83-pin/56-pin I/O: 43/43/29 • Input: 1/1/1 Pull-up resistors: 43/43/29 • Open-drain outputs: 31/31/24 • 5-V tolerance: 5/5/4
		(Omitted)

After correction

Table 1.1 Outline of Specifications (2/5)

Classification	Module/Function	Description
		(Omitted)
I/O ports	General I/O ports	85-pin/83-pin/56-pin • I/O:43/43/29 • Input: 1/1/1 • Pull-up resistors: 43/43/29 • Open-drain outputs: 58/34/26 • 5-V tolerance: 3/3/2
		(Omitted)

• Page 439 of 1852

Functions of P30 and P31 in Table 21.2, Port Functions are corrected as follows.

Before correction

Table 21.2 Port Functions

Port	Pin	Input Pull-up	Open Drain Output	Drive Capacity Switching	5-V Tolerant
(Omitted)					
PORT3	P30, P31	✓	✓	✓	✓
(Omitted)					

After correction

Table 21.2 Port Functions

Port	Pin	Input Pull-up	Open Drain Output	Drive Capacity Switching	5-V Tolerant
(Omitted)					
PORT3	P30, P31	✓	✓	✓	—
(Omitted)					

• Page 1761 of 1852

Description of Note 1 in Table 51.1, Absolute Maximum Ratings is corrected and Note 2 is added as follows.

Before correction

Table 51.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VSS_USB = VSS_RF = 0 V

Item		Symbol	Value	Unit
(Omitted)				
Input voltage	Ports for 5 V tolerant*1	V_{in}	–0.3 to +6.5	V
	P03, P05, P07, P40 to P47		–0.3 to AVCC0 + 0.3	
	ANT		–1.0 to +1.4	
	XTAL1_RF, XTAL2_RF		–0.3 to +1.4	
	DCLIN_A, DCLIN_D		–0.3 to +2.2	
	Ports other than above		–0.3 to VCC + 0.3	
(Omitted)				

Note 1. Ports 16, 17, 30, 31, and B5 are 5 V tolerant.

After correction

Table 51.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VREFL = VSS_USB = 0 V

Item		Symbol	Value	Unit
(Omitted)				
Input voltage	Ports for 5 V tolerant*1	V_{in}	–0.3 to +6.5	V
	P03, P05, P07, P40 to P47		–0.3 to AVCC0 + 0.3	
	ANT		–1.0 to +1.4	
	XTAL1_RF, XTAL2_RF		–0.3 to +1.4	
	DCLIN_A, DCLIN_D		–0.3 to +2.2	
	Ports other than above*2		–0.3 to VCC + 0.3	
(Omitted)				

Note 1. P16, P17, and PB5 are 5 V tolerant.
Note 2. When the VBATT power supply is selected, P30 and P31 are rated from –0.3 V to VBATT + 0.3 V.

• Page 1763 of 1852

ΔV_T of P30 and P31 is added to Table 51.3, DC Characteristics (1) and the PB5 is corrected as follows; and the expression "other than RIIC input pin" is changed to specific pin names.

Before correction

Table 51.3 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB = VCC_RF = AVCC_RF ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V,
VSS = AVSS0 = VSS_USB = VSS_RF= 0 V, Ta = –40 to +85°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)		V_{IH}	VCC × 0.7	—	5.8	V	
	Ports 16, 17, port B5 (5 V tolerant)			VCC × 0.8	—	5.8		
	Ports 14, 15, ports 21, 22, 25 to 27, ports 35 to 37, ports B0, B1, B3, B5, B7 ports C0, C2 to C7, ports D3, ports E0 to E4, port J3, Ports 30, 31 (when time capture event input is not selected), RES#			VCC × 0.8	—	VCC + 0.3		
	Ports 03, 05, 07, ports 40 to 47			AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports 30, 31 (when time capture event input is selected)	When VCC is supplied		VCC × 0.8	—	VCC + 0.3		
		When VBATT is supplied		VBATT × 0.8	—	VBATT + 0.3		
	Ports 03, 05, 07, ports 40 to 47		V_{IL}	–0.3	—	AVCC0 × 0.2		
	RIIC input pin (except for SMBus)			–0.3	—	VCC × 0.3		
	Other than RIIC input pin or ports 30, 31			–0.3	—	VCC × 0.2		
	Ports 30, 31 (when time capture event input is selected)	When VCC is supplied		–0.3	—	VCC × 0.3		
		When VBATT is supplied		–0.3	—	VBATT × 0.3		
	Ports 03, 05, 07, ports 40 to 47		ΔV_T	AVCC0 × 0.1	—	—		
	RIIC input pin (except for SMBus)			VCC × 0.05	—	—		
	Ports 12, 13, 16, 17, Port B5			VCC × 0.05	—	—		
	Other than RIIC input pin			VCC × 0.1	—	—		

(Omitted)

After correction

Table 51.3 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB = VCC_RF = AVCC_RF ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V,
VSS = AVSS0 = VSS_USB = VSS_RF= 0 V, Ta = –40 to +85°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)		V_{IH}	VCC × 0.7	—	5.8	V	
	P16, P17, PB5 (5 V tolerant)			VCC × 0.8	—	5.8		
	P14, P15, P21, P22, P25 to P27, P35 to P37, PB0, PB1, PB3, PB7, PC0, PC2 to PC7, PD3, PE0 to PE4, PJ3, P30, P31 (other than RTCICn pin), RES#			VCC × 0.8	—	VCC + 0.3		
	P03, P05, P07, P40 to P47			AVCC0 × 0.8	—	AVCC0 + 0.3		
	P30, P31 (RTCICn pin)	When VCC is supplied		VCC × 0.8	—	VCC + 0.3		
		When VBATT is supplied		VBATT × 0.8	—	VBATT + 0.3		
	RIIC input pin (except for SMBus)		V_{IL}	–0.3	—	VCC × 0.3		
	P14 to P17, P21, P22, P25 to P27, P35 to P37, PB0, PB1, PB3, PB5, PB7, PC0, PC2 to PC7, PD3, PE0 to PE4, PJ3, P30, P31 (other than RTCICn pin), RES#			–0.3	—	VCC × 0.2		
	P03, P05, P07, P40 to P47			–0.3	—	AVCC0 × 0.2		
	P30, P31 (RTCICn pin)	When VCC is supplied		–0.3	—	VCC × 0.3		
		When VBATT is supplied		–0.3	—	VBATT × 0.3		
	RIIC input pin (except for SMBus), P16, P17, PB5		ΔV_T	VCC × 0.05	—	—		
	P14, P15, P21, P22, P25 to P27, P35 to P37, PB0, PB1, PB3, PB7, PC0, PC2 to PC7, PD3, PE0 to PE4, PJ3, P30, P31 (other than RTCICn pin), RES#			VCC × 0.1	—	—		
	P03, P05, P07, P40 to P47			AVCC0 × 0.1	—	—		
(Omitted)								

• Page 1764 of 1852

Characteristics of P30 and P31 are added to Table 51.4, DC Characteristics (2) and PB5 is corrected as follows; and the expression “Ports other than above” is changed to specific pin names.

Before correction

Table 51.4 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = VCC_RF = AVCC_RF ≤ 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V,
VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, Ta = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports 16, 17, port B5 (5 V tolerant)	V_{IH}	VCC × 0.8	—	5.8	V	
	Ports 14, 15, ports 21, 22, 25 to 27, ports 30, 31, 35 to 37, ports B0, B1, B3, B5, B7, ports C0, C2 to C7, ports D3, ports E0 to E4, port J3, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports 03, 05, 07, ports 40 to 47		AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports 03, 05, 07, ports 40 to 47	V_{IL}	–0.3	—	AVCC0 × 0.2		
	Ports other than above		–0.3	—	VCC × 0.2		
	Ports 03, 05, 07, ports 40 to 47	ΔV_T	AVCC0 × 0.01	—	—		
	Ports other than above		VCC × 0.01	—	—		

(Omitted)

After correction

Table 51.4 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = VCC_RF = AVCC_RF < 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V,
VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, Ta = –40 to +85°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	P16, P17, PB5 (5 V tolerant)		V_{IH}	VCC × 0.8	—	5.8	V	
	P14, P15, P21, P22, P25 to P27, P35 to P37, PB0, PB1, PB3, PB7, PC0, PC2 to PC7, PD3, PE0 to PE4, PJ3, P30, P31 (other than RTCICn pin), RES#			VCC × 0.8	—	VCC + 0.3		
	P03, P05, P07, P40 to P47			AVCC0 × 0.8	—	AVCC0 + 0.3		
	P30, P31 (RTCICn pin)	When VCC is supplied		VCC × 0.8	—	VCC + 0.3		
		When VBATT is supplied		VBATT × 0.8	—	VBATT + 0.3		
	P14 to P17, P21, P22, P25 to P27, P35 to P37, PB0, PB1, PB3, PB5, PB7, PC0, PC2 to PC7, PD3, PE0 to PE4, PJ3, P30, P31 (other than RTCICn pin), RES#		V_{IL}	–0.3	—	VCC × 0.2		
	P03, P05, P07, P40 to P47			–0.3	—	AVCC0 × 0.2		
	P30, P31 (RTCICn pin)	When VCC is supplied		–0.3	—	VCC × 0.2		
		When VBATT is supplied		–0.3	—	VBATT × 0.2		
	P14 to P17, P21, P22, P25 to P27, P35 to P37, PB0, PB1, PB3, PB5, PB7, PC0, PC2 to PC7, PD3, PE0 to PE4, PJ3, P30, P31 (other than RTCICn pin), RES#		ΔV_T	VCC × 0.01	—	—		
	P03, P05, P07, P40 to P47			AVCC0 × 0.01	—	—		
(Omitted)								