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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A137A/E	Rev.	1.00
Title	Errata to RX230 Group, RX231 Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Products	RX230 Group , RX231 Group	Lot No. All	Reference Document	RX230 Group, RX231 Group User's Manual: Hardware Rev.1.00 (R01UH0496EJ0100)		

This document describes additions of electrical characteristics and corrections to the RX230 Group, RX231 Group User's Manual: Hardware Rev.1.00.

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Description for the VBTLVDLVL[1:0] bits in 12.2.1, VBATT Control Register (VBATTCR) is modified as follows:

[Before correction]

VBTLVDLVL[1:0] Bit (VBATT Pin Voltage Drop Detection Level Select)

These bits are used to select the detection voltage level (Vdetvbt) when the voltage drop detection function of the VBATT pin is enabled.

[After correction]

VBTLVDLVL[1:0] (VBATT Pin Voltage Drop Detection Level Select)

These bits are used to select the detection voltage level (Vdetvbt) when the voltage drop detection function of the VBATT pin is enabled.

VBTLVDLVL[1:0] bits are enabled when the VBATTCR.VBATTDIS bit is 0 (battery backup function enabled).

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Description for the VBTLVDMON flag in 12.2.2, VBATT Status Register (VBATTSR) is modified as follows:

[Before correction]

VBTLVDMON Flag (VBATT Pin Voltage Monitor Flag)

This flag indicates whether the VBATT pin voltage is below Vdetvbt.

This flag is enabled only when the battery backup function is enabled (the VBATTCR.VBATTDIS bit is 0).

[After correction]

VBTLVDMON Flag (VBATT Pin Voltage Monitor Flag)

This flag indicates whether the VBATT pin voltage is below Vdetvbt.

This flag is enabled when the VBATTCR.VBATTDIS bit is 0 (battery backup function enabled) and the VBATTCR.VBTLVDEN bit is 1 (VBATT pin voltage drop detection enabled).

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Table 21.6, Unused Pin Configuration is modified as follows:

[Before correction]

Pin Name	Description
omitted	
Ports 0 to 5 Ports A to E, H, J	• If the direction setting is for input (PORTn.PDR = 0), the corresponding pin is connected to VCC (pulled up) via a resistor or to VSS (pulled down) via a resistor.*1 • If the direction setting is for output (PORTn.PDR = 1), the pin is released.*1, *2
VREFH0	Connect this pin to AVCC0
VREFL0	Connect this pin to AVSS0

[After correction]

Pin Name	Description
omitted	
Ports 1 to 3, 5 Ports A to E, H, J	• If the direction setting is for input (PORTn.PDR = 0), the corresponding pin is connected to VCC (pulled up) via a resistor or to VSS (pulled down) via a resistor.*1 • If the direction setting is for output (PORTn.PDR = 1), the pin is released.*1, *2
Ports 0, 4	• If the direction setting is for input (PORTn.PDR = 0), the corresponding pin is connected to AVCC0 (pulled up) via a resistor or to AVSS0 (pulled down) via a resistor.*1 • If the direction setting is for output (PORTn.PDR = 1), the pin is released.*1, *2
VREFH0	Connect this pin to AVCC0
VREFL0	Connect this pin to AVSS0
VREFH	Connect this pin to AVCC0
VREFL	Connect this pin to AVSS0

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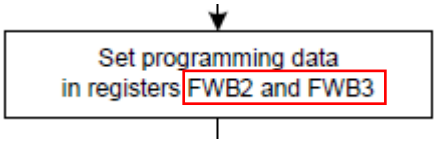
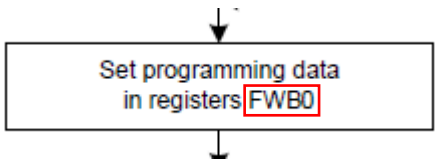
Step 3 in Figure 49.13, Procedure to Issue the Program Command for the E2 DataFlash is modified as follows:

[Before correction]



[After correction]



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Input voltage row in Table 50.1, Absolute Maximum Ratings is modified as follows:

[Before correction]

Item		Symbol	Value	Unit
omitted				
Input voltage	Except for ports for 5 V tolerant*1	V_{in}	-0.3 to VCC+0.3	V
	Ports for 5 V tolerant*1		-0.3 to +6.5	

[After correction]

Item		Symbol	Value	Unit
omitted				
Input voltage	Ports for 5 V tolerant*1	V_{in}	-0.3 to +6.5	V
	Ports 03, 05, 07 Ports 40 to 47		-0.3 to AVCC0+0.3	
	Ports other than above		-0.3 to VCC+0.3	

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ΔV_T row in Table 50.3, DC Characteristics (1) is modified as follows:

[Before correction]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
omitted							
Schmitt trigger input voltage	Ports 03, 05, 07, ports 40 to 47	ΔV_T	AVCC0×0.1	—	—	V	
	RIIC input pin (except for SMBus)		VCC×0.05	—	—		
	Other than RIIC input pin		VCC×0.1	—	—		

[After correction]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
omitted							
Schmitt trigger input voltage	Ports 03, 05, 07, ports 40 to 47	ΔV_T	AVCC0×0.1	—	—	V	
	RIIC input pin (except for SMBus)		VCC×0.05	—	—		
	Ports 12, 13, 16, 17 Ports B5		VCC×0.05	—	—		
	Other than RIIC input pin		VCC×0.1	—	—		

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Units “mA” and “MHz” and value “32” in Figure 50.3, Voltage Dependency in Low-Speed Operating Mode (Reference Data) are corrected as follows:

[Before correction]

ICC(mA)

ICLK = 32MHz

[After correction]

ICC(μA)

ICLK = 32.768kHz

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"Increment for LPT operation" and "Increment for IWDT operation" are added to Table 50.8, DC Characteristics (6) as follows:

[Before change]

Item		Symbol	Typ. *3	Max	Unit	Test Condition
omitted						
Supply Current *1	Increment for RTC operation*4		0.4	—		RCR3.RTCDV[2:0] set to low drive capacity
			1.2	—		RCR3.RTCDV[2:0] set to normal drive capacity

[After change]

Item		Symbol	Typ. *3	Max	Unit	Test Condition
omitted						
Supply Current *1	Increment for LPT operation	I_{CC}	0.4	—	μA	Use IWDT-Dedicated On-Chip Oscillator for clock source
	Increment for IWDT operation		0.4	—		
	Increment for RTC operation*4		0.4	—		RCR3.RTCDV[2:0] set to low drive capacity
			1.2	—		RCR3.RTCDV[2:0] set to normal drive capacity

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Operating current for LVD1, LVD2, and CTSU are added to Table 50.11, DC Characteristics (9) as follows:

[Before change]

Item		Symbol	Min	Typ. *7	Max	Unit	Test Condition
Analog power Supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.7	1.7	mA	
omitted							
Temperature sensor*6	—	I_{TEMP}	—	75	—	μA	
Comparator B operating current*6	Window mode	I_{CMP}	—	12.5	28.6	μA	
	Comparator high-speed mode (per channel)		—	3.2	16.2	μA	
	Comparator low-speed mode (per channel)		—	1.7	4.4	μA	

[After change]

Item		Symbol	Min	Typ. *7	Max	Unit	Test Condition
Analog power Supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.7	1.7	mA	
omitted							
LVD1 and LVD2 operating current*6	Per channel	I_{LVD}	—	0.15	—	μA	
Temperature sensor*6	—	I_{TEMP}	—	75	—	μA	
Comparator B operating current*6	Window mode	I_{CMP}	—	12.5	28.6	μA	
	Comparator high-speed mode (per channel)		—	3.2	16.2	μA	
	Comparator low-speed mode (per channel)		—	1.7	4.4	μA	
CTSU operating current*6	When sleep mode Base clock: 2 MHz Pin capacitance: 50 pF	I_{CTSU}	—	150	—	μA	

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Values in Table 50.16, Permissible Output Currents (1) are corrected as follows:

[Before correction]

Item		Symbol	Max.	Unit
Permissible output low current	Total of ports 40 to 47, ports 03, 05, 07	ΣI_{OL}	25	mA
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3		40	
omitted				
Permissible output high current	Total of ports 40 to 47, ports 03, 05, 07	ΣI_{OH}	-25	mA
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3		-40	

[After correction]

Item		Symbol	Max.	Unit
Permissible output low current	Total of ports 40 to 47, ports 03, 05, 07	ΣI_{OL}	40	mA
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3		40	
omitted				
Permissible output high current	Total of ports 40 to 47, ports 03, 05, 07	ΣI_{OH}	-40	mA
	Total of ports 12 to 17, ports 20 to 27, ports 30 to 37, port PJ3		-40	

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Value in Table 51.17, Output Permissible Currents (2) is corrected as follows:

[Before correction]

Item			Symbol	Max.	Unit
omitted					
Permissible output high current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37		I_{OH}	-0.1	mA
	Ports other than above	Normal output mode		-4.0	
		High-drive output mode		-8.0	

[After correction]

Item			Symbol	Max.	Unit
omitted					
Permissible output high current (maximum value per pin)	Ports 40 to 47, ports 03, 05, 07, ports 36, 37		I_{OH}	-4.0	mA
	Ports other than above	Normal output mode		-4.0	
		High-drive output mode		-8.0	

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Normal output mode row in Table 50.18, Output Values of Voltage (1) is modified as follows:

[Before correction]

Item			Symbol	Min.	Max.	Unit	Test Conditions
omitted							
Output high	All output ports	Normal output mode	V_{OH}	VCC – 0.5	—	V	I_{OH} = -0.5mA
		High-drive output mode		VCC – 0.5	—		I_{OH} = -1.0mA

[After correction]

Item				Symbol	Min.	Max.	Unit	Test Conditions
omitted								
Output high	All output ports	Normal output mode	Ports 03, 05, 07, ports 40 to 47	V_{OH}	AVCC0 – 0.5	—	V	I_{OH} = -0.5mA
			Ports other than above		VCC-0.5	—		
		High-drive output mode			VCC – 0.5	—		I_{OH} = -1.0mA

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Normal output mode row in Table 50.19, Output Values of Voltage (2) is modified as follows:

[Before correction]

Item			Symbol	Min.	Max.	Unit	Test Conditions
omitted							
Output low	RIIC pins	Standard mode	V_{OL}	—	0.4	V	I_{OL} = 3.0mA
		Fast mode		—	0.6		I_{OL} = 6.0mA
Output high	All output ports	Normal output mode	V_{OH}	VCC – 0.8	—	V	I_{OH} = -1.0mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = -2.0mA

After correction]

Item				Symbol	Min.	Max.	Unit	Test Conditions
omitted								
Output low	RIIC pins	Standard mode (Normal output mode)		V_{OL}	—	0.4	V	I_{OL} = 3.0mA
		Fast mode (High-drive output mode)			—	0.6		I_{OL} = 6.0mA
Output high	All output ports	Normal output mode	Ports 03, 05, 07, ports 40 to 47	V_{OH}	AVCC0 – 0.8	—	V	I_{OH} = -1.0mA
			Ports other than above		VCC-0.8	—		
		High-drive output mode			VCC – 0.8	—		I_{OH} = -2.0mA

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Normal output mode row in Table 50.20, Output Values of Voltage (3) is modified as follows:

[Before correction]

Item			Symbol	Min.	Max.	Unit	Test Conditions
omitted							
Output high	All output ports	Normal output mode	V_{OH}	VCC – 0.8	—	V	I_{OH} = -2.0mA
		High-drive output mode		VCC – 0.8	—		I_{OH} = -4.0mA

[After correction]

Item				Symbol	Min.	Max.	Unit	Test Conditions
omitted								
Output high	All output ports	Normal output mode	Ports 03, 05, 07, ports 40 to 47	V_{OH}	AVCC0 – 0.8	—	V	I_{OH} = -2.0mA
			Ports other than above		VCC-0.8	—		
		High-drive output mode			VCC – 0.8	—		I_{OH} = -4.0mA

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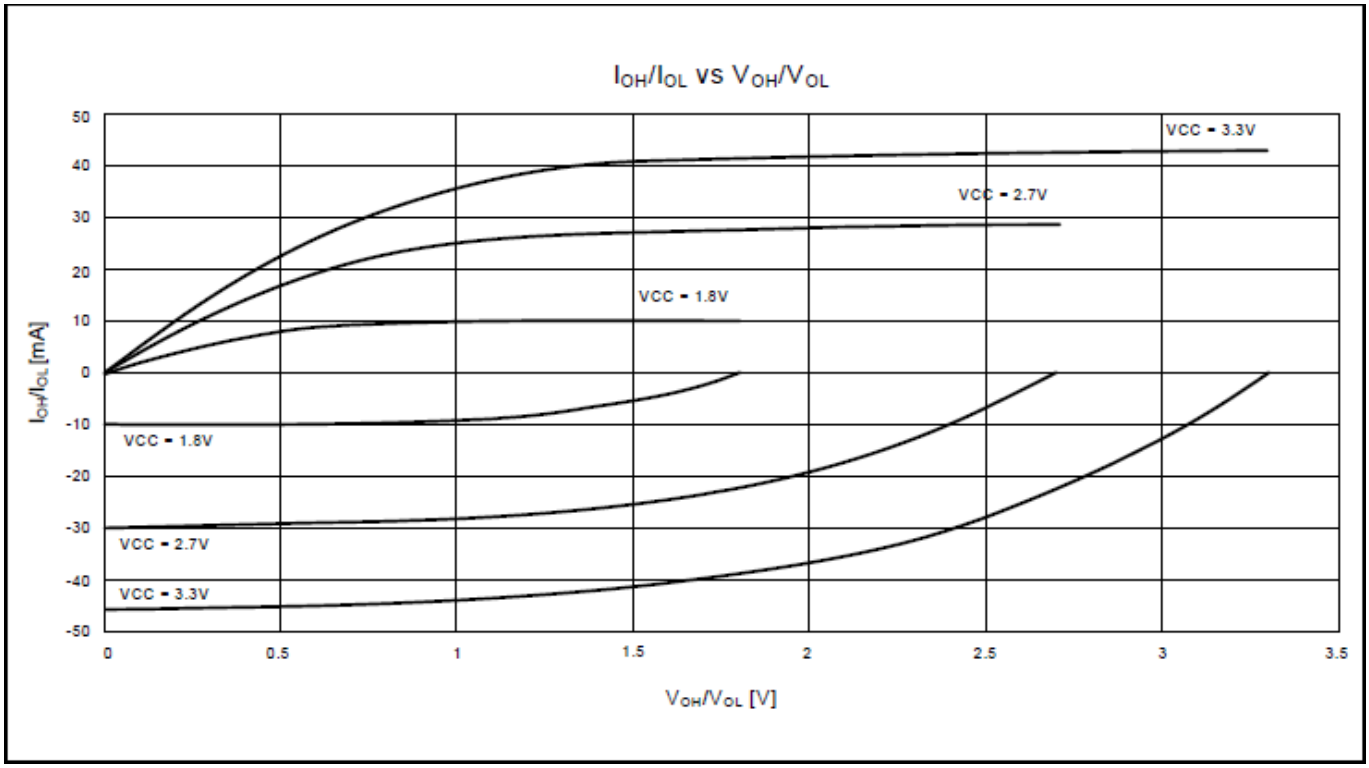
Figure 50.13 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C When High-Drive Output is Selected (Reference Data) is corrected as follows:

[Before correction]



[After correction]

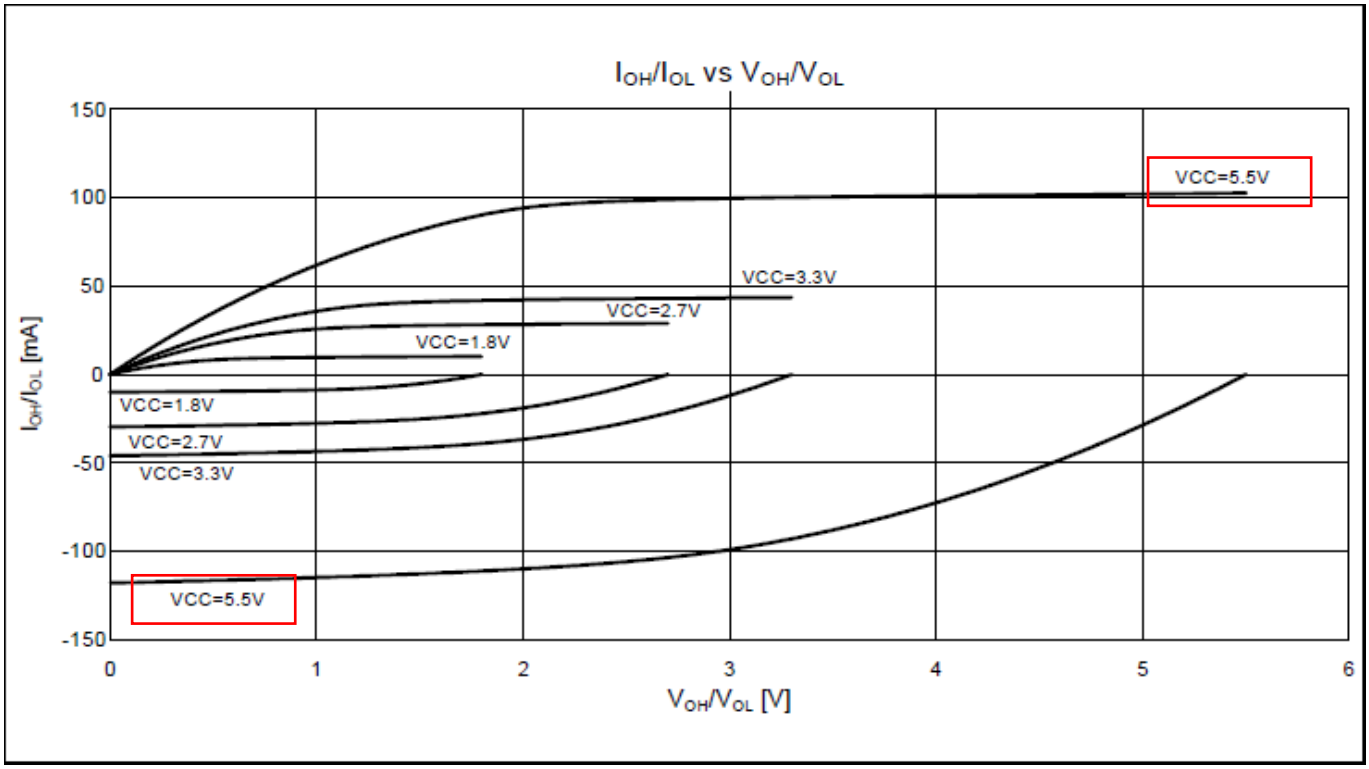


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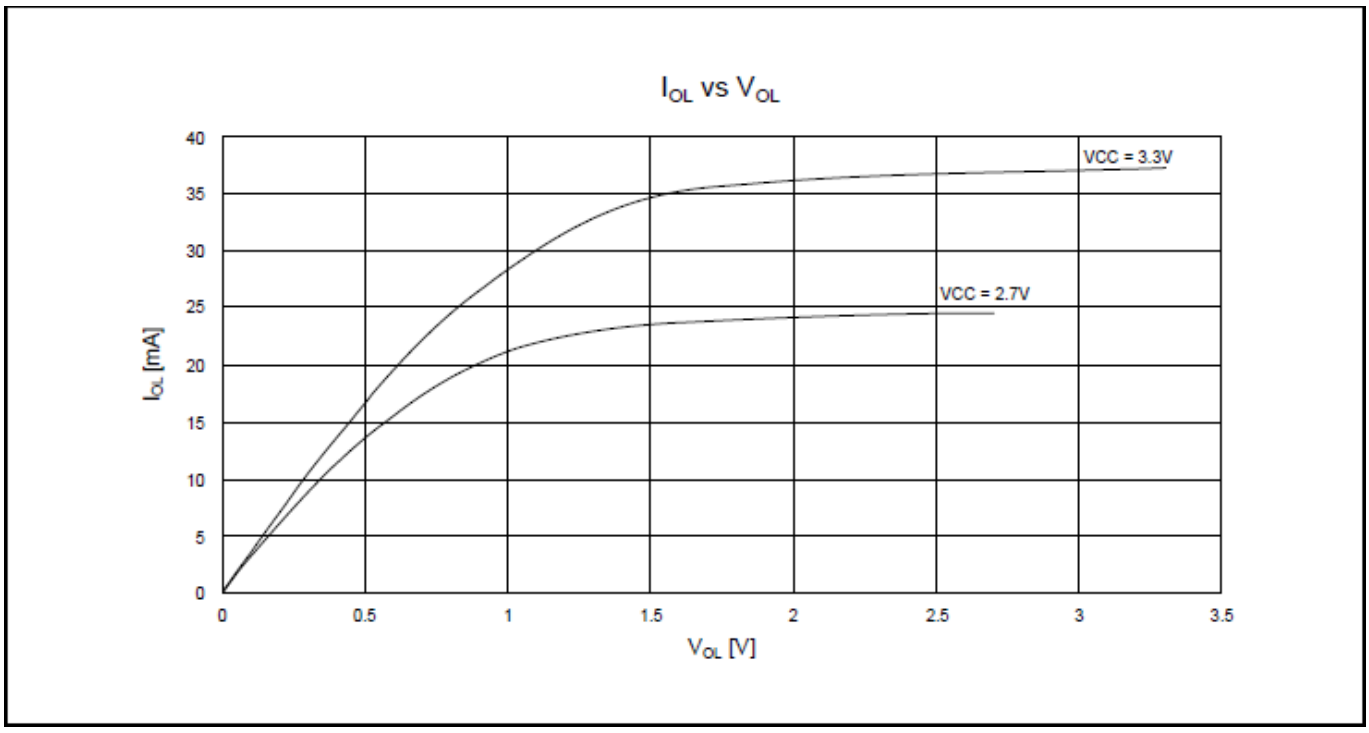
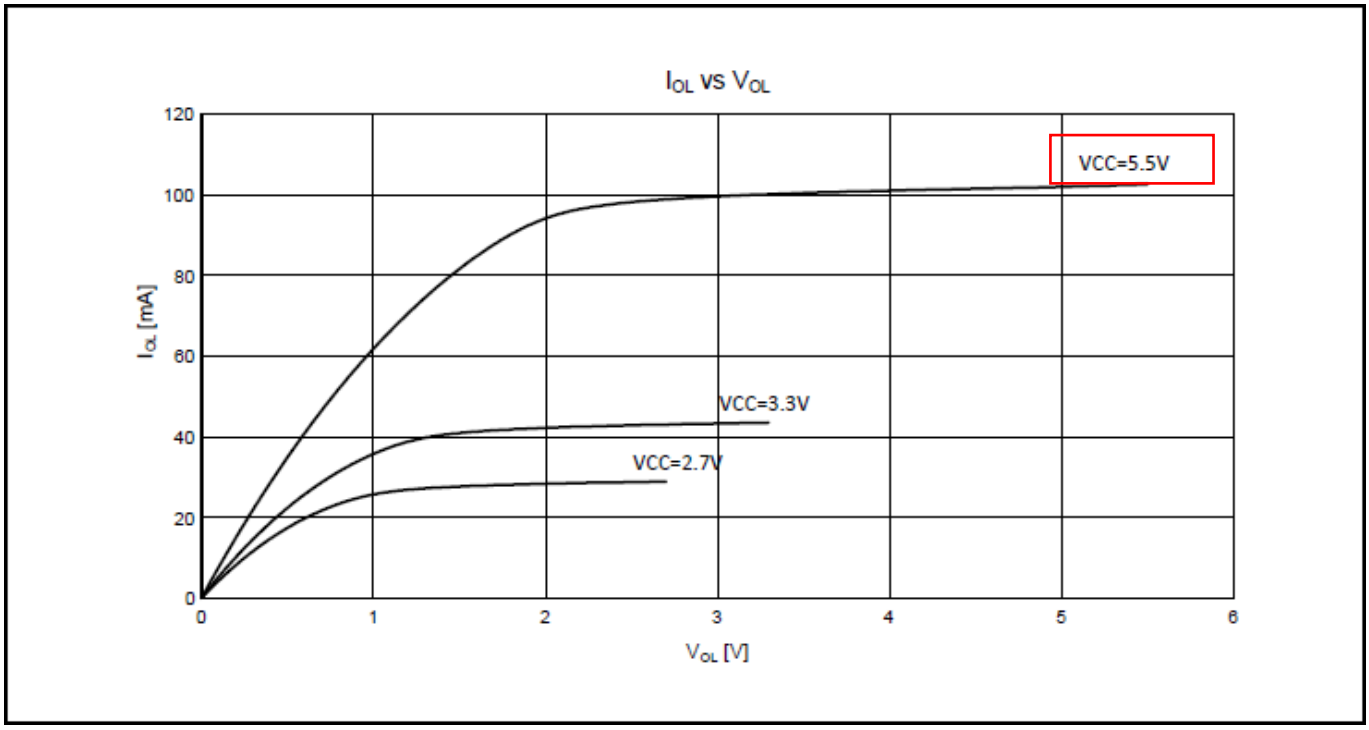
Figure 50.18 VOL and IOL Voltage Characteristics of RIIC Output Pin at Ta = 25°C (Reference Data) is corrected as follows:

[Before correction]



[After correction]



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Note 3 in Table 50.21, Operating Frequency Value (High-Speed Operating Mode) is corrected as follows:

[Before correction]

Note 3. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

[After correction]

Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.

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Note 3 in Table 50.22, Operating Frequency Value (Middle-Speed Operating Mode) is corrected as follows:

[Before correction]

Note 3. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

[After correction]

Note 3. The VCC_USB range is 3.0 to 5.5 V when the USB clock is in use.

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Operating condition in Table 50.26, Clock Timing is corrected as follows:

[Before correction]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
omitted							
Main clock oscillator oscillation frequency*2	2.4≤VCC≤3.6	f_{MAIN}	1	—	20	MHz	
	1.8≤VCC<2.4		1	—	8		

[After correction]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
omitted							
Main clock oscillator oscillation frequency*2	2.4≤VCC≤5.5	f_{MAIN}	1	—	20	MHz	
	1.8≤VCC<2.4		1	—	8		

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Value in Table 50.57, Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1) is corrected, Note 3 is modified, and Note 4 is deleted as follows:

[Before correction]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
omitted							
Voltage detection level	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.84	3.97	V	Figure 50.74 At falling edge VCC
		V_{det0_1}	2.70	2.82	3.00		
		V_{det0_2}	2.37	2.51	2.67		
		V_{det0_3}	1.79	1.90	1.99		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42	V	Figure 50.75 At falling edge VCC
		omitted					
		V_{det1_D}	1.76	1.86	1.96		
	Voltage detection circuit (LVD2)*3	V_{det2_0}	4.08	4.29	4.48	V	Figure 50.76 At falling edge VCC
		V_{det2_1}	3.85	4.14	4.35		
		V_{det2_2}	3.82	4.02	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note 3. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

Note 4. Vdet2_0 selection can be used only when the CMPA2 pin input voltage is selected, and cannot be used when the power supply voltage (VCC) is selected.

[After correction]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
omitted							
Voltage detection level	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.84	3.97	V	Figure 50.74 At falling edge VCC
		V_{det0_1}	2.70	2.82	3.00		
		V_{det0_2}	2.37	2.51	2.67		
		V_{det0_3}	1.80	1.90	1.99		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42	V	Figure 50.75 At falling edge VCC
		omitted					
		V_{det1_D}	1.80	1.86	1.96		
	Voltage detection circuit (LVD2)*3	V_{det2_0}	4.08	4.29	4.48	V	Figure 50.76 At falling edge VCC
		V_{det2_1}	3.95	4.14	4.35		
		V_{det2_2}	3.82	4.02	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note 3. n in the symbol Vdet2_n denotes the value of the LVDLVLR.LVD2LVL[1:0] bits.

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Dimensions in Figure B, 100-Pin LQFP (PLQP0100KB-B) are modified as follows:

[Before correction]

Reference Symbol	Dimension in Millimeters		
	Min	Norm	Max
D	—	14.0	—
omitted			
A	—	—	1.6
omitted			
θ	0°	3.5°	7°

[After correction]

Reference Symbol	Dimension in Millimeters		
	Min	Norm	Max
D	—	14.0	—
omitted			
A	—	—	1.7
omitted			
θ	0°	3.5°	8°

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Dimensions in Figure E, 64-pin LQFP (PLQP0064KB-C) are modified as follows:

[Before correction]

Reference Symbol	Dimension in Millimeters		
	Min	Norm	Max
D	—	10.0	—
omitted			
A	—	—	1.6
omitted			
θ	0°	3.5°	7°

[After correction]

Reference Symbol	Dimension in Millimeters		
	Min	Norm	Max
D	—	10.0	—
omitted			
A	—	—	1.7
omitted			
θ	0°	3.5°	8°

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Dimensions in Figure G, 48-pin LQFP (PLQP0048KB-B) are modified as follows:

[Before correction]

Reference Symbol	Dimension in Millimeters		
	Min	Norm	Max
D	—	7.0	—
omitted			
A	—	—	1.6
omitted			
θ	0°	3.5°	7°

[After correction]

Reference Symbol	Dimension in Millimeters		
	Min	Norm	Max
D	—	7.0	—
omitted			
A	—	—	1.7
omitted			
θ	0°	3.5°	8°