Date: Aug. 3, 2017

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A179A/E	Rev.	1.00
Title	Errata to RX130 Group User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RX130 Group	Lot No. All	Reference Document	RX130 Group User's Manual: Hardware Rev.1.00 (R01UH0560EJ0100)		

This document describes corrections to the RX130 Group User's Manual: Hardware, Rev.1.00.

• Page 103 to 104 of 1316

The access size for the open drain control registers in Table 5.1, List of I/O Registers (Address Order) is corrected as follows.

Before correction

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	Reference Section
Omitted							
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB	section 18
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	section 18
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	section 18
Omitted							

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After correction

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	Reference Section
			Omitted				
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB	section 18
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB	section 18
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB	section 18
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB	section 18
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB	section 18
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB	section 18
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB	section 18
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB	section 18
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB	section 18
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8	2 or 3 PCLKB	section 18
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB	section 18
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8	2 or 3 PCLKB	section 18
			Omitted				

• Page 1118 of 1316

The following note is added between section 32.8.7, Notes on Canceling Software Standby Mode and section 32.8.8, Error in Absolute Accuracy When Disconnection Detection Assistance is in Use.

After correction

32.8.8 Pin Setting when the 12-bit A/D Converter is Used

When the 12-bit A/D converter is used, do not set any pin of port 4 as output. Output from any of the pins may affect on A/D conversion accuracy because analog power supply is used in the part of the port 4 circuit.

• Page 1119 of 1316

The second note in section 32.8.9, ADHSC Bit Rewriting Procedure is deleted as follows.

Before correction

ADHSC Bit Rewriting Procedure:

1. Set the sleep bit (ADHVREFCNT.ADSLP) to 1.
2. Wait for at least 0.2 µs, and then modify the A/D conversion select bit (ADCSR.ADHSC).
3. Wait for at least 4.8 µs, and then clear the sleep bit (ADHVREFCNT.ADSLP) to 0.

Note: It is prohibited to set the ADHVREFCNT.ADSLP bit to 1 except for modifying the A/D conversion select bit (ADCSR.ADHSC).

Note: Do not reset the sleep bit (ADHVREFCNT.ADSLP) while the A/D conversion select bit (ADCSR.ADHSC) is 1. After the A/D conversion select bit (ADCSR.ADHSC) is cleared to 0 or the operating mode is transitioned to module stop mode, reset the sleep bit according to the ADHVREFCNT.ADSLP bit rewriting procedure.

After correction

ADHSC Bit Rewriting Procedure:

1. Set the sleep bit (ADHVREFCNT.ADSLP) to 1.
2. Wait for at least 0.2 µs, and then modify the A/D conversion select bit (ADCSR.ADHSC).
3. Wait for at least 4.8 µs, and then clear the sleep bit (ADHVREFCNT.ADSLP) to 0.

Note: It is prohibited to set the ADHVREFCNT.ADSLP bit to 1 except for modifying the A/D conversion select bit (ADCSR.ADHSC).

• Page 1273 of 1316

Table 39.32, Timing of On-Chip Peripheral Modules (2) is corrected as follows.

Before correction

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 39.45
		Slave		8	4096		
(Omitted)							

After correction

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 39.45
		Slave		8	—		
(Omitted)							

• Page 1274of 1316

Table 39.33, Timing of On-Chip Peripheral Modules (3) is corrected as follows.

Before correction

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 39.45
	SCK clock cycle input (slave)		6	65536	t_{Pcyc}	
(Omitted)						

After correction

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 39.45
	SCK clock cycle input (slave)		6	—	t_{Pcyc}	
(Omitted)						