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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-RX*-A070A/E	Rev.	1.00
Title	Errata to RX Family User's Manuals Regarding the RIIC Module		Information Category	Technical Notification		
Applicable Product	RX610 Group, RX62N Group, RX621 Group, RX62G Group, RX62T Group, RX630 Group, RX63N Group, RX631 Group, RX63T Group, RX210 Group, RX220 Group, RX21A Group	Lot No. All	Reference Document	User's Manual: Hardware for applicable products (see the table at the last page)		

This document describes corrections and additions to the "I²C Bus Interface (RIIC)" chapter in User's Manual: Hardware for the applicable products.
Page and section numbers are based on the RX630 Group. Refer to the table on the last page for the corresponding page and section numbers in the other groups.

•Page of 1150 of 1654

Names and Descriptions of bits ICCR1.SDAI, SCLI, SDAO, SCLO, and SOWP are changed, and explanation of bits SDAO and SCLO is added as follows:

Before change

Bit	Symbol	Bit Name	Description	R/W
b0	SDAI	SDA Bus Input Monitor	0: SDAn pin input is at a low level. 1: SDAn pin input is at a high level.	R
b1	SCLI	SCL Bus Input Monitor	0: SCLn pin input is at a low level. 1: SCLn pin input is at a high level.	R
b2	SDAO	SDA Output Control	• Read: 0: SDAn pin output is at a low level. 1: SDAn pin is in a high-impedance state. • Write: 0: Changes the SDAn pin output to a low level. 1: Changes the SDAn pin in a high-impedance state. (High level output is achieved through an external pull-up resistor.)	R/W *1,*2
b3	SCLO	SCL Output Control	• Read: 0: SCLn pin output is at a low level. 1: SCLn pin is in a high-impedance state. • Write: 0: Changes the SCLn pin output to a low level. 1: Changes the SCLn pin in a high-impedance state. (High level output is achieved through an external pull-up resistor.)	R/W *1,*2
b4	SOWP	SCLO/SDAO Write Protect	0: Allows the SCLO and SDAO bits to be rewritten. (This bit is read as 1.)	R/W*2

Note 1. Do not write to these bits during communication. Changing a value during communication may cause a transmission or reception failure or an AL error.
Note 2. To change the SDAO and SCLO bits, set the SOWP bit to 0 at the same timing to set the SDAO and SCLO bits to 0.

After change

Bit	Symbol	Bit Name	Description	R/W
b0	SDAI	SDA Line Monitor	0: SDAn line is low. 1: SDAn line is high.	R
b1	SCLI	SCL Line Monitor	0: SCLn line is low. 1: SCLn line is high.	R
b2	SDAO	SDA Output Control/Monitor	• Read: 0: The RIIC has driven the SDAn pin low. 1: The RIIC has released the SDAn pin. • Write: 0: The RIIC drives the SDAn pin low. 1: The RIIC releases the SDAn pin.	R/W
b3	SCLO	SCL Output Control/Monitor	• Read: 0: The RIIC has driven the SCLn pin low. 1: The RIIC has released the SCLn pin. • Write: 0: The RIIC drives the SCLn pin low. 1: The RIIC releases the SCLn pin.	R/W
b4	SOWP	SCLO/SDAO Write Protect	0: Bits SCLO and SDAO can be written. 1: Bits SCLO and SDAO are protected. (This bit is read as 1.)	R/W

SDAO Bit (SDA Output Control/Monitor) and SCLO Bit (SCL Output Control/Monitor)

These bits are used to directly control the SDAn and SCLn signals output from the RIIC.
When writing to these bits, also write 0 to the SOWP bit.
The result of setting these bits is input to the RIIC via the input buffer. When slave mode is selected, a START condition may be detected and the bus may be released depending on the bit settings.
Do not rewrite these bits during a START condition, STOP condition, repeated START condition, or during transmission or reception. Operation after rewriting under the above conditions is not guaranteed.
When reading these bits, the state of signals output from the RIIC can be read.

•Page of 1181 of 1654

The following figure is added to 33.3.4 “Master Receive Operation.”

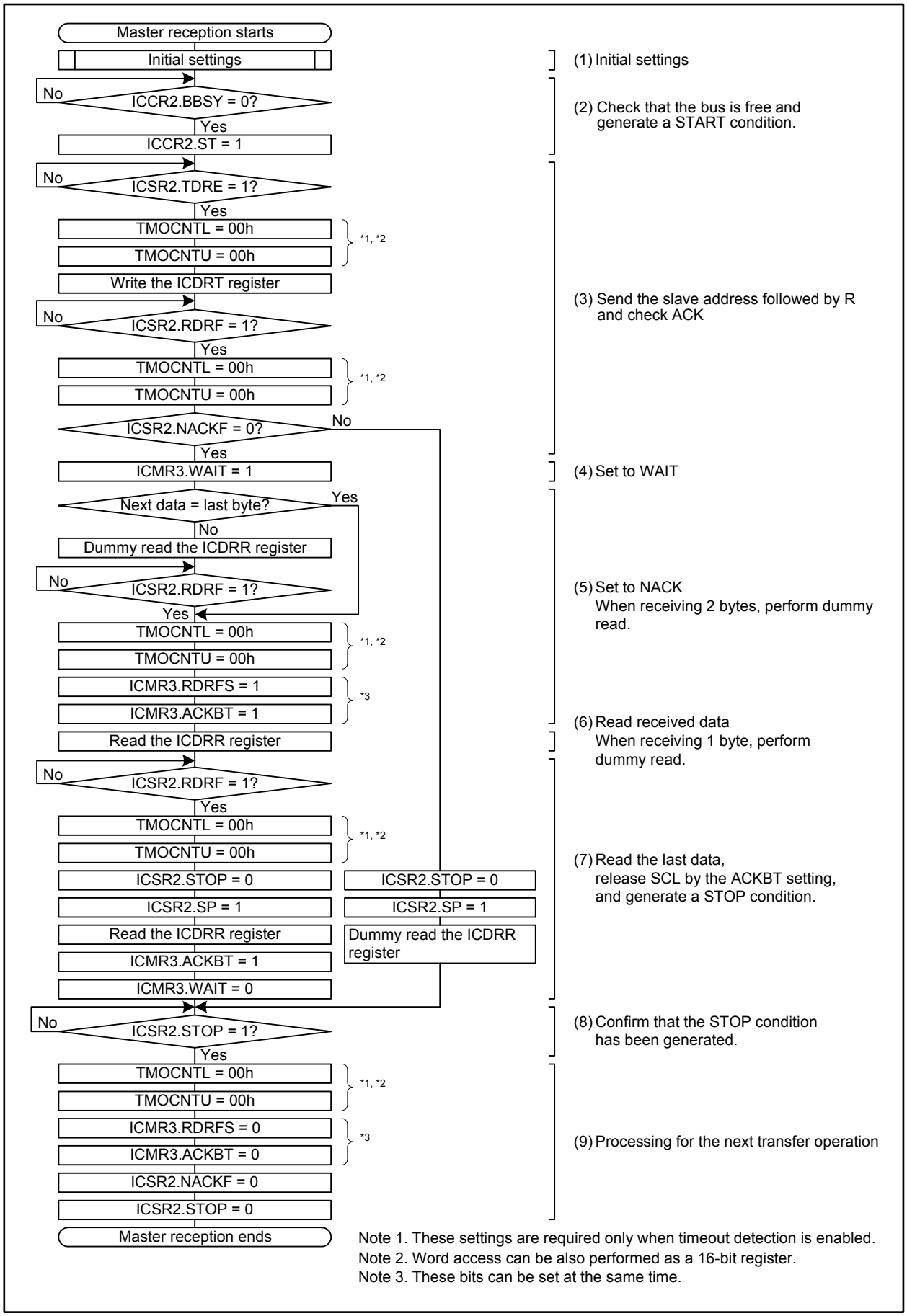

Figure 33.XX Example of Master Reception (7-Bit Address Format, 1 or 2 bytes)

•Page of 1183 of 1654

The title of Figure 33.10 is corrected as follows:

Before change

Figure 33.10 Example of Master Reception Flowchart (7-Bit Address Format)

After change

Figure 33.10 Example of Master Reception (7-Bit Address Format, 3 Bytes or More)

•Page of 1207 of 1654

The first paragraph of 33.11.1 is corrected as follows (“timeout function” is replaced with “timeout detection function” in Before change for RX610, RX62n, and RX621):

Before change

The RIIC has the timeout function to detect an abnormality that the SCLn line is held for a certain period of time. In the bus busy state, the RIIC can detect an abnormal bus state by monitoring that the SCLn line is held low or high for a predetermined time.

After change

The RIIC includes a timeout function for detecting when the SCLn line has been stuck longer than the predetermined time. The RIIC can detect an abnormal bus state by monitoring that the SCLn line is stuck low or high for a predetermined time.

•Page of 1207 of 1654

The third paragraph of 33.11.1 is corrected as follows (“timeout function” is replaced with “timeout detection function” in Before change for RX610, RX62n, and RX621):

Before change

This timeout function is enabled when the TMOE bit in ICFER is 1. It detects an abnormal bus state that the SCLn line is held low or high when the bus is busy (BBSY flag = 1 in ICCR2) in master mode or when the BBSY flag is 1 and the RIIC’s own slave address matches (ICSR1 is not 00h) in slave mode.

After change

This timeout function is enabled when the ICFER.TMOE bit is 1. It detects an abnormal bus state that the SCLn line is stuck low or high during the following conditions:

- The bus is busy (ICCR2.BBSY flag is 1) in master mode (ICCR2.MST bit is 1).
- The RIIC’s own slave address is detected (ICSR1 register is not 00h) and the bus is busy (ICCR2.BBSY flag is 1) in slave mode (ICCR2.MST bit is 0).
- The bus is free (ICCR2.BBSY flag is 0) while generation of a START condition is requested (ICCR2.ST bit is 1).

Reference Documents

Applicable Product	Manual Title (Document Number)	Page number, Section/Figure number			
		ICCR1	Reception flow	Figure title	Timeout
RX610 Group	RX610 Group User's Manual: Hardware Rev.1.20 (R01UH0032EJ0120)	Page 692 22.2.1	Page 733 22.3.4	Page 735 Figure 22.10	Page 763 22.11.1
RX62N Group, RX621 Group	RX62N Group, RX621 Group User's Manual: Hardware Rev.1.30 (R01UH0033EJ0130)	Page 1483 31.2.1	Page 1521 31.3.4	Page 1523 Figure 31.10	Page 1552 31.11.1
RX62G Group	RX62G Group User's Manual: Hardware Rev.1.00 (R01UH0321EJ0100)	Page 910 24.2.1	Page 948 24.3.4	Page 950 Figure 24.10	Page 978 24.11.1
RX62T Group	RX62T Group User's Manual: Hardware Rev.1.30 (R01UH0034EJ0130)	Page 955 24.2.1	Page 993 24.3.4	Page 995 Figure 24.10	Page 1023 24.11.1
RX630 Group	RX630 Group User's Manual: Hardware Rev.1.50 (R01UH0040EJ0150)	Page 1150 33.2.1	Page 1181 33.3.4	Page 1183 Figure 33.10	Page 1207 33.11.1
RX63N Group, RX631 Group	RX63N Group, RX631 Group User's Manual: Hardware Rev.1.60 (R01UH0041EJ0160)	Page 1414 36.2.1	Page 1445 36.3.4	Page 1447 Figure 36.10	Page 1471 30.11.1
RX63T Group	RX63T Group User's Manual: Hardware Rev.2.00 (R01UH0238EJ0 200)	Page 1232 30.2.1	Page 1264 36.3.4	Page 1266 Figure 30.10	Page 1291 30.11.1
RX210 Group	RX210 Group User's Manual: Hardware Rev.1.40 (R01UH0037EJ0140)	Page 1090 30.2.1	Page 1126 30.3.4	Page 1128 Figure 30.10	Page 1155 30.11.1
RX220 Group	RX220 Group User's Manual: Hardware Rev.1.00 (R01UH0292EJ0100)	Page 852 29.2.1	Page 888 29.3.4	Page 890 Figure 29.10	Page 917 29.11.1
RX21A Group	RX21A Group User's Manual: Hardware Rev.1.00 (R01UH0251EJ0100)	Page 903 31.2.1	Page 939 31.3.4	Page 941 Figure 31.10	Page 968 31.11.1