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RENESAS TECHNICAL UPDATE

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Product Category	SOC		Document No.	TN-RE*-A0002A/E	Rev.	1.00
Title	Errata to RE01Group User's Manual:Hardware		Information Category	Technical Notification		
Applicable Product	RE01 Products with 256-Kbyte Flash Memory	Lot No. All	Reference Document	RE01 Group User's Manual:Hardware Rev.1.00 (R01UH0894EJ0100)		

This document describes corrections to the RE01 Group User's Manual: Hardware, Rev.1.00.

The corrections are indicated in red.

No	Chapter	Title	Content
1	1	Overview	Table1.7 Pin list is modified.
2	9	Clock Generation Circuit	9.2.15 Sub-Clock Oscillator Mode Control Register (SOMCR) SOMCR.SODRV bits is modified.
3	Appendix 1	Connecting the Capacitors to the Power Supply Pins	Figure 1.3 Energy harvesting startup mode with the VREF in use and Figure 1.4 Energy harvesting startup mode with AVCC0 as the reference voltage in 1.2 Example of Connections in Energy Harvesting Startup Mode (1) are capacitance value of the smoothing capacitor is corrected.

The corrections are indicated in red in the following description.

1 1.7 Pin Lists

Page 63 of 1343

Table1.15 Pin list will be modified as follows.

Before modified

15	L7	E2	8	8	VCL							
16	M8	F3	9	9	CLKOUT32K_A	P411	AGTWEE1_A/ GTIOC0B_B	TXD9_A/ SCK3_A		IRQ0_A_DS		IOVCC
17	K9	C1	—	—		P410				IRQ9_A		IOVCC
18	K8	—	—	—	CLKOUT32K_B	P409				IRQ9_B		IOVCC
19	M9	D2	10	10	EHMD							IOVCC
20	L9	C2	11	11	VBN							
21	L8	B1	12	12	VBP							
22	L10	E3	13	13		P207	AGTWO1_A/ GTIOC0A_B	RXD9_A/ CTS3_A		IRQ1_A_DS		IOVCC
23	M10	D3	14	14	RES#							IOVCC

After modified

15	L7	E2	8	8	VCL							
16	M8	F3	9	9	CLKOUT32K_A/ SWCLK	P411	AGTWEE1_A/ GTIOC0B_B	TXD9_A/ SCK3_A		IRQ0_A_DS		IOVCC
17	K9	C1	—	—		P410				IRQ9_A		IOVCC
18	K8	—	—	—	CLKOUT32K_B	P409				IRQ9_B		IOVCC
19	M9	D2	10	10	EHMD							IOVCC
20	L9	C2	11	11	VBN							
21	L8	B1	12	12	VBP							
22	L10	E3	13	13	SWDIO	P207	AGTWO1_A/ GTIOC0A_B	RXD9_A/ CTS3_A		IRQ1_A_DS		IOVCC
23	M10	D3	14	14	RES#							IOVCC

2 9.2.15 Sub-Clock Oscillator Mode Control Register (SOMCR)

Page 140 of 1343

The description for the SOMCR.SODRV bits is modified as follows.

Before modification

Base address SYSC = 0x4001_E000

Offset address 0x481

Bit position:	b7	b6	b5	b4	b3	b2	b1	b0
Bit field:	-	-	-	SONFSTP	-	-	SODRV	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	–	This bit is read as 0. The write value should be 0.	R/W
1	SODRV	Sub-Clock Oscillator Drive Capability Switching 0 : Standard CL 1 : Low CL	R/W
3:2	–	These bits are read as 0. The write value should be 0.	R/W
4	SONFSTP	Sub-Clock Oscillator Noise Filter Disable 0 : Noise filter is enabled 1 : Noise filter is disabled	R/W
7:5	–	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

When changing the bits other than SONFSTP, do so while SOSCCR.SOSTP is 1 (SOSC stopped).

SODRV bit (Sub-Clock Oscillator Drive Capability Switching)

The SODRVbit switches the drive capability of the sub-clock oscillator.

After modification

Base address SYSC = 0x4001_E000

Offset address 0x481

Bit position:	b7	b6	b5	b4	b3	b2	b1	b0
Bit field:	-	-	-	SONFSTP	-	-	SODRV	SODRV0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Description	R/W
0	SODRV0	Sub-Clock Oscillator Drive Capability Switching For details, see Table 9.5	R/W
1	SODRV	Sub-Clock Oscillator Drive Capability Switching For details, see Table 9.5	R/W
3:2	–	These bits are read as 0. The write value should be 0.	R/W
4	SONFSTP	Sub-Clock Oscillator Noise Filter Disable 0 : Noise filter is enabled. 1 : Noise filter is disabled.	R/W
7:5	–	読むと0が読めます。書く場合、0としてください。	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

When changing the bits other than SONFSTP, do so while SOSCCR.SOSTP is 1 (SOSC stopped).

SODRV, SODRV0 bit (Sub-Clock Oscillator Drive Capability Switching)

The SODRV and SODRV0 bit switches the drive capability of the sub-clock oscillator Table 9.5 shows the details of the functions of these bits.

Table 9.5 Setting of the Sub-Clock Oscillator Drive Capability

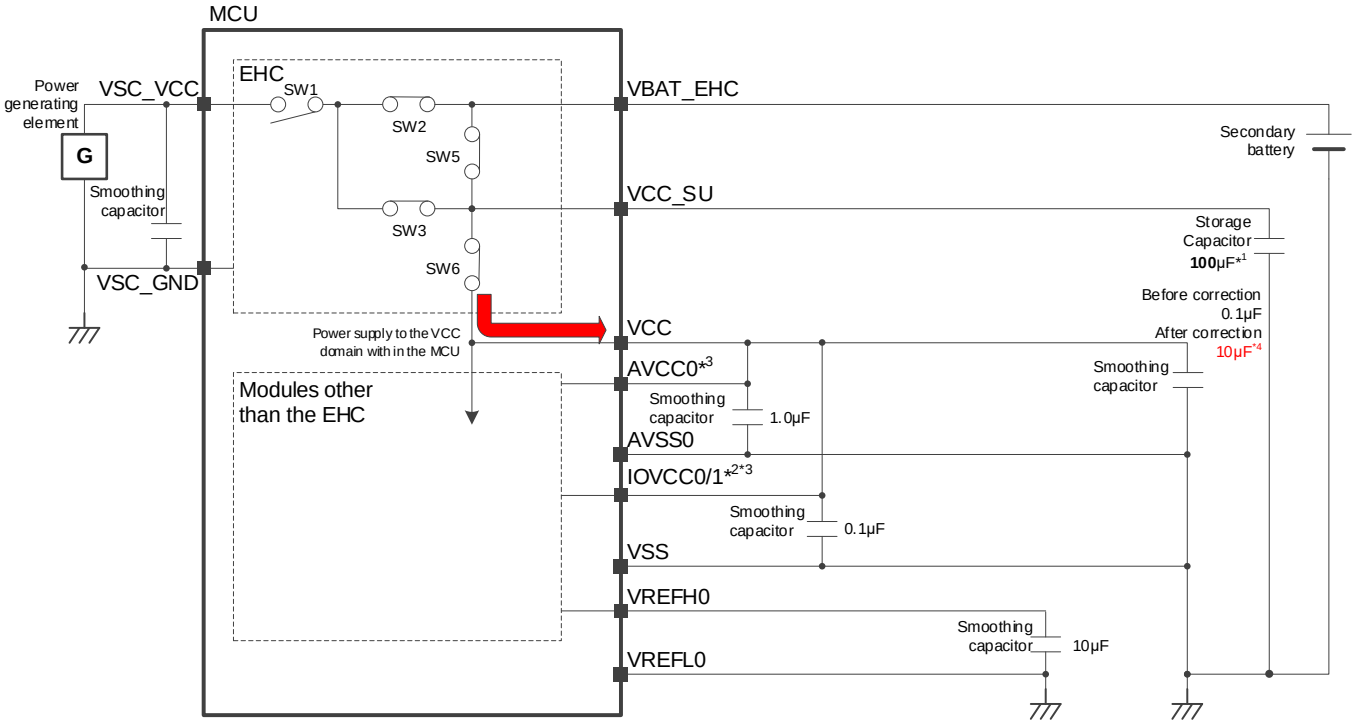
Setting		Function
SODRV	SODRV0	
0	0	Standard CL（CL=12.5pF）
0	1	Low CL6（CL is approximately 6pF） *1
1	0	Low CL4（CL is approximately 4pF） *1
1	1	Low CL7（CL is approximately 7pF） *1

Note1: Select the value closest to the capacitance of the low CL capacitance to be used.

3 1.2 Example of Connections in Energy Harvesting Startup Mode (1)

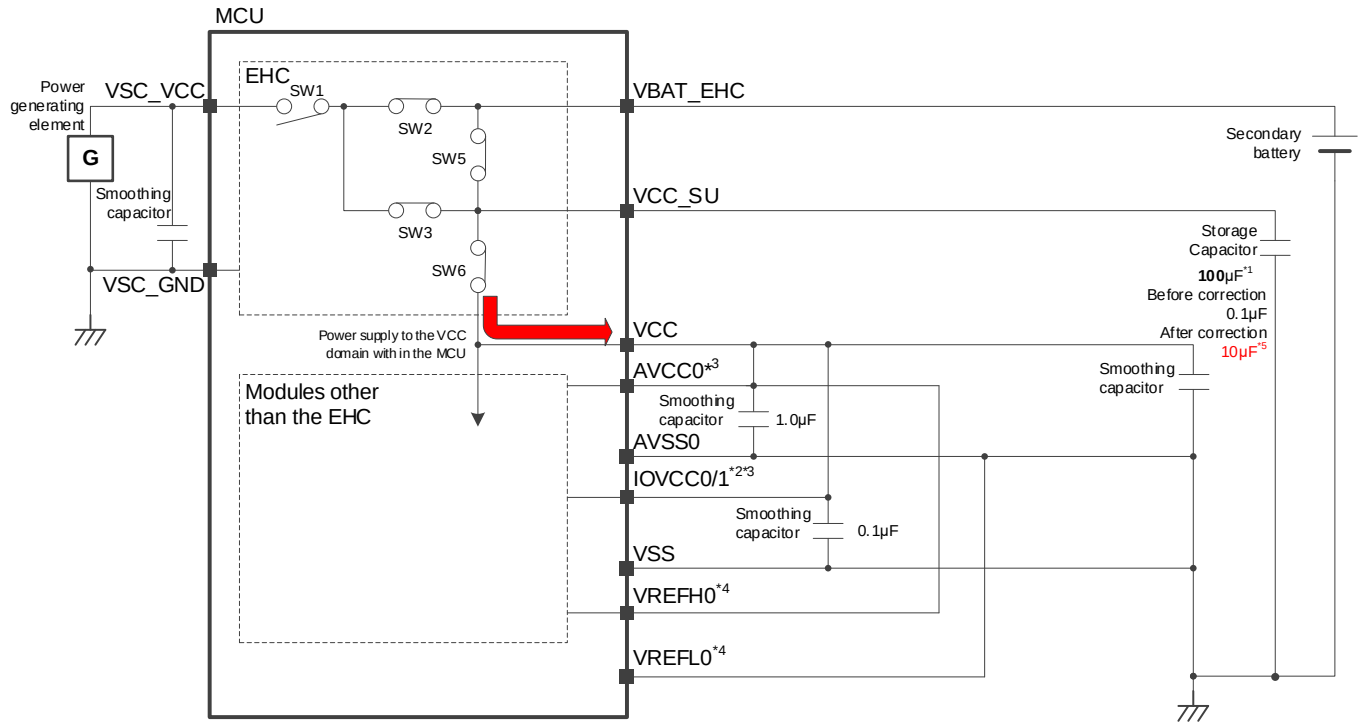
Page 1331 of 1343

The capacitance of a smoothing capacitor will be corrected in Figure 1.3 Energy harvesting startup mode with the VREF in use and Figure 1.4 Energy harvesting startup mode with AVCC0 as the reference voltage



Note: For details on the connections and values of capacitors, see section 1.5. Pin Functions in section 1, Overview.
Note1: The required capacitance of the storage capacitor depends on the ambient temperature range. For details, see section 51.9. EHC Characteristics.
Note2: A smoothing capacitor should be connected to each of IOVCC0/1.
Note3: Set the VOCR register to enable the supply of power to these pins.
Note4: The capacitance should be at least 1/10 that of the storage capacitor connected to the VCC_SU pin.

Figure 1.3 Energy harvesting startup mode with the VREF in use



Note: For details on the connections and values of capacitors, see section 1.5. Pin Functions in section 1, Overview.
Note1: The required capacitance of the storage capacitor depends on the ambient temperature range. For details, see section 51.9. EHC Characteristics.
Note2: A smoothing capacitor should be connected to each of IOVCC0/1.
Note3: Set the VOCR register to enable the supply of power to these pins.
Note4: In this example, the setting of the ADHVREFCNT register in the ADC14 is 0x00 (selecting AVCC0 as the reference voltage).
Note5: The capacitance should be at least 1/10 that of the storage capacitor connected to the VCC_SU pin.

Figure 1.4 Energy harvesting startup mode with AVCC0 as the reference voltage

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