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RENESAS TECHNICAL UPDATE

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Product Category	SOC		Document No.	TN-RE*-A0005A/E	Rev.	1.00
Title	Errata to RE01Group User's Manual:Hardware		Information Category	Technical Notification		
Applicable Product	RE01 Products with 256-Kbyte Flash Memory	Lot No. All	Reference Document	RE01 Group User's Manual:Hardware Rev.1.00 (R01UH0894EJ0100)		

This document describes corrections to the RE01 Group User's Manual: Hardware, Rev.1.00.

The corrections are indicated in red.

No	Chapter	Title	Content
1	1	Overview	Table 1.4 Pin Functions Description of Clock items is corrected.
2	9	Clock Generation Circuit	9.2.10 OSCSF : Oscillation Stabilization Flag Register HOCOSF flag is corrected.
3	22	I/O Ports	22.5.5 Regulator (LDO) stop is added.
4	28	Realtime Clock (RTC)	28.2.28 RTCCRn : Time Capture Control Register n (n = 0 to 2) TCEN bit (Time Capture Event Input Pin Enable) is corrected.
5	30	Watchdog Timer (WDT)	30.3.4 Status Flags Description is corrected.
6	31	Independent Watchdog Timer (IWDT)	31.3.3 Status Flags Description is corrected.

No.1 1.4 Pin Functions

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Table 1.4 Pin functions will be corrected as follows.

Before correction

Function	Signal	I/O	Description
Omitted			
Clock	XTAL	Input	MOSC resonator connect pin. EXTAL is an external clock input pin.
	EXTAL	Output	
	XCIN	Input	SOSC resonator connect pin
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
	CLKOUT32K	Output	SOSC clock output pin
Omitted			

After correction

Function	Signal	I/O	Description
Omitted			
Clock	XTAL	Output	MOSC resonator connect pin. EXTAL is an external clock input pin.
	EXTAL	Input	
	XCIN	Input	SOSC resonator connect pin
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
	CLKOUT32K	Output	SOSC clock output pin
Omitted			

No.2 9.2.10 OSCSF : Oscillation Stabilization Flag Register

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OSCSF.HOCOSF flag will be corrected as follows.

Before correction

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

The HOCOSF flag indicates the operating status of the counter that measures the wait time for the high-speed clock oscillator (HOCO). When OFS1.HOCOEN is set to 1, confirm that OSCSF.HOCOSF is also set to 1 before using the HOCO clock.

After correction

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

The HOCOSF flag indicates the operating status of the counter that measures the wait time for the high-speed clock oscillator (HOCO). When OFS1.HOCOEN is set to 0, confirm that OSCSF.HOCOSF is also set to 1 before using the HOCO clock.

No.3 22.5 Usage Notes

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Section 22.5.5 will be added as follows.

22.5.5 Regulator (LDO) stop

When the LDOCR.LDOCUT bit is set to 1, the P208 and P209 outputs are fixed. The LDOCR register is not initialized to 0 by some reset sources, so the outputs of P208 and P209 are held when the corresponding reset occurs. For details, see section 6, Resets.

No.4 28.2.28 RTCCRn : Time Capture Control Register n (n = 0 to 2)

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RTCCRn.TCEN bit will be corrected as follows.

Before correction

TCEN bit (Time Capture Event Input Pin Enable)

The TCEN bit enables or disables the time capture event input pins RTCIC0, RTCIC1, and RTCIC2.

Table 28.3 lists the conditions for enabling the RTCICn pin. Before setting this bit to 1, be sure to set RTC time capture event enable bit (RCPE.RTCEN), port control setting bits (PmnPFS.PSEL[4:0], and PmnPFS.PMR). For details on the port control setting bits (PmnPFS.PSEL[4:0] and PmnPFS.PMR), see section 22, I/O Ports.

Table 28.3 Conditions for Enabling the RTCICn Pin

PmnPFS.PSEL[4:0] PmnPFS.PMR	RCPE.RTCEN	RTCCRn.TCEN	Time Capture Event Input Pin Enabled/Disabled
RTCICn pin not selected	Don't care	Don't care	Disabled
RTCICn pin selected	0 (disabling input)	Don't care	
	1 (enabling input)	0 (disableing input)	
		1 (enabling input)	Enabled

After correction

TCEN bit (Time Capture Event Input Pin Enable)

The TCEN bit enables or disables the time capture event input pins RTCIC0, RTCIC1, and RTCIC2.

Table 28.3 lists the conditions for enabling the RTCICn pin. Before setting this bit to 1, be sure to set RTC time capture event enable bit (RCPE.RTCEN), port control setting bits (PmnPFS.PDR, and PmnPFS.PMR). For details on the port control setting bits (PmnPFS.PDR and PmnPFS.PMR), see section 22, I/O Ports.

Table 28.3 Conditions for Enabling the RTCICn Pin

PmnPFS	RCPE.RTCEN	RTCCRn.TCEN	Time Capture Event Input Pin Enabled/Disabled
PMR = 0 PDR = 0	0 (disabling input)	Don't care	Disabled
	1 (enabling input)	0 (disableing input)	
		1 (enabling input)	Enabled

No.5 30.3.4 Status Flag

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Description of status flag will be corrected as follows.

Before correction

30.3.4 Status Flags

The refresh error (WDTSR.REFEF) and underflow (WDTSR.UNDFF) flags retain the source of the reset signal output from the WDT or the source of the interrupt request from the WDT. After a release from the reset state or interrupt request generation, read the WDTSR.REFEF and WDTSR.UNDFF flags to check for the reset or interrupt source. For each flag, writing 0 clears the bit. Writing 1 has no effect. Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the next reset or interrupt request from the WDT, the earlier reset or interrupt source is cleared and the new reset or interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 30.2.3. WDTSR : WDT Status Register.

After correction

30.3.4 Status Flags

The refresh error (WDTSR.REFEF) and underflow (WDTSR.UNDFF) flags retain the source of the interrupt request from the WDT. After a release from the interrupt request generation, read the WDTSR.REFEF and WDTSR.UNDFF flags to check for the interrupt source. For each flag, writing 0 clears the bit. Writing 1 has no effect. Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the next interrupt request from the WDT, the earlier interrupt source is cleared and the new interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 30.2.3. WDTSR : WDT Status Register.

No.6 31.3.3 Status Flag

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Description of status flag will be corrected as follows.

Before correction

31.3.3 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the reset signal output or the source of the interrupt request from the IWDT. Therefore, after a release from the reset state or interrupt request generation, read the IWDTSR.REFEF and UNDFF flags to check for the reset or interrupt source. For each flag, writing 0 clears the bit and writing 1 has no effect.

Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the time of the next reset or interrupt request from the IWDT, the earlier reset or interrupt source is cleared and the new reset or interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 31.2.2. IWDTSR : IWDT Status Register.

After correction

31.3.3 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the interrupt request from the IWDT. Therefore, after a release from the interrupt request generation, read the IWDTSR.REFEF and UNDFF flags to check for the interrupt source. For each flag, writing 0 clears the bit and writing 1 has no effect.

Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the time of the next interrupt request from the IWDT, the earlier interrupt source is cleared and the new interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 31.2.2. IWDTSR : IWDT Status Register.

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