

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

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Title	Errata to R32C/118A Group User's Manual: Hardware	Information Category	Technical Notification		
Applicable Product	R32C/118A Group	Lot No.	Reference Document	R32C/118A Group User's Manual: Hardware Rev. 1.00 (REJ09B0577-0100)	

This document describes corrections to the R32C/118A Group User's Manual: Hardware, Rev. 1.00. The corrections are indicated in red in the list below.

- Page 24 of 639, specifications for pins P2_0 to P2_7 in Table 1.19 is corrected as follows:

Pin names	Package		Selectable Functions		5 V tolerant input ⁽³⁾
	176-pin	144-pin	Pull-up resistor ⁽¹⁾	N-channel open drain ⁽²⁾	
P2_0 to P2_7	✓	✓	✓	✓	

- Page 26 of 639, register symbol "R3R0" in line 3 of 2.1.1 is corrected as follows:

"R3R1"

- Page 42 of 639, description of register name "Increment/Decrement Counting Select Register" in Table 4.13 is corrected as follows:

"Increment/Decrement Select Register"

- Pages 67 to 68 and 81 to 82 of 639, description of register name "CAN1/0 Acceptance Mask Register 0/1/2/3/4/5/6/7" in Tables 4.38 to 4.39 and 4.52 to 4.53 is corrected as follows:

"CAN1/0 Mask Register 0/1/2/3/4/5/6/7"

- Pages 70 and 84 of 639, reset value "XXXX XX00b" for registers C1MSMR and C0MSMR in Tables 4.41 and 4.55 is corrected as follows:

"0000 0000b"

- Page 92 of 639, descriptions for the VDEN bit in Figure 6.4 are modified as follows:

Bit Symbol	Bit Name	Function	RW
VDEN	Low Voltage Detector Enable Bit	0: Low voltage detector disabled 1: Low voltage detector enabled	RW

- Page 94 of 639, description of the third paragraph in 6.2.1 is modified as follows:

"When the voltage rises to or above Vdet(R) again, the VMF bit becomes 1 ($V_{CC} \geq V_{det}$) and the LVDF bit becomes 1. At this point, an interrupt request is generated when the LVDIEN bit is 1."

•Page 100 of 639, Figure 8.1 is corrected as follows:

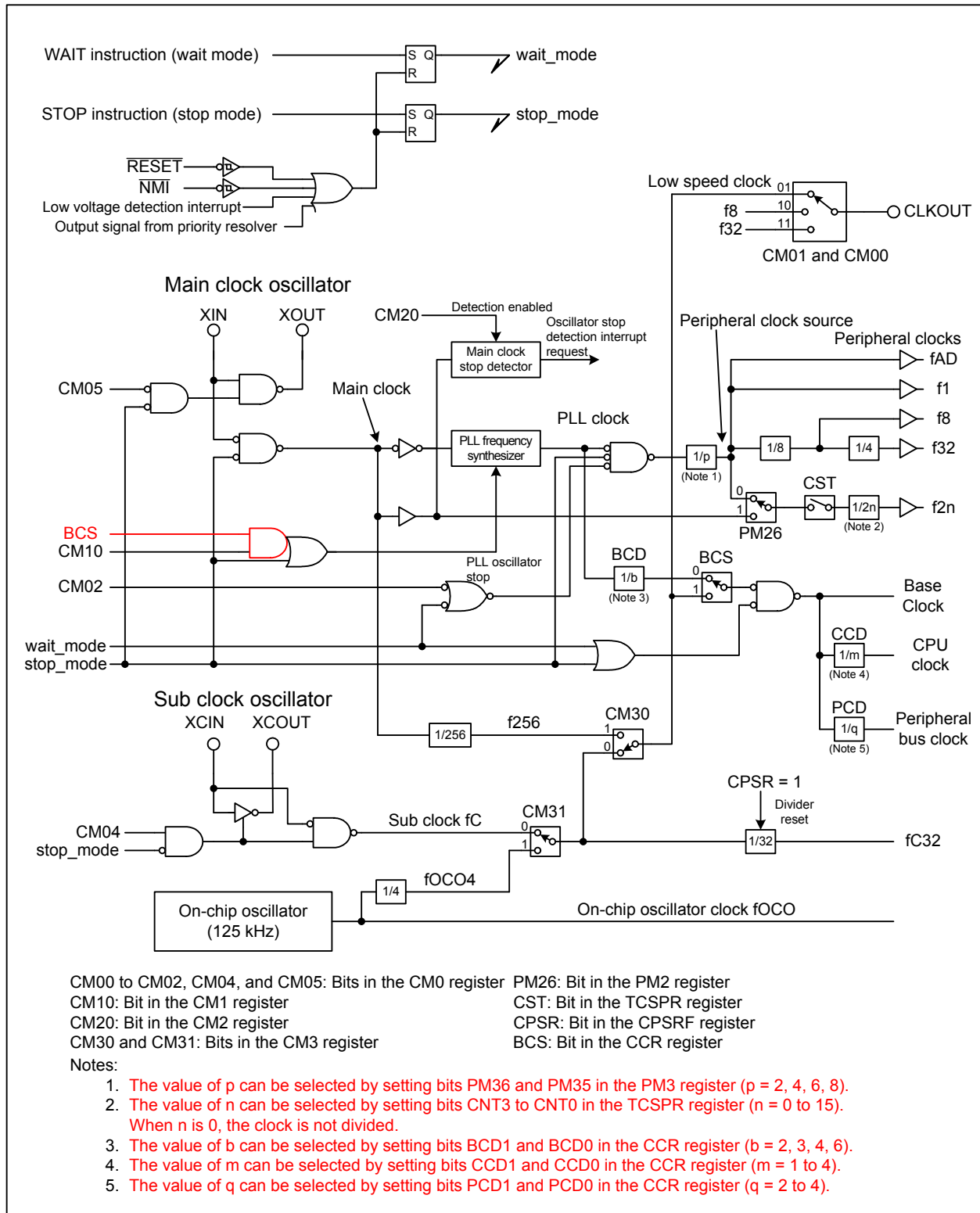


Figure 8.1 Clock Generation Circuitry

•Page 102 of 639, description of bit name “XCIN-XCOU Drive Power Select Bit” in Figure 8.3 is modified as follows:

“XCIN-XCOU Drive **Strength** Select Bit”

- Page 102 of 639, the following description is added to Note 8 in Figure 8.3:
 “When rewriting this bit while the watchdog timer is running, set it immediately after writing to the WDTS register.”
- Page 103 of 639, description of bit name “XIN-XOUT Drive Power Select Bit” in Figure 8.4 is modified as follows:
 “XIN-XOUT Drive **Strength** Select Bit”
- Page 103 of 639, description of Note 2 in Figure 8.4 is modified as follows:
 “When the BCS bit in the CCR register is 0 (PLL clock selected as base clock source), **the PLL frequency synthesizer does not stop oscillating even if the CM10 bit is set to 1.**”
- Page 104 of 639, bit symbol “CM02” in Note 3 of Figure 8.5 is corrected as follows:
 “**CM20**”
- Page 113 of 639, description of the last paragraph in 8.1.4 is modified as follows:
 “When the **WCSS** bit in the OFS area is 1 **and the WPCS bit is 0**, the on-chip oscillator clock is stopped after a reset. It starts running **when setting any of the following bits to 1**; the CM31 bit in the CM3 register, **the PM23 bit in the PM2 register, or the WDK4 bit in the WDK register. It is not necessary to wait for stabilization because the on-chip oscillator instantly starts oscillating.**”
- Page 114 of 639, description “(Refer to Figure 8.17 “State Transition (when the sub clock is used)”)” is deleted from 8.2.
- Page 123 of 639, description of 8.7.2 is modified as follows:
 “**The base clock stops in wait mode so that clocks generated by the base clock**, the CPU clock and peripheral bus clock, stop running as well. **Thus** the CPU and watchdog timer, operated by **these two clocks**, also stop. However, the watchdog timer continues operating when the PM23 bit in the PM2 register is 1 (on-chip oscillator selected as count source for the watchdog timer) or when the WDK4 bit in the WDK register is 1 (on-chip oscillator selected as count source for the prescaler). Since the main clock, sub clock, PLL clock, and on-chip oscillator clock continue running, **the peripherals** using these clocks also continue operating.”
- Page 132 of 639, mathematical symbol in 9.3.1 is corrected as follows:
 - In memory expansion mode

$$0080000h \leq (CB23 \times 2^{18}) \leq (CB12 \times 2^{18}) \leq (CB01 \times 2^{18}) \leq 3DC0000h$$
 - In microprocessor mode

$$0080000h \leq (CB23 \times 2^{18}) \leq (CB12 \times 2^{18}) \leq (CB01 \times 2^{18}) \leq 3FC0000h$$
- Pages 134 and 135 of 639, Note 2 “This register should not be set in single-chip mode.” is deleted from Figures 9.4 to 9.6.
- Pages 135 and 136 of 639, setting ranges for registers CB01, CB12, and CB23 in Figures 9.7 to 9.9 are corrected as follows:
 - CB01: “**02h** to F8h in memory expansion mode” and “**02h** to FFh in microprocessor mode”
 - CB12: “**02h** to **F8h** in memory expansion mode” and “**02h** to **FFh** in microprocessor mode”
 - CB23: “**02h** to **F8h** in memory expansion mode” and “**02h** to **FFh** in microprocessor mode”

- Pages 135 and 136 of 639, descriptions of Note 2 in Figures 9.7 to 9.9 are modified as follows:
 - CB01: “The setting value should be **equal to or greater than that of** the CB12 register.”
 - CB12: “The setting value should be **equal to or greater than that of** the CB23 register and **should be equal to or less than that of** the CB01 register.”
 - CB23: “The setting value should be **equal to or less than that of** the CB12 register.”
- Page 139 of 639, bit names of bits ESUR1 and ESUR0, bits ESUW1 and ESUW0, bits EWR1 and EWR0, and EWW1 and EWW0 in Figure 9.12 are modified as follows:
 - ESUR1 and ESUR0: “Address Setup **Cycles Before Read** Setting Bit”
 - ESUW1 and ESUW0: “Address Setup **Cycles Before Write** Setting Bit”
 - EWR1 and EWR0: “**Read** Pulse Width Setting Bit”
 - EWW1 and EWW0: “**Write** Pulse Width Setting Bit”
- Page 155 of 639, description “Bits PRC0 and PRC1 do not automatically become 0. They should be set to 0 by a program.” is deleted from Note 1 of Figure 10.1.
- Page 159 of 639, description of Note 1 in Figure 11.1 is modified as follows:
 - “**The peripheral interrupts are generated by the corresponding peripherals in the MCU.**”
- Page 160 of 639, descriptions in the second paragraph of (5) in 11.2 are modified as follows:
 - “The stack pointer (SP) **used for this interrupt differs depending on the software interrupt numbers.** For **software interrupt** numbers 0 to 127, when an interrupt request is accepted, the U flag is saved **and set to 0** to select the interrupt stack pointer (ISP) **during the interrupt sequence.** The saved data of the U flag is restored upon returning from the interrupt handler. For **software interrupt** numbers 128 to 255, the stack pointer **does not change during** the interrupt sequence.”
- Page 162 of 639, description of 11.5 is corrected as follows:
 - “Each interrupt vector has a 4-byte memory space, in which the start address of the associated interrupt handler is stored. When an interrupt request is accepted, **a jump** to the address set in the interrupt vector **takes place.** Figure 11.2 shows an interrupt vector.”
- Page 163 of 639, description in the Remarks for the BRK instruction in Table 11.1 is corrected as follows:
 - “If address FFFFFFFE7h is FFh, **a jump** to the **interrupt vector of software interrupt number 0** in the relocatable vector table **takes place**”
- Page 170 of 639, description for the IR bit below Figure 11.4 is corrected as follows:
 - “The IR bit becomes 1 (interrupt requested) when an interrupt request is generated; this bit setting is retained until the interrupt request is accepted. When the request is accepted and **a jump** to the corresponding interrupt vector **takes place,** the IR bit becomes 0 (no interrupt requested). The IR bit can be set to 0 by a program. This bit should not be set to 1.”
- Page 174 of 639, description of Note 1 in Table 11.7 is corrected as follows:
 - “**These are the values when the interrupt vectors are aligned to the addresses in multiples of 4 in the internal ROM. However, the condition does not apply to the fast interrupt.**”
- Page 181 of 639, register symbol “IIOiE” in line 16 of 11.13 is corrected as follows:
 - “**IIOiE**”
- Page 185 of 639, description in lines 4 to 6 of 12. Watchdog Timer is corrected as follows:
 - “**Select either an interrupt request or a reset with the CM06 bit in the CM0 register for** when the watchdog timer underflows. Once the CM06 bit is set to 1 (reset), it cannot be changed to 0 (watchdog timer interrupt) by a program. **It can be set to 0 only by a reset.**”

- Page 185 of 639, register symbol “WKD” in line 11 of 12. Watchdog Timer is corrected as follows:
“WDK”
- Page 190 of 639, expression “a value more than 00000001h” in the Specification of the DMA transfer start-up in Table 13.1 is corrected as follows:
“a value other than 00000000h”
- Page 198 of 639, description of the first paragraph in 13.1 is corrected as follows:
“The transfer cycle is composed of bus cycles to read data from (source read) or to write data to (destination write) memory or an SFR.”
- Page 199 of 639, external bus address “00060000h” in Table 13.5 is corrected as follows:
“00080000h”
- Page 204 of 639, source address “FFFFFFFh” in Note 1 of Table 14.1 is corrected as follows:
“FFFFFFFh”
- Page 204 of 639, bit symbol “IIRLT” in the fifth bullet point of 14.1 is corrected as follows:
“IRLT”
- Pages 206 and 207 of 639, expression “DMA II transfer complete interrupt vector address” in lines 3 to 4 and the seventh bullet point of 14.1.2 and Figure 14.2 is corrected as follows:
“jump address for the DMA II transfer complete interrupt handler”
- Pages 206 and 209 of 639, expression “interrupt vector” in Figure 14.2 and 14.1.4 is corrected as follows:
“interrupt vector space”
- Page 207 of 639, description “jump address” in the seventh bullet point of 14.1.2 is corrected as follows:
“start address”
- Page 208 of 639, bit names of the OPER bit and bits CNT0 to CNT2 in Figure 14.3 are modified as follows:
OPER: “Calculation Result Transfer Select Bit”
CNT0 to CNT2: “Number of Transfers Setting Bit”
- Page 222 of 639, expression “Counting” is deleted from bit names of bits TA0UD to TA4UD and the register name in Figure 16.7
- Page 230 of 639, bit name of the MR2 bit in Figure 16.12 is modified as follows:
“Increment/Decrement Switching Source Select Bit”
- Page 230 of 639, bit symbols “TAiTGH and TAiTGL” in Note 5 of Figure 16.12 are corrected as follows:
“TAjTGH and TAjTGL”
- Page 231 of 639, pin name “INT2” in Figures 16.13 and 16.14 is corrected as follows:
“INT2”
- Page 232 of 639, register symbol “TA4NR” in line 3 of 16.1.3 is corrected as follows:
“TA4MR”
- Page 249 of 639, description in the first bullet point of 16.3.3.2 is corrected as follows:
“While the TBjS bit in the TABSR or TBSR register is 1 (start counter), after the MR3 bit becomes 1 (overflow) and at least one count source cycle has elapsed, a write operation to the TBjMR register sets the MR3 bit to 0 (no overflow).”

- Page 249 of 639, expression “Tbj interrupt handler” in the eighth bullet point of 16.3.3.2 is changed as follows:
“timer Bj interrupt handler”
- Page 253 of 639, description of Note 1 in Figure 17.3 is modified as follows:
“Set this register after setting the PRC1 bit in the PRCR register to 1 (write enabled). Also, rewrite this register while timers A1, A2, A4, and B2 are stopped.”
- Page 260 of 639, description “The sum of setting values for registers TAI and TAI1 should be identical to the setting value of the TB2 register in this mode.” is deleted from lines 8 to 9 of 17.3
- Page 264 of 639, bit symbol “INV06” in Note 3 of Figure 17.15 is corrected as follows:
“INV16”
- Page 265 of 639, register symbol “INV1” in Note 2 of Figure 17.17 is corrected as follows:
“INVC1”
- Pages 273 and 274 of 639, descriptions for the CRD bit in Figures 18.5 and 18.6 are modified as follows:

Bit Symbol	Bit Name	Function	RW
CRD	CTS Function Disable Bit	0: CTS function enabled 1: CTS function disabled	RW

- Page 275 of 639, description of function of the UiIRS bit in Figure 18.7 is modified as follows:
“0: Transmit buffer is empty (TI = 1)
1: Transmission is completed (TXEPT = 1)”
- Page 278 of 639, description of function of the SWC bit in Figure 18.12 is modified as follows:
“0: No wait-state/wait-state cleared
1: Hold the SCLi pin low after the eighth bit is received”
- Page 279 of 639, description “UiBRG count source” in the function of bits DL0 to DL2 in Figure 18.13 is corrected as follows:
“baud rate generator count source”
- Page 280 of 639, description of function of the SWC9 bit in Figure 18.14 is modified as follows:
“0: No wait-state/wait-state cleared
1: Hold the SCLi pin low after the ninth bit is received”
- Page 288 of 639, description “Pulse stops because the TE bit is set to 0” in Figure 18.21 is corrected as follows:
“Data is transferred from the UiTB register to the UARTi transmit register”
- Page 288 of 639, description “TXEPT flag” in Figure 18.21 is corrected as follows:
“TXEPT bit”
- Page 288 of 639, bit symbol “UiRS” in the fourth dash of Figure 18.21 is corrected as follows:
“UiIRS”
- Pages 296 and 297 of 639, descriptions of functions of the UiIRS bit in Figures 18.26 and 18.27 are corrected as follows:
0: “(an interrupt request is generated when the transmit buffer is empty)”
1: “(an interrupt request is generated when transmission is completed)”

- Page 333 of 639, description in 19.1.5 is modified as follows:
 “In repeat sweep mode 1, the analog voltage applied to eight selected pins including **one to four** prioritized pins is repeatedly converted into a digital code. Table 19.6 lists specifications of repeat sweep mode 1.”
- Page 333 of 639, description for the function in Table 19.6 is modified as follows:
 “**The analog voltage applied to eight selected pins including one to four prioritized pins is repeatedly converted into a digital code. The prioritized pins are selected by setting bits SCAN1 and SCAN0 in the AD0CON1 register and bits APS1 and APS0 in the AD0CON2 register**”
- Page 342 of 639, description “AD0i register” in the ninth bullet point of 19.3.2 is modified as follows:
 “**AD00 register**”
- Page 345 of 639, Figure 21.1 is corrected as follows:

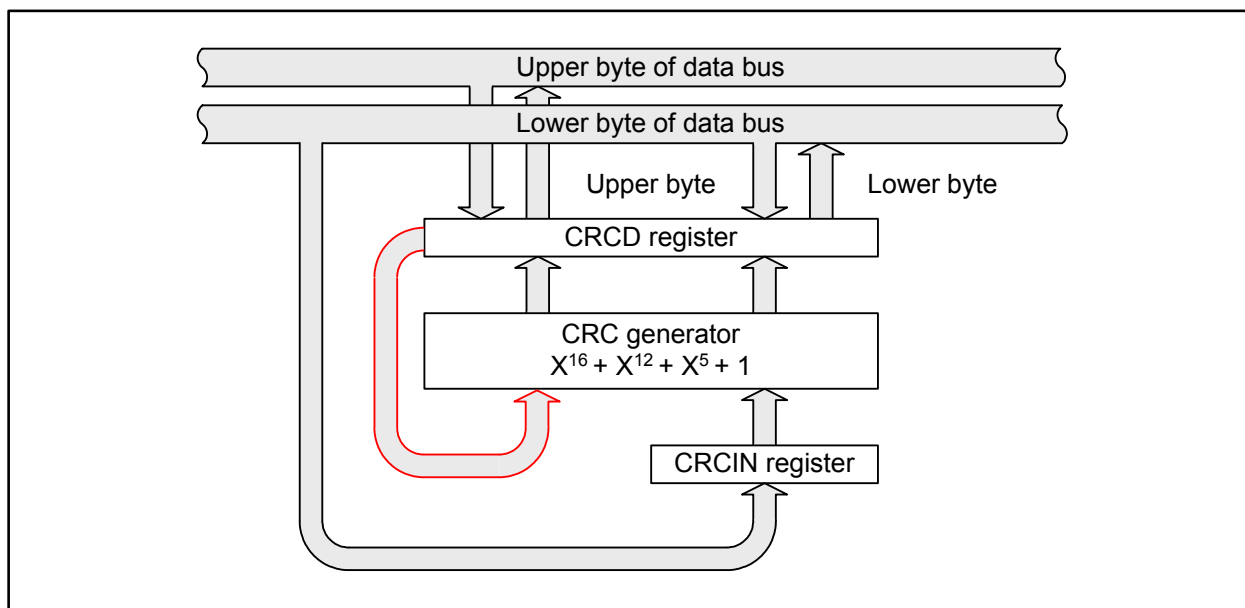


Figure 21.1 CRC Calculator Block Diagram

- Page 355 of 639, pin name “IE_OUT” in Figure 23.3 is corrected as follows:
 “**IEOUT**”
- Page 358 of 639, descriptions for bits UD0 and UD1 in Figure 23.6 are modified as follows:

Bit Symbol	Bit Name	Function	RW
UD0	Increment/Decrement Control Bit	b6 b5 0 0 : Increment mode	RW
UD1		0 1 : Increment/decrement mode 1 0 : Two-phase pulse signal processing mode ⁽⁶⁾	RW
		1 1 : Do not use this combination	

- Page 361 of 639, Note 3 “The GOC bit becomes 0 after gating is cleared.” is deleted from Figure 23.9.
- Page 367 of 639, description in the second bullet point for the reset conditions in Table 23.2 is modified as follows:
 “An input of low signal into the external interrupt pin (**INT0 or INT1**) as follows:”

- Page 368 of 639, description in the first bullet point for the selectable functions in Table 23.2 is corrected as follows:
 “The base timer starts counting when the BTS or BTiS bit is set to 1. **When the base timer reaches** FFFFh, it starts **decrementing**. When the RST1 bit in the GiBCR1 register is 1 (**the base timer is** reset by **matching** with the GiPO0 register), the timer counter starts **decrementing two counts after** the base timer value **matches** the GiPO0 register setting. When the timer counter **reaches** 0000h, it starts **incrementing** again (refer to Figure 23.20).”
- Pages 379, 381, and 384 of 639, description “Input to the IIOi_j pin” in Figures 23.25 to 23.27 is corrected as follows:
 “**IIOi_j pin**”
- Pages 386 and 388 of 639, description “Input to the OUTC2_j pin” in Figures 23.28 and 23.30 is corrected as follows:
 “**OUTC2_j pin**”
- Page 388 of 639, description “Bits RST2 to RST0 in the G2BCR1 register are set to 000b (base timer is not reset)” in the second dash is deleted from Case 1 in Figure 23.30.
- Page 400 of 639, “slave-transmit mode” is deleted from the description for the slave address match detector in Table 24.2.
- Page 405 of 639, description in Note 1 of Table 24.3 is modified as follows:
 “The CKS value must be set so the SCL clock frequency is 100 kHz **or less** in Standard-mode or 400 kHz **or less** in Fast-mode. The high period of the SCL has a margin of error of +2 to -4 ϕ IIC in Standard-mode, and +2 to -2 ϕ IIC in Fast-mode. Note that if the high period is shortened, the low period is lengthened, so the frequency remains unchanged.”
- Page 418 of 639, bit symbol “STR” in line 8 of 24.2 is corrected as follows:
 “**TRS**”
- Pages 421 and 422 of 639, “VIIC” in Figures 24.19 and 24.22 is modified as follows:
 “ **ϕ IIC**”
- Page 436 of 639, descriptions for the RBOC bit in Figure 26.2 are modified as follows:

Bit Symbol	Bit Name	Function	RW
RBOC	Forced Recovery From Bus-off Bit ⁽⁴⁾	0: Nothing occurred 1: Forced recovery from bus-off ⁽⁵⁾	RW

- Page 453 of 639, description “fCAN (CAN system clock)” in line 5 of 26.1.9.5 is modified as follows:
 “**the peripheral bus clock**”
- Page 456 of 639, description “fCAN” in line 6 of 26.1.10.3 is modified as follows:
 “**the peripheral bus clock**”
- Page 462 of 639, description of function of b7 in Figure 26.17 is corrected as follows:
 b7: “No register bit; **the read value is 0**” (“should be written with 0 and” is deleted)
- Page 466 of 639, description of function of b6-b5 in Figure 26.19 is corrected as follows:
 b6-b5: “No register bits; **the read value is 0**” (“should be written with 0 and” is deleted)

- Page 486 of 639, description of the first paragraph in 26.2.3 is modified as follows:
 “CAN sleep mode is used for reducing current consumption by stopping the clock supply to the CAN module. After a MCU reset, the CAN module starts from CAN sleep mode.”
- Page 489 of 639, q value “q = 1, 2, 3, 4” in Figure 26.36 is corrected as follows:
 “q = 2, 3, 4”
- Page 501 of 639, description of the first and second paragraphs in 27. I/O Pins is corrected as follows (refer to TN-16C-A200A/E):
 “Each pin of the MCU functions as a programmable I/O port, an I/O pin for integrated peripherals, or a bus control pin. These functions can be switched by the function select registers or the processor mode registers. This chapter particularly addresses the function select registers. For the use as a bus control pin, refer to 7. “Processor Mode” and 9. “Bus”.
 The pull-up resistors are enabled for every group of four pins. However, a pull-up resistor is separated from other peripherals even if it is enabled, when a pin functions as an output pin.” (“or an analog I/O pin” is deleted)
- Page 501 of 639, Figure 27.1 is corrected as follows (refer to TN-16C-A200A/E):

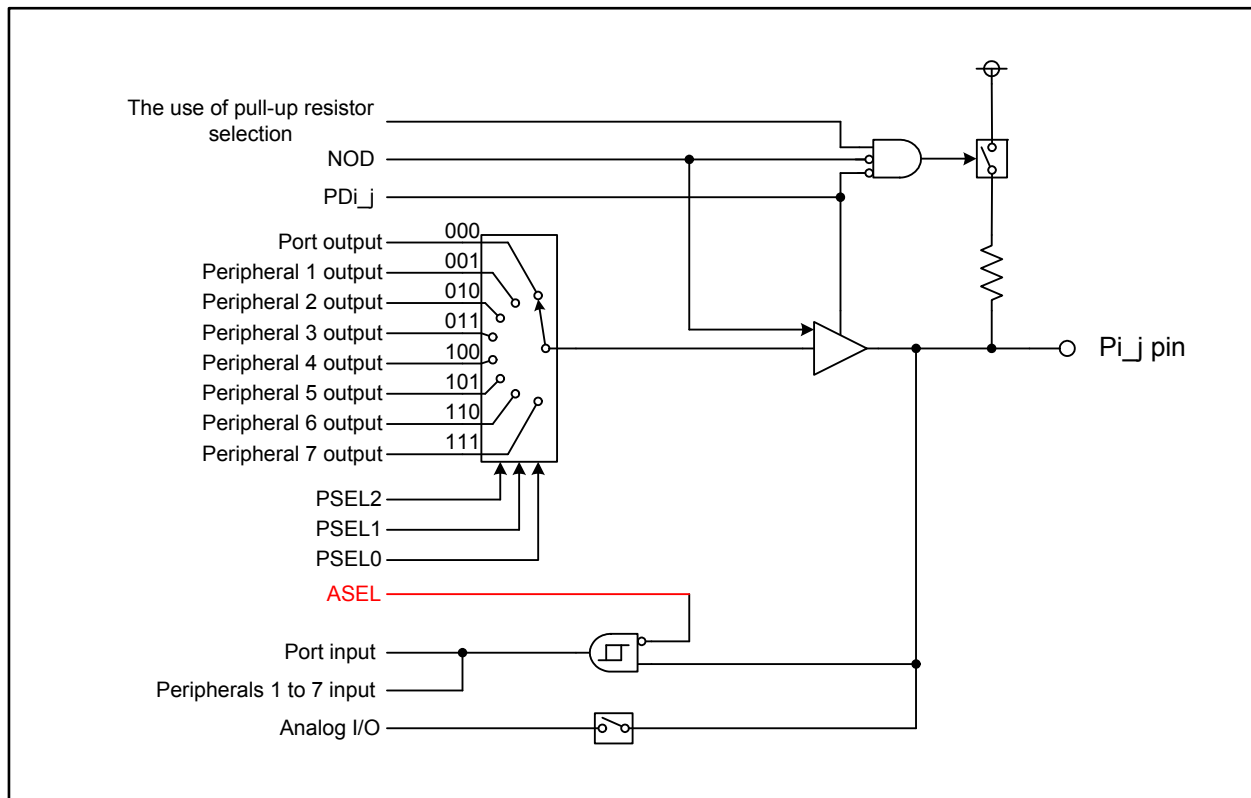


Figure 27.1 Typical I/O Pin Block Diagram (i = 0 to 19; j = 0 to 7)

- Page 501 of 639, description in the last paragraph of 27. I/O Pins is corrected as follows:
 “The input-only port P8_5 shares a pin with $\overline{\text{NMI}}$ and has no function select register or bit 5 in the PD8 register. Port P14_1 also functions as an input-only port. The function select register and bit 1 in the PD14 register are reserved. Port P9 is protected from unexpected write accesses by the PRC2 bit in the PRCR register (refer to 10. “Protection”).”
- Page 502 of 639, pin symbols “WR/WR0”, “BC1/WR1”, “BC2/WR2”, and “BC3/WR3” in line 4 of 27.1 are corrected as follows:
 “ $\overline{\text{WR/WR0}}$ ”, “ $\overline{\text{BC1/WR1}}$ ”, “ $\overline{\text{BC2/WR2}}$ ”, “ $\overline{\text{BC3/WR3}}$ ”

- Pages 505, 516, and 520 of 639, descriptions “IIO0 output” and “IIO1 output” in Figures 27.4, 27.14, and 27.18 are changed as follows:
“IIO0_i output” and “IIO1_i output”
- Page 507 of 639, description “PD3_i register” in line 3 below Figure 27.6 is corrected as follows:
“PD3_i bit”
- Page 566 of 639, register symbol “FMSR” in line 6 of 28.3.6.2 is corrected as follows:
“FMSR0”
- Page 582 of 639, description “Programming and erasure endurance of flash memory” in Table 29.8 is changed as follows:
“Program/erase cycles”
- Page 582 of 639, unit “times” for “Programming and erasure endurance of flash memory” in Table 29.8 is corrected as follows:
“Cycles”
- Pages 587 and 600 of 639, the following pins are added to the hysteresis for V_{T+} - V_{T-} in Tables 29.16 and 29.42:
“MSCL” and “MSDA”
- Pages 588 and 601 of 639, description “Driver power” in Tables 29.17 and 29.43 is modified as follows:
“Drive strength”
- Pages 594 and 607 of 639, pin name “INTi” in the title of Tables 29.32 and 29.58 is corrected as follows:
“INTi”
- Page 618 of 639, expression “counting” is deleted from the UDF register name in Table 30.1.
- Page 626 of 639, description in the first bullet point of 30.7.3.2 is corrected as follows:
“While the TBjS bit in the TABSR or TBSR register is 1 (start counter), after the MR3 bit becomes 1 (overflow) and at least one count source cycle has elapsed, a write operation to the TBjMR register sets the MR3 bit to 0 (no overflow).”
- Page 626 of 639, expression “TBj interrupt handler” in the eighth bullet point of 30.7.3.2 is changed as follows:
“timer Bj interrupt handler”
- Page 631 of 639, description “AD0i register” in the ninth bullet point of 30.10.2 is modified as follows:
“AD00 register”