This document describes corrections to the chapter “CAN module” in the User’s Manuals: Hardware of the above groups. The corrections are indicated in red in the list below.

Page and section numbers are based on the R32C/121 Group. Refer to the table on the last page for the corresponding pages and chapters in other groups.

• Page 459 of 608
  The description in 25.1.20.8 BLIF Bit is corrected as follows:

  **Before correction**

  The BLIF bit becomes 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.
  After the BLIF bit becomes 1, **32 consecutive dominant bits are detected again under** either of the following conditions:
  • After this bit is set to 0 from 1, recessive bits are detected.
  • After this bit is set to 0 from 1, the CAN module enters CAN reset mode or CAN halt mode and then enters CAN operation mode again.

  **Corrections**

  The BLIF bit becomes 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.
  After the BLIF bit becomes 1, **bus lock can be detected again after** either of the following conditions **is satisfied**:
  • After this bit is set to 0 from 1, recessive bits are detected (**bus lock is resolved**).
  • After this bit is set to 0 from 1, the CAN module enters CAN reset mode and then enters CAN operation mode again (**internal reset**).
Note 3 is added to Figure 25.34 as follows:

**Before correction**

![Diagram showing transition between CAN Operating Modes (i = 0, 1)](image)

**Notes:**
1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the BOM bit.
   - When the BOM bit is 01b, the state transition timing is immediately after entering the bus-off state.
   - When the BOM bit is 10b, the state transition timing is at the end of the bus-off state.
   - When the BOM bit is 11b, the state transition timing is at the setting of the CANM bit to 10b (CAN halt mode).
2. Write only to the SLPM bit to exit/set CAN sleep mode.

**Figure 25.34 Transition between CAN Operating Modes (i = 0, 1)**
Corrections

Figure 25.34 Transition between CAN Operating Modes (i = 0, 1)

Notes:
1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the BOM bit.
   - When the BOM bit is 01b, the state transition timing is immediately after entering the bus-off state.
   - When the BOM bit is 10b, the state transition timing is at the end of the bus-off state.
   - When the BOM bit is 11b, the state transition timing is at the setting of the CANM bit to 10b (CAN halt mode).
2. Write only to the SLPM bit to exit/set CAN sleep mode.
3. The CAN module does not enter CAN Halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

CANM, SLPM, BOM, and RBOC: Bits in the CiCTL register

- When the BOM bit is 00b or 11b (no halt request) and 11 consecutive recessive bits are detected 128 times or the RBOC bit is 1.
Table 25.9 is corrected as follows:

Before correction

<table>
<thead>
<tr>
<th>Mode</th>
<th>Receiver</th>
<th>Transmitter</th>
<th>Bus-off</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAN reset mode</td>
<td>CAN module enters CAN reset mode without waiting for the end of message reception</td>
<td>CAN module enters CAN reset mode after waiting for the end of message transmission (^{(1, 4)})</td>
<td>CAN module enters CAN reset mode without waiting for the end of bus-off recovery</td>
</tr>
</tbody>
</table>
| CAN halt mode | CAN module enters CAN halt mode after waiting for the end of message reception \(^{(2, 3)}\) | CAN module enters CAN halt mode after waiting for the end of message transmission \(^{(1, 4)}\) | - When the BOM bit is 00b
  - A halt request from a program will be acknowledged only after bus-off recovery
  - When the BOM bit is 01b
  - CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program)
  - When the BOM bit is 10b
  - CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program)
  - When the BOM bit is 11b
  - CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off |

BOM bit: Bit in the CiCTL register \(i = 0, 1\)

Notes:

1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first message transmission. When CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.

2. If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF bit in the CIEIFR register.

3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN mode transits to CAN halt mode.

4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN mode transits to the requested CAN mode.
Table 25.9 Operation in CAN Reset Mode and CAN Halt Mode

<table>
<thead>
<tr>
<th>Mode</th>
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<th>Bus-off</th>
</tr>
</thead>
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<td>CAN reset mode</td>
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<td>CAN module enters CAN reset mode after waiting for the end of message transmission &lt;sup&gt;(1, 4)&lt;/sup&gt;</td>
<td>CAN module enters CAN reset mode without waiting for the end of bus-off recovery</td>
</tr>
</tbody>
</table>
| CAN halt mode   | CAN module enters CAN halt mode after waiting for the end of message reception <sup>(2, 3)</sup> | CAN module enters CAN halt mode after waiting for the end of message transmission <sup>(1, 2, 4)</sup> | - When the BOM bit is 00b  
- A halt request from a program will be acknowledged only after bus-off recovery  
- When the BOM bit is 01b  
- CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program)  
- When the BOM bit is 10b  
- CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program)  
- When the BOM bit is 11b  
- CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off |

BOM bit: Bit in the CiCTLRR register (i = 0, 1)

Notes:

1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first message transmission. When CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.

2. If the CAN bus is locked in dominant state, the program can detect this state by monitoring the BLIF bit in the CiEIFR register. The CAN module does not enter CAN Halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.
<table>
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<th>Page Number, Figure/Title Number</th>
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</thead>
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</tr>
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<td>R32C/161 Group</td>
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<td>Page 447 24.1.20.8 Page 456 Figure 24.34 Page 458 Table 24.9</td>
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