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RENESAS TECHNICAL UPDATE

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Title	Errata to R32C/111 Group Hardware Manual No. 3		Information Category	Technical Notification		
Applicable Product	R32C/111 Group	Lot No.	Reference Document	R32C/111 Group Hardware Manual Rev. 1.10 (REJ09B0424-0110)		

This document describes corrections to the R32C/111 Group Hardware Manual, Rev. 1.10.
The corrections are indicated in red in the list below.

- Pages 4 and 6 of 493, operating mode in the Performance column of the CPU in Tables 1.3 and 1.5 is corrected as follows:
  "Operating mode: Single-chip mode"
  ("memory expansion mode" and "microprocessor mode" are deleted)

- Page 24 of 493, description "Output of the clock with the same frequency as fC, f8, or f32" in the description for the Clock output column in Table 1.15 is corrected as follows:
  "Output of the clock with the same frequency as low speed clocks, f8, or f32"

- Page 32 of 493, register symbol "R3R0" in line 3 of 2.1.1 is corrected as follows:
  "R3R1"

- Page 41 of 493, description of register name "Group 1 Timer Measurement Prescaler Register 6/7" in Table 4.6 is corrected as follows:
  "Group 1 Time Measurement Prescaler Register 6/7"

- Page 44 of 493, description of register name "Group 0 Timer Measurement Prescaler Register 6/7" in Table 4.9 is corrected as follows:
  "Group 0 Time Measurement Prescaler Register 6/7"

- Page 48 of 493, description of register name "UART2 Transmission/Receive Mode Register" in Table 4.13 is corrected as follows:
  "UART2 Transmit/Receive Mode Register"

- Page 48 of 493, description of register name "Increment/Decrement Counting Select Register" in Table 4.13 is corrected as follows:
  "Increment/Decrement Select Register"

- Page 50 of 493, reset value of the AD0CON2 register "X00X X000b" in Table 4.15 is corrected as follows:
  "XX0X X000b"

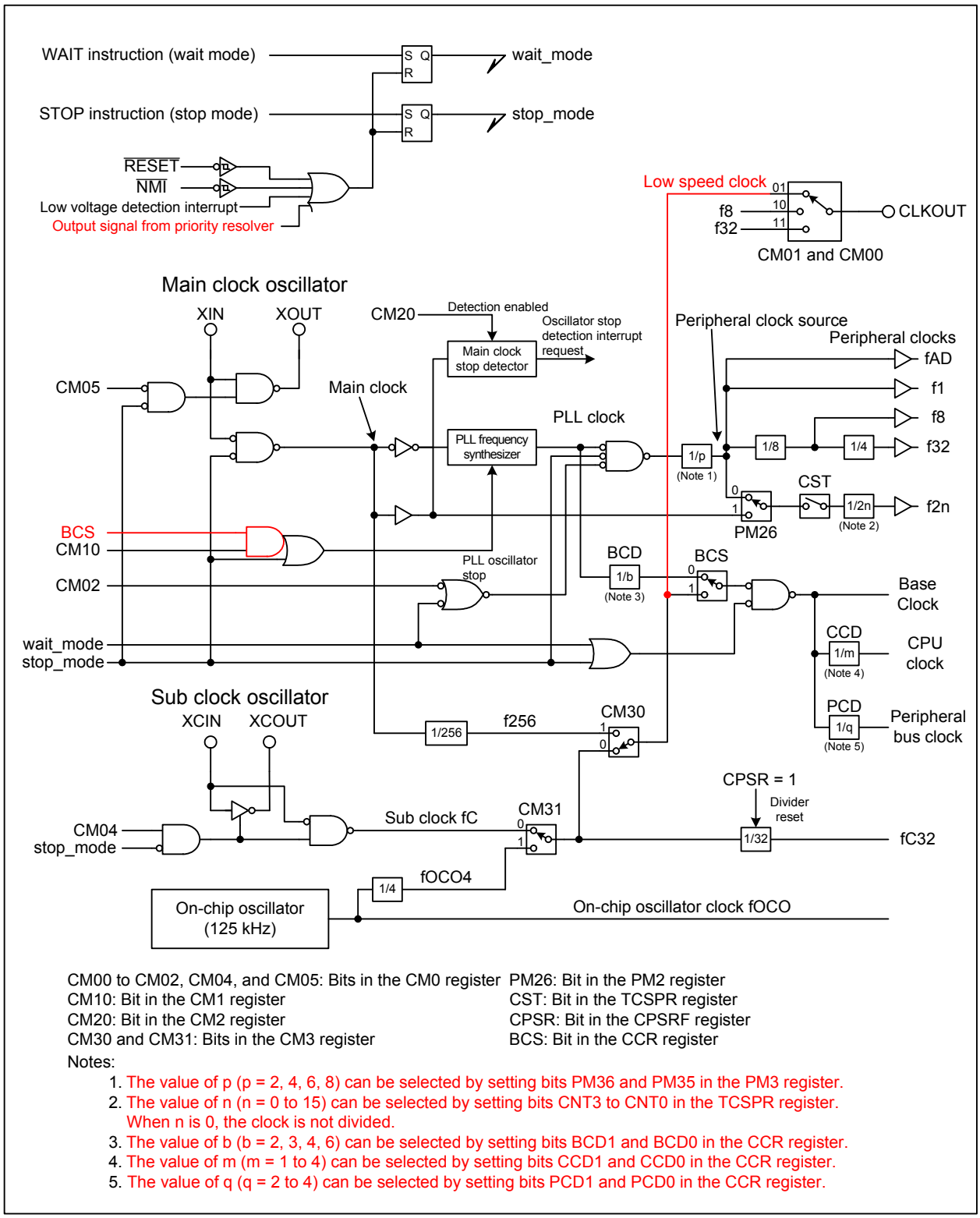
- Page 59 of 493, description of register name "External Interrupt Source Select Register 1/0" in Table 4.24 is corrected as follows:
  "External Interrupt Request Source Select Register 1/0"

•Page 68 of 493, descriptions for the VDEN bit in Figure 6.4 are modified as follows:

Bit Symbol	Bit Name	Function	RW
VDEN	Low Voltage Detector Enable Bit	0: Low voltage detector disabled 1: Low voltage detector enabled	RW

•Page 73 of 493, address of the PM0 register “44044h” in Figure 7.1 is corrected as follows:
“40044h”

•Page 76 of 493, Figure 8.1 is corrected as follows:



CM00 to CM02, CM04, and CM05: Bits in the CM0 register
CM10: Bit in the CM1 register
CM20: Bit in the CM2 register
CM30 and CM31: Bits in the CM3 register
PM26: Bit in the PM2 register
CST: Bit in the TCSPR register
CPSR: Bit in the CPSRF register
BCS: Bit in the CCR register

Notes:

1. The value of p (p = 2, 4, 6, 8) can be selected by setting bits PM36 and PM35 in the PM3 register.
2. The value of n (n = 0 to 15) can be selected by setting bits CNT3 to CNT0 in the TCSPR register. When n is 0, the clock is not divided.
3. The value of b (b = 2, 3, 4, 6) can be selected by setting bits BCD1 and BCD0 in the CCR register.
4. The value of m (m = 1 to 4) can be selected by setting bits CCD1 and CCD0 in the CCR register.
5. The value of q (q = 2 to 4) can be selected by setting bits PCD1 and PCD0 in the CCR register.

Figure 8.1 Clock Generation Circuitry

•Page 77 of 493, descriptions of Notes 2 and 6 in Figure 8.2 are corrected as follows:
Note 2: "The divide ratios of the base clock and peripheral bus clock should not be changed simultaneously. Doing so may cause the peripheral bus clock frequency to go over the maximum operating frequency." ("To increase the base clock frequency, the divide ratio of the peripheral bus clock should be increased before reducing the divide ratio of base clock." is deleted)
Note 6: "To use these low speed clocks, select one of them by setting bits CM31 and CM30 in the CM3 register and then set the BCS bit to 1."

•Pages 78, 92, 99, and 102 of 493, description "fC" in the function column of bits CM00 and CM01 in Figure 8.3, Section 8.6, Tables 8.3 to 8.5, and Table 8.7 is corrected as follows:
Figure 8.3: "0 1 : Output a low speed clock"
Section 8.6: "Low speed clocks, f8, and f32 can be output from the CLKOUT pin in the 100-pin package."
Tables 8.3 and 8.4: "Output a low speed clock"
Table 8.5: "When a low speed clock is selected"
Table 8.7: "When a low speed clock is selected"

•Page 78 of 493, the following description is added to Figure 8.3 as Note 8:
"Set this bit before activating the watchdog timer. When rewriting this bit while the watchdog timer is running, set it immediately after writing to the WDTS register."

•Page 79 of 493, description of bit name "PLL Clock Oscillator Stop Bit" in Figure 8.4 is modified as follows:
"PLL Oscillator Stop Bit"

•Page 79 of 493, description of Note 2 in Figure 8.4 is corrected as follows:
"When the BCS bit in the CCR register is 0 (PLL clock selected as base clock source), the PLL frequency synthesizer does not stop oscillating even if the CM10 bit is set to 1."

•Page 79 of 493, the following description is added to Figure 8.4 as Note 4:
"These bits become 01b when the main clock is stopped. When setting to 00b or 10b, rewrite them after the main clock is fully stabilized."

•Page 80 of 493, bit symbol "CM02" in Note 3 of Figure 8.5 is corrected as follows:
"CM20"

•Page 80 of 493, description of Note 1 in Figure 8.6 is corrected as follows:
"Rewrite this register after setting the PRC27 bit in the PRCR2 register to 1 (write enabled) and while the BCS bit in the CCR register is 0 (PLL clock)."

•Page 82 of 493, descriptions in Note 3 in Figure 8.9 are modified as follows:
"CM05 bit in the CM0 register (main clock oscillator enabled/disabled)
CM10 bit in the CM1 register (PLL oscillator enabled/disabled)"

•Page 82 of 493, the following description is added to Figure 8.9 as Note 5:
"Disable all the peripheral functions that use f2n before rewriting this bit."

•Page 83 of 493, the following description is added to Note 1 in Figure 8.10:
"Disable all the peripheral functions that use fAD, f1, f8, f32, or f2n (when the clock source is the peripheral clock source) to rewrite this register."

•Page 87 of 493, descriptions for the SEO bit in Figure 8.15 are corrected as follows:

Bit Symbol	Bit Name	Function	RW
SEO	Self-oscillating Setting Bit	0: PLL lock-in 1: Self-oscillating	RW

•Page 90 of 493, description “(Refer to Figure 8.17 “State Transition (when the sub clock is used)”)” is deleted from 8.2.

•Page 90 of 493, description of the second paragraph in 8.2.1 is corrected as follows:
“When the main clock oscillator resumes running after an oscillator stop is detected, the PLL clock frequency may temporarily exceed the preset value before the PLL frequency synthesizer oscillation stabilizes. As soon as an oscillator stop is detected, the main clock oscillator should be stopped from resuming (set the CM05 bit in the CM0 register to 1) or the divide ratios of the base clock and peripheral clock source should be increased by a program. They can be set using bits BCD1 and BCD0 in the CCR register and bits PM36 and PM35 in the PM3 register.”

•Page 94 of 493, description “f(XPLL)” in the third row of Figure 8.17 is corrected as follows:
“f(PLL)”

•Page 95 of 493, description “CM0 = 1” in the fourth row of Figure 8.18 is corrected as follows:
“CM05 = 1”

•Page 96 of 493, description “CM31 = 1” in the first row and “CM10 = 0” for “Low speed mode” in the second row of Figure 8.19 are corrected as follows:
“CM31 = 0” and “CM10 = 1”

•Page 98 of 493, description in 8.7.2 is corrected as follows:
“The base clock stops in wait mode so that clocks generated by the base clock, the CPU clock and peripheral bus clock, stop running as well. Thus the CPU and watchdog timer, operated by these two clocks, also stop. Since the main clock, sub clock, PLL clock, and on-chip oscillator clock continue running, peripheral functions using these clocks also continue operating.”

•Page 101 of 493, description in 8.7.3 is corrected as follows:
“In stop mode, all of the clocks, except for those that are protected, stop running. That is, the CPU and peripheral functions, operated by the CPU clock and peripheral clock, also stop. This mode saves the most power.”

•Page 107 of 493, mathematical symbol in 9.3.1 is corrected as follows:
• In memory expansion mode

$$0080000\text{h} \le (\text{CB23} \times 2^{18}) \le (\text{CB12} \times 2^{18}) \le (\text{CB01} \times 2^{18}) \le 3\text{DC0000h}$$

• In microprocessor mode

$$0080000\text{h} \le (\text{CB23} \times 2^{18}) \le (\text{CB12} \times 2^{18}) \le (\text{CB01} \times 2^{18}) \le 3\text{FC0000h}$$

•Page 109 of 493, Note 2 “This register should not be set in single-chip mode.” is deleted from Figures 9.4 and 9.5.

•Pages 110 and 111 of 493, setting ranges for registers CB01, CB12, and CB23 in Figures 9.6 to 9.8 are corrected as follows:
CB01 register: “02h to F8h in memory expansion mode” and “02h to FFh in microprocessor mode”
CB12 register: “02h to F8h in memory expansion mode” and “02h to FFh in microprocessor mode”
CB23 register: “02h to F8h in memory expansion mode” and “02h to FFh in microprocessor mode”

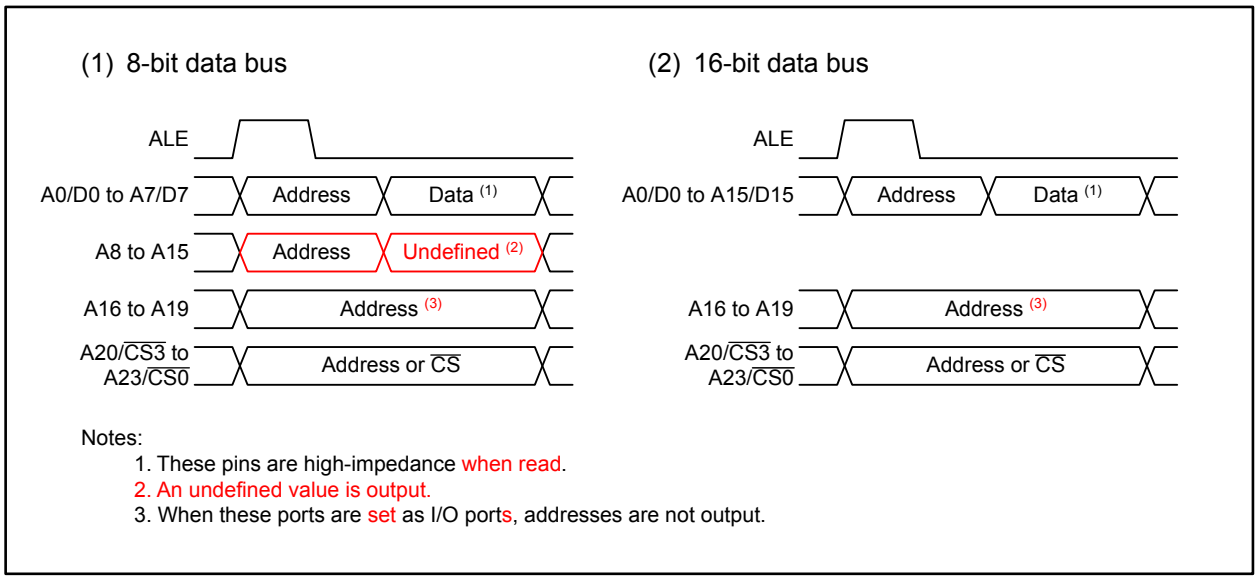
•Pages 110 and 111 of 493, descriptions of Note 2 in Figures 9.6 to 9.8 are corrected as follows:
CB01 register: “The setting value should be equal to or greater than that of the CB12 register.”
CB12 register: “The setting value should be equal to or greater than that of the CB23 register and should be equal to or less than that of the CB01 register.”
CB23 register: “The setting value should be equal to or less than that of the CB12 register.”

•Page 114 of 493, bit names of bits ESUR0 and ESUR1, bits ESUW0 and ESUW1, bits EWR0 and EWR1, and bits EWW0 and EWW1 in Figure 9.11 are modified as follows:
ESUR0 and ESUR1: "Address Setup Cycles Before Read Setting Bit"
ESUW0 and ESUW1: "Address Setup Cycles Before Write Setting Bit"
EWR0 and EWR1: "Read Pulse Width Setting Bit"
EWW0 and EWW1: "Write Pulse Width Setting Bit"

•Page 116 of 493, function of P4_0 to P4_3 "A16 to A19 or I/O ports" for memory expansion mode in Table 9.2 is corrected as follows:
"I/O ports"

•Page 119 of 493, descriptions in the second paragraph of 9.3.5 is corrected as follows:
"Table 9.6 lists the bit setting of MPY1, MPY0, ESUR1, and ESUR0 and the Tsu(A-R) (address setup cycles before read), Table 9.7 lists the bit setting of MPY1, MPY0, EWR1, and EWR0 and the Tw(R) (read pulse width), Table 9.8 lists the bit setting of MPY1, MPY0, ESUW1, and ESUW0 and the Tsu(A-W) (address setup cycles before write), and Table 9.9 lists the bit setting of MPY1, MPY0, EWW1, and EWW0 and the Tw(W) (write pulse width)."

•Page 123 of 493, Figure 9.14 is corrected as follows:



Notes:
1. These pins are high-impedance when read.
2. An undefined value is output.
3. When these ports are set as I/O ports, addresses are not output.

Figure 9.14 ALE Signal and Address Bus/Data Bus

•Page 132 of 493, description of Note 1 of Figure 11.1 is modified as follows:
"The peripheral interrupts are generated by the corresponding peripheral functions in the MCU."

•Page 133 of 493, descriptions in the second paragraph of (5) in 11.2 are corrected as follows:
"The stack pointer (SP) used for this interrupt differs depending on the software interrupt numbers. For software interrupt numbers 0 to 127, when an interrupt request is accepted, the U flag is saved and set to 0 to select the interrupt stack pointer (ISP) during the interrupt sequence. The saved data of the U flag is restored upon returning from the interrupt handler. For software interrupt numbers 128 to 255, the stack pointer does not change during the interrupt sequence."

•Page 135 of 493, description in 11.5 is corrected as follows:
"Each interrupt vector has a 4-byte memory space, in which the start address of the associated interrupt handler is stored. When an interrupt request is accepted, a jump to the address set in the interrupt vector takes place. Figure 11.2 shows an interrupt vector."

•Page 136 of 493, description in the remarks column for the BRK instruction in Table 11.1 is corrected as follows:

"If address FFFFFFE7h is FFh, a jump to the interrupt vector of software interrupt number 0 in the relocatable vector table takes place"

•Page 143 of 493, description for the IR bit below Figure 11.4 is corrected as follows:

"The IR bit becomes 1 (interrupt requested) when an interrupt request is generated; this bit setting is retained until the interrupt request is accepted. When the request is accepted and a jump to the corresponding interrupt vector takes place, the IR bit becomes 0 (no interrupt requested). The IR bit can be set to 0 by a program. This bit should not be set to 1."

•Page 147 of 493, description of Note 1 in Table 11.7 is corrected as follows:

"These are the values when the interrupt vectors are aligned to the addresses in multiples of 4 in the internal ROM. However, the condition does not apply to the fast interrupt."

•Page 150 of 493, Figure 11.8 is corrected as follows:

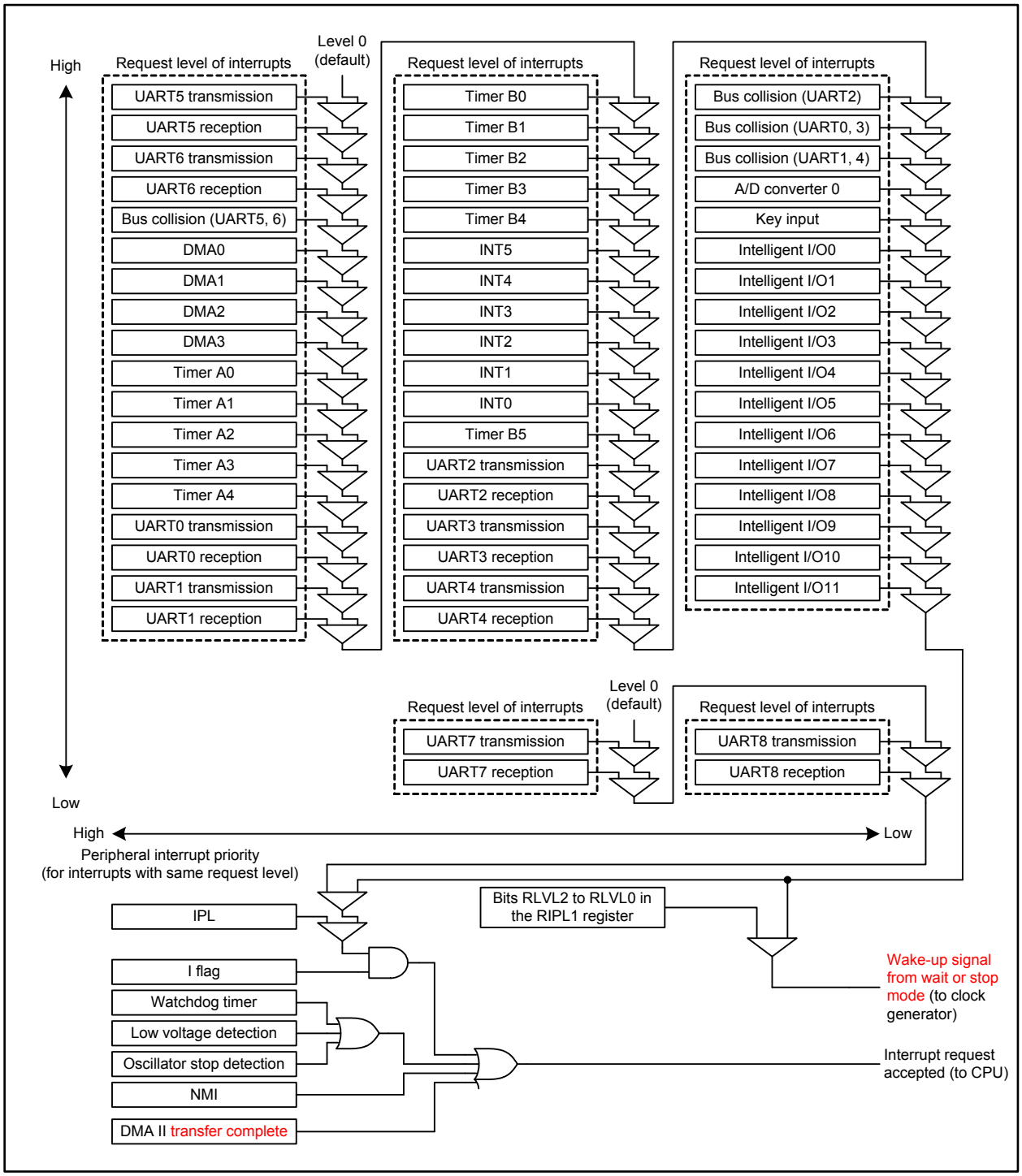


Figure 11.8 Priority Resolver

(Description “Bits RLVL2 to RLVL0 in the RIPL2 register” and associated signal lines are deleted from Figure 11.8)

•Page 152 of 493, Note 1 “This bit should be set to 0 to select the level sensitive input as trigger. To set this bit to 1, the POL bit in the corresponding INTiIC register (i = 6 to 8) should be set to 0 (falling edge).” is deleted from Figure 11.10.

•Page 154 of 493, register symbol “IIOiE” in line 16 of 11.13 is corrected as follows:
“IIOiIE”

•Page 155 of 493, descriptions for b0 and Note 3 in Figure 11.13 are corrected as follows:
b0: "No register bit; this bit is read as 1" ("should be written with 0 and" is deleted)
Note 3: "When this bit is function-assigned, it can only be set to 0. It should not be set to 1. To set it to 0, either the AND or BCLR instruction should be used; when the bit is not function-assigned (reserved), it should be set to 0."

•Page 158 of 493, description in the second paragraph of 12. Watchdog Timer is corrected as follows:
"Select either an interrupt request or a reset with the CM06 bit in the CM0 register for when the watchdog timer underflows. Once the CM06 bit is set to 1 (reset), it cannot be changed to 0 (watchdog timer interrupt) by a program. It can be set to 0 only by a reset."

•Page 159 of 493, the following description is added to Figure 12.2 as Note 1:
"Set this bit before activating the watchdog timer."

•Page 161 of 493, description "a value more than 00000001h" in the Specification column of the DMA transfer startup in Table 13.1 is corrected as follows:
"a value other than 00000000h"

•Page 169 of 493, description in the first paragraph of 13.1 is corrected as follows:
"The transfer cycle is composed of bus cycles to read data from (source read) or to write data to (destination write) memory or an SFR."

•Page 175 of 493, address "FFFFFFFh" in Note 1 of Table 14.1 is corrected as follows:
"FFFFFFFFh"

•Page 175 of 493, bit symbol "IIRLT" in the fifth bullet point of 14.1 is corrected as follows:
"IRLT"

•Page 179 of 493, bit names of the OPER bit and bits CNT0 to CNT2 are modified as follows:
OPER: "Calculation Result Transfer Select Bit"
CNT0 to CNT2: "Number of Transfers Setting Bit"

•Page 180 of 493, addresses "001FFFFFh", "00200000h", and "00000000h" in lines 4 to 5 of the second paragraph in 14.3.1 are corrected as follows:
"01FFFFFFh", "02000000h", and "FE000000h"

•Page 185 of 493, the following ports are added to the 64-pin package in 15. Programmable I/O Ports:
"P6 to P10 (excluding P8_5, P9_0 to P9_2, and P9_4 to P9_7)"

•Page 187 of 493, description "bus control pins" in line 7 of 15.1 and Note 1 of Figure 15.4 is corrected as follows:
"bus control signals"

•Page 189 of 493, Figure 16.2 is corrected as follows:

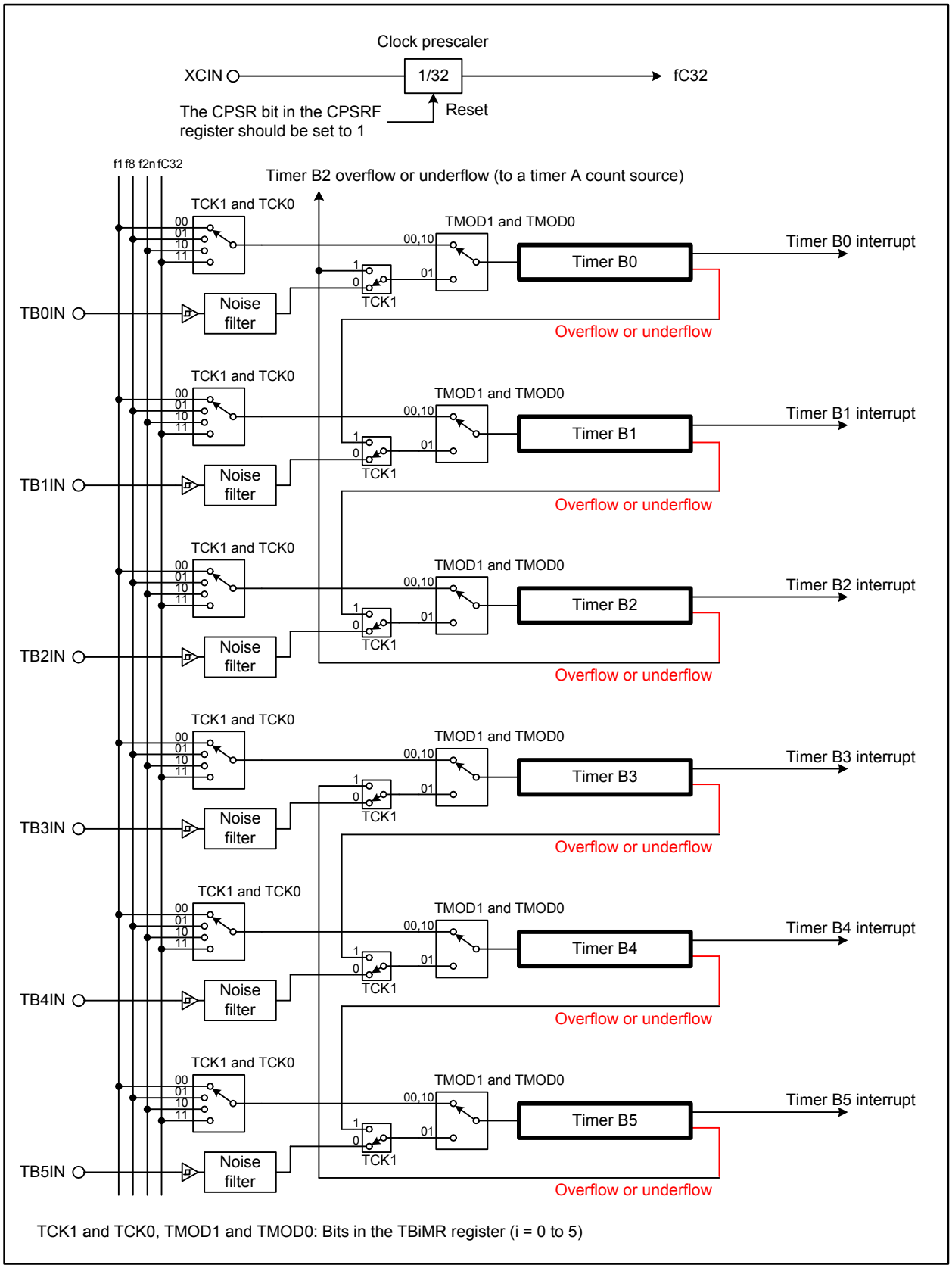


Figure 16.2 Timer B Configuration

•Page 193 of 493, expression “Counting” is deleted from bit names of bits TA0UD to TA4UD and the register name in Figure 16.7

•Page 201 of 493, bit name of the MR2 bit in Figure 16.12 is modified as follows:
"Increment/Decrement Switching Source Select Bit"

•Page 201 of 493, bit symbols "TAiTGH and TAiTGL" in Note 5 of Figure 16.12 are corrected as follows:
"TAjTGH and TAjTGL"

•Page 203 of 493, register symbol "TA4NR" in line 3 of 16.1.3 is corrected as follows:
"TA4MR"

•Page 204 of 493, descriptions of functions of the MR2 bit in Figure 16.15 are modified as follows:
"0: TAiOS bit in the ONSF register is enabled
1: Selected using bits TAiTGH and TAiTGL in the ONSF or TRGSR register"

•Page 206 of 493, descriptions of functions of the MR2 bit in Figure 16.16 are modified as follows:
"0: TAiS bit in the ONSF register is enabled
1: Selected using bits TAiTGH and TAiTGL in the ONSF or TRGSR register"

•Page 220 of 493, expression "TBj interrupt handler" in the eighth bullet point of 16.3.3.3 is corrected as follows:
"timer Bj interrupt handler"

•Page 224 of 493, descriptions of functions of the INV13 bit in Figure 17.3 are corrected as follows:
INV13: "0: Timer A1 reload control signal is 0
1: Timer A1 reload control signal is 1"

•Page 224 of 493, description in Note 1 of Figure 17.3 is corrected as follows:
"This register should be set after the PRC1 bit in the PRCR register is set to 1 (write enabled). This register should be rewritten while timers A1, A2, A4, and B2 are stopped."

•Page 229 of 493, descriptions of functions of bits MR2 and MR3 in Figure 17.8 are corrected as follows:
MR2: "No register bit; should be written with 0 and read as undefined value"
MR3: "Disabled when using the three-phase motor control timers. Should be written with 0 and read as undefined value"

•Page 230 of 493, description of function of the PWCON bit in Figure 17.9 is corrected as follows:
PWCON: "1: The underflow of timer B2 when the reload control signal for timer A1 is 0"

•Page 231 of 493, description "The sum of setting values for registers TAi and TAi1 should be identical to the setting value of the TB2 register in this mode." is deleted from lines 8 to 9 of 17.3

•Page 239 of 493, descriptions in 17.6.2 are corrected as follows:
"Do not write to the TAi1 register (i = 1, 2, 4) before and after timer B2 underflows. Before writing to the TAi1 register, read the TB2 register to verify that sufficient time remains until timer B2 underflows. Then, immediately write to the TAi1 register so no interrupt handling is performed during this write procedure. If the TB2 register indicates little time remains until the underflow, write to the TAi1 register after timer B2 underflows."

•Page 244 of 493, mode "0 1 0 : I^2C mode" for the function of bits SMD0 to SMD2 is deleted from Figure 18.4.

•Page 250 of 493, description of function of the SWC bit in Figure 18.11 is modified as follows:
"0: No wait-state/wait-state cleared
1: Hold the SCLi pin low after the eighth bit is received"

•Page 251 of 493, description “UiBRG count source” in the function of bits DL0 to DL2 in Figure 18.12 is corrected as follows:
“baud rate generator count source”

•Page 252 of 493, description of function of the SWC9 bit in Figure 18.13 is modified as follows:
“0: No wait-state/wait-state cleared
1: Hold the SCLi pin low after the ninth bit is received”

•Pages 252 and 280 of 493, bit symbol “STARREQ” in Note 3 of Figure 18.13 and line 1 of 18.3.2 is corrected as follows:
“STAREQ”

•Page 256 of 493, Note 1 “This bit should be set to 0 to select the level sensitive input as trigger. To set this bit to 1, the POL bit in the corresponding INTiIC register (i = 6 to 8) should be set to 0 (falling edge)” is deleted from Figure 18.19.

•Page 257 of 493, i value “(i = 0 to 6)” in the Specification column of the Transmit/receive clock in Table 18.2 is corrected as follows:
“(i = 0 to 8)”

•Page 260 of 493, description “TXEPT flag” in Figure 18.20 is corrected as follows:
“TXEPT bit”

•Page 260 of 493, bit symbol “UiRS” in the fourth dash of Figure 18.20 is corrected as follows:
“UiIRS”

•Page 267 of 493, bit symbol “SUM0” in the Function column of the UiRB register in Table 18.7 is corrected as follows:
“SUM”

•Pages 268 and 269 of 493, descriptions of functions of the UiIRS bit in Figures 18.25 and 18.26 are corrected as follows:
0: “(an interrupt request is generated when the transmit buffer is empty)”
1: “(an interrupt request is generated when transmission is completed)”

•Pages 272 and 273 of 493, description “Transmit/receive clock” in Figures 18.29 and 18.30 is corrected as follows:
“CLKi”

•Page 304 of 493, description in 19.1.5 is modified as follows:
“In repeat sweep mode 1, the analog voltage applied to eight selected pins including one to four prioritized pins is repeatedly converted into a digital code. Table 19.6 lists specifications of repeat sweep mode 1.”

•Page 304 of 493, description in the specification of the function in Table 19.6 is modified as follows:
“Converts the analog voltage input to a set of eight pins into a digital code repeatedly. One to four pins are converted by priority”

•Page 315 of 493, description “CRC_CCITT” in line 2 of Chapter 21. CRC Calculator is corrected as follows:
“CRC-CCITT”

•Page 315 of 493, Figure 21.1 is corrected as follows:

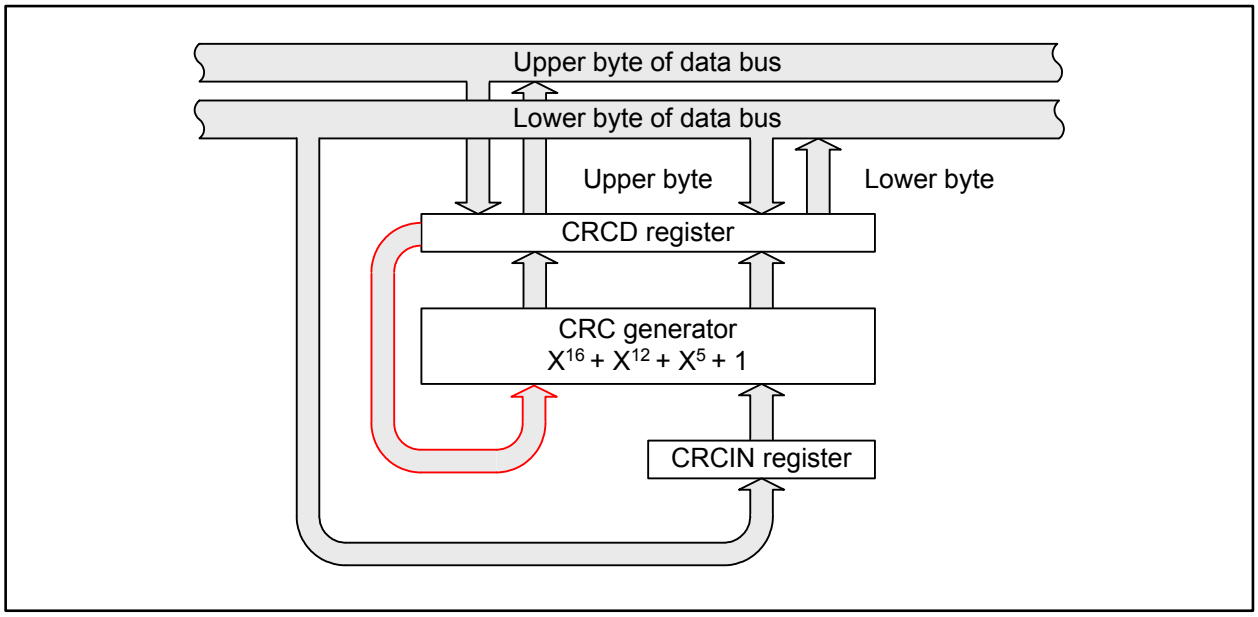


Figure 21.1 CRC Calculator Block Diagram

•Pages 323 and 324 of 493, descriptions "Request from the $\overline{\text{INT0}}$ pin" in Figure 23.1 and "Request from the $\overline{\text{INT1}}$ pin" in Figure 23.2 are corrected as follows:
Figure 23.1: "Request from the $\overline{\text{INT0}}$ pin or the $\overline{\text{INT1}}$ pin"
Figure 23.2: "Request from the $\overline{\text{INT0}}$ pin or the $\overline{\text{INT1}}$ pin"

•Page 325 of 493, pin names "IE_IN/ISRxD2" and "ISTxD2/IE_OUT" in Figure 23.3 are corrected as follows:
"IEIN/ISRXD2" and "ISTXD2/IEOUT"

•Page 328 of 493, descriptions for bits RST2, UD0, and UD1 in Figure 23.6 are modified as follows:

Bit Symbol	Bit Name	Function	RW
RST2	Base Timer Reset Source Select Bit 2	0: No reset 1: Low signal input into the $\overline{\text{INT0}}$/$\overline{\text{INT1}}$ pin (3)	RW

UD0	Increment/Decrement Control Bit	b6 b5 0 0 : Increment mode 0 1 : Increment/decrement mode 1 0 : Two-phase pulse signal processing mode (4) 1 1 : Do not use this combination	RW
UD1			RW

•Page 328 of 493, description of Note 3 in Figure 23.6 is modified as follows:
"The base timer is reset by an input of low signal to the external interrupt input pin selected for the UDiZ signal by the IFS2 register."

•Page 330 of 493, bit symbol "BT3S" in (2) of Note 1 in Figure 23.8 is corrected as follows:
"BT2S"

•Page 331 of 493, Note 3 "The GOC bit becomes 0 after gating is cleared." is deleted from Figure 23.9.

•Page 334 of 493, pin name “ISTxD2” in Note 3 of Figure 23.13 is corrected as follows:
“ISTXD2”

•Page 337 of 493, descriptions in the second bullet point of the specification for the reset conditions in Table 23.2 are corrected as follows:
“An input of low signal into the external interrupt pin ($\overline{INT0}$ or $\overline{INT1}$) as follows:
for group 0: selected using bits IFS23 and IFS22 in the IFS2 register
for group 1: selected using bits IFS27 and IFS26 in the IFS2 register”

•Page 338 of 493, description in the first bullet point in the specification of Table 23.2 is corrected as follows:
“The base timer starts counting when the BTS or BTiS bit is set to 1. When the base timer reaches FFFFh, it starts decrementing. When the RST1 bit in the GiBCR1 register is set to 1 (reset by match with the GiPO0 register), the timer counter starts decrementing two counts after the base timer value matches the GiPO0 register setting. When the timer counter reaches 0000h, it starts incrementing again (refer to Figure 23.20).”

•Page 338 of 493, description “Low signal input to the $\overline{INTi}$ pin” in Figure 23.18 is corrected as follows:
“Low signal input to the $\overline{INT0}$/$\overline{INT1}$ pin”

•Pages 349, 351, and 354 of 493, description “Input to the IIOi_j pin” in Figures 23.25 to 23.27 is corrected as follows:
“IIOi_j pin”

•Page 355 of 493, descriptions of variables for the output waveform in Table 23.10 are corrected as follows:
“n: G2POj register (j = 0 to 7) setting value (6 upper bits), 00h to 3Fh
m: G2POj register setting value (10 lower bits), 000h to 3FFh”

•Page 356 of 493, expressions “fBTi” and “G2POCR” in Figure 23.28 are corrected as follows:
“fBT2” and “G2POCRj”

•Pages 356 and 358 of 493, description “Input to the OUTC2_j pin” in Figures 23.28 and 23.30 is corrected as follows:
“OUTC2_j pin”

•Page 358 of 493, description “Bits RST2 to RST0 in the G2BCR1 register are set to 000b (base timer is not reset)” in the second dash is deleted from Case 1 in Figure 23.30

•Page 363 of 493, bit names of bits OPOL and IPOL in Figure 23.36 are corrected as follows:
OPOL: “ISTXD2 Output Polarity Switching Bit”
IPOL: “ISRXD2 Input Polarity Switching Bit”

•Page 367 of 493, pin name “ISRX2” for the IPOL bit in the G2CR register in Table 23.15 is corrected as follows:
“ISRXD2”

•Page 369 of 493, description in the second paragraph of 24. I/O Pins is corrected as follows (refer to TN_16C_A198A/E):
“The pull-up resistors are enabled for every group of four pins. However, a pull-up resistor is separated from other peripheral functions even if it is enabled, when a pin functions as an output pin.” (“or an analog I/O pin” is deleted)

•Page 369 of 493, Figure 24.1 is corrected as follows (refer to TN_16C_A198A/E):

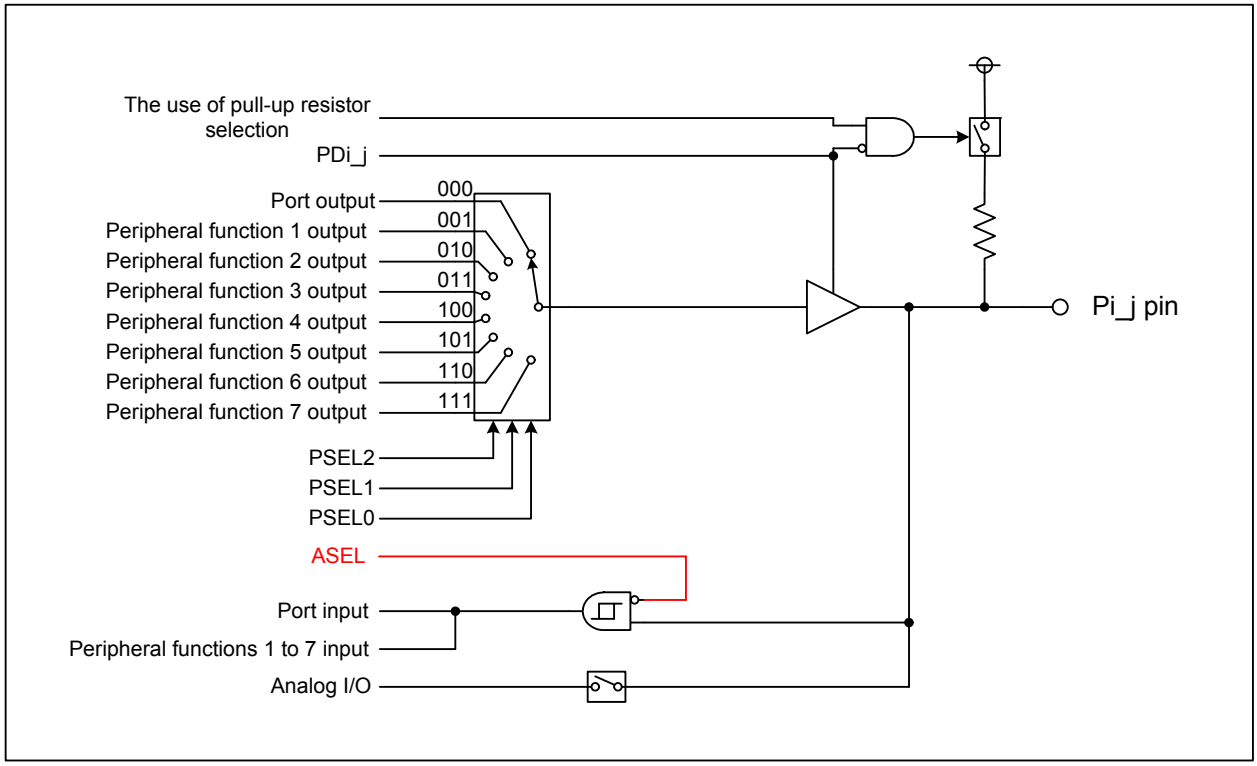


Figure 24.1 Typical I/O Pin Block Diagram (i = 0 to 10; J = 0 to 7)

•Page 370 of 493, description “bus control pins” in line 4 of 24.1 and Note 1 of Figure 24.2 is corrected as follows:
“bus control signals”

•Page 377 of 493, description “PD3_i register” in line 5 below Figure 24.8 is corrected as follows:
“PD3_i bit”

•Page 380 of 493, pin name “OUTC_1” in Figure 24.11 is corrected as follows:
“OUTC2_1”

•Page 383 of 493, bit symbol “PD_9i” in line 8 below Figure 24.14 is corrected as follows:
“PD9_i”

•Page 399 of 493, descriptions in Table 25.3 are corrected as follows:

Protection Type	Lock Bit Protection	ROM Code Protection	ID Code Protection
Protected operations	Erase, write	Read, write	Read, erase, write

(Deleted description “erase” from the ROM Code Protection column)

Protection deactivated by	Setting the LBD bit in the FMR register to 1 (lock bit protection disabled), or by erasing the blocks whose lock bits are set to 0 to permanently deactivate the protection	Erasing all blocks whose protect bits are set to 0	Inputting a proper ID code to the serial programmer

(Deleted description “by using the serial programmer” from the ROM Code Protection column)

•Page 399 of 493, description “use the serial programmer to” in line 3 of 25.2.2 is deleted.

•Page 400 of 493, address “FFFFFE8h” in line 9 of 25.2.3 is corrected as follows:
“FFFFFFE8h”

•Page 401 of 493, description of the second paragraph in 25.2.5 is corrected as follows:
“When the ROM code protection is activated and ID codes corresponding to “Protect” are programmed, the serial programmer cannot deactivate the ROM code protection. In this case, the flash memory is not accessible from the outside of MCU, except that the parallel programmer can delete the flash memory.”

•Page 403 of 493, descriptions in Table 25.7 are corrected as follows:

Restrictions on software commands	None	• Do not execute either the program command or the block erase command for blocks where the rewrite control programs are written to • Do not execute the enter read status register mode command • Execute the enter read lock bit status mode command in RAM • Execute the enter read protect bit status mode command in RAM

Flash memory state detection by	• Reading the FMSR0 register by a program • Executing the enter read status register mode command to read data	• Reading the FMSR0 register by a program

•Page 409 of 493, descriptions in Table 25.8 are corrected as follows:

Item	CPU Operating Mode	
	Single-chip mode	Memory expansion mode
CB01 register	Hold the reset value 00h	Setting range: 02h to F8h Set a value equal to or greater than that of the CB12 register
CB12 register	Hold the reset value 00h	Setting range: 02h to F8h Set a value equal to or greater than that of the CB23 register and equal to or less than that of the CB01 register
CB23 register	Hold the reset value 00h	Setting range: 02h to F8h Set a value equal to or less than that of the CB12 register

•Pages 410 and 412 of 493, descriptions in Figures 25.12 and 25.13 are corrected as follows:

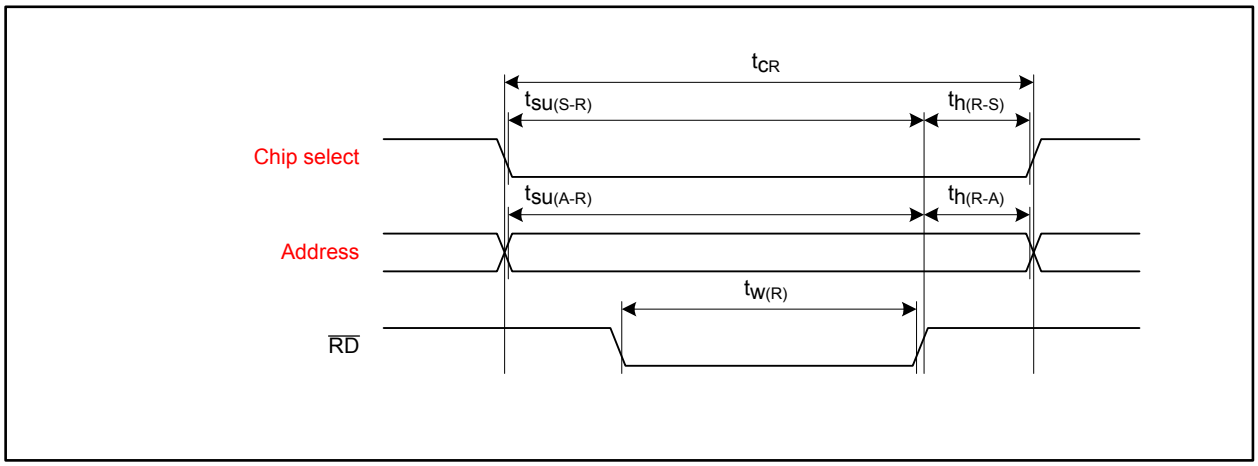


Figure 25.12 Read Timing

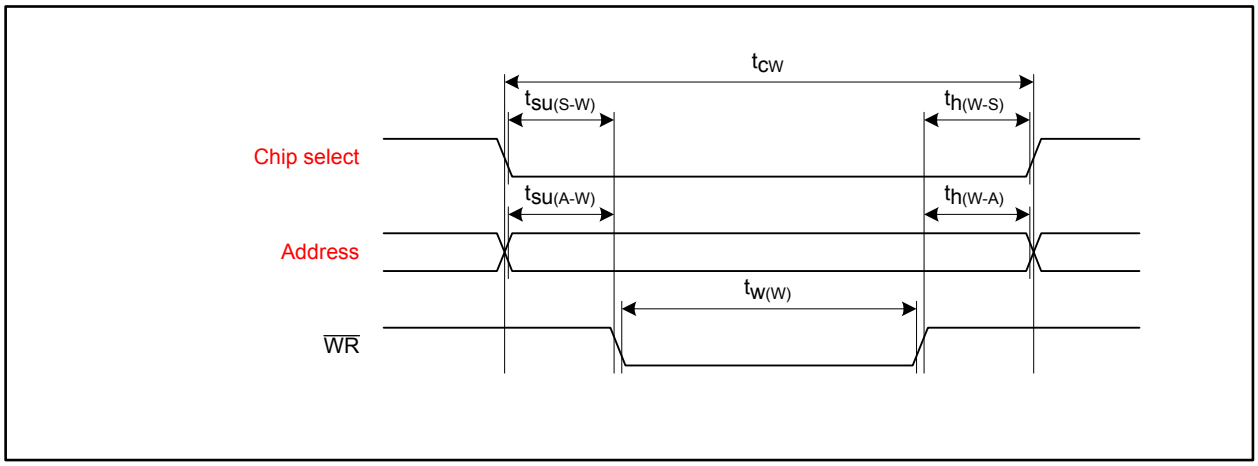


Figure 25.13 Write Timing

•Page 424 of 493, power supply “VCC2” for ports P6_0 to P6_7 in Table 25.21 is corrected as follows:
“VCC1”

•Page 438 of 493, descriptions in Table 26.8 are corrected as follows:

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
—	Program and erase cycles (1)	Program area	1000			Cycles
		Data area	10000			Cycles

•Page 438 of 493, descriptions in Note 1 of Table 26.8 are corrected as follows:
"Program/erase definition
The value represents the number of erasures per block.
When the number of program and erase cycles is n, each block can be erased n times.
For example, if a 4-word write is performed in 512 different addresses in the 4-Kbyte block A and then the block is erased, this is counted as a single program/erase operation.
However the same address cannot be written to more than once per erasure (overwrite disabled)."

•Page 441 of 493, descriptions in Figure 26.5 are corrected as follows:

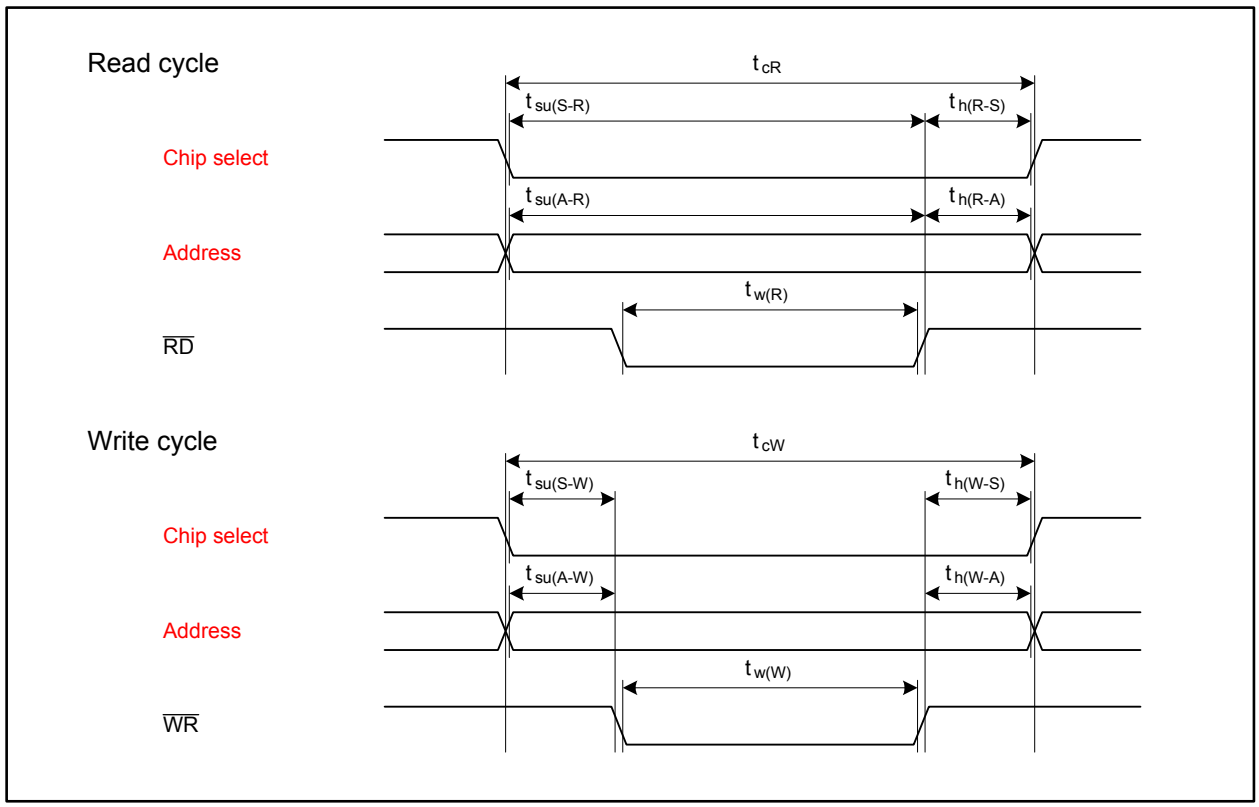


Figure 26.5 Flash Memory CPU Rewrite Mode Timing

•Page 472 of 493, register name "Increment/decrement counting select register" in Table 27.1 is corrected as follows:
"Increment/decrement select register"

•Page 480 of 493, expression "TBj interrupt handler" in the eighth bullet point of 27.7.3.3 is corrected as follows:
"timer Bj interrupt handler"

•Page 481 of 493, descriptions in 27.8.2 are corrected as follows:

"Do not write to the TAi1 register (i = 1, 2, 4) before and after timer B2 underflows. Before writing to the TAi1 register, read the TB2 register to verify that sufficient time remains until timer B2 underflows. Then, immediately write to the TAi1 register so no interrupt handling is performed during this write procedure. If the TB2 register indicates little time remains until the underflow, write to the TAi1 register after timer B2 underflows."