To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-16C-A181A/E	Rev.	1.00
Title	Errata to R32C/111 Group Hardware Manual No. 2		Information Category	Technical Notification		
Applicable Product	R32C/111 Group	Lot No.	Reference Document	R32C/111 Group Hardware Manual Rev. 1.00 (REJ09B0424-0100) Technical Update TN-16C-A174A/E		

This document describes corrections to the R32C/111 Group Hardware Manual, Rev. 1.00.
The corrections indicated in red list as follows:

- Pages 39 to 41 of 464, description of register name “Port Pi_j Port Function Select Register” (i = 0 to 10, j = 0 to 7) in Tables 4.20 to 4.22 is corrected as follows:
  “Port Pi_j Function Select Register”

- Page 43 of 464, description of register name “DMAi Request Source Select Register 1” (i = 0 to 3) in Table 4.24 is corrected as follows:
  “DMAi Request Source Select Register”

- Page 59 of 464, description of a figure number “Figure 8.3” in line 7 of “8.1 Clock Generator Type” is corrected as follows:
  “Figure 8.2”

- Page 89 of 464, description of a peripheral bus width “Peripheral data bus (16-bit)” in Figure 9.1 is corrected as follows:
  “Peripheral data bus (16-/32-bit)”

- Page 90 of 464, description in line 1 of “9.2 Peripheral Bus Timing Setting” is corrected as follows:
  “The peripheral bus of 16-/32-bit width operates at a frequency up to 32 MHz (the theoretical value and the maximum frequency of each product group are as defined by f(BCLK) in 26. “Electrical Characteristics”).”

- Page 91 of 464, description in line 1 of “9.3 External Bus Setting” is corrected as follows:
  “External bus of 8-/16-bit width operates at a frequency up to 32 MHz (the theoretical value and the maximum frequency of each product group are as defined by f(BCLK) in 26. “Electrical Characteristics”).”

- Page 93 of 464, description of register names “CS Output Pin Setting Register 0” in Figure 9.4 and “CS Output Pin Setting Register 1” in Figure 9.5 are respectively corrected as follows:
  “Chip Select Output Pin Setting Register 0” and “Chip Select Output Pin Setting Register 1”

- Page 101 of 464, description “$\overline{\text{WR0}}$” in Table 9.4 is corrected as follows:
  “$\overline{\text{WR1}}$”

- Page 101 of 464, description “$\overline{\text{WR0}}$” in Table 9.5 is corrected as follows:
  “$\overline{\text{BC0}}$”

•Pages 125 and 126 of 464, description of bit name “Interrupt Request Bit” in Figures 11.3 and 11.4 is corrected as follows:

“Interrupt Request Flag”

•Page 133 of 464, description of bit symbols “Bits RLVL02 to RLVL00” and “Bits RLVL12 to RLVL10” in Figure 11.8 are respectively corrected as follows:

“Bits RLVL2 to RLVL0 in the RIPL1 register” and “Bits RLVL2 to RLVL0 in the RIPL2 register”

•Pages 138 and 139 of 464, description of register names ”Intelligent I/O Interrupt Request Register” in Figure 11.13, and “Intelligent I/O Interrupt Enable Register” in Figure 11.14 are corrected as follows:

“Intelligent I/O Interrupt Request Register i (i = 0 to 11)” and “Intelligent I/O Interrupt Enable Register i (i = 0 to 11)”, respectively, in addition to that, variables “i”s, “j”s, and “k”s for description of bits in these figures are changed as follows:

“x”s, “y”s, and “z”s, respectively

•Pages 140 and 449 of 464, description “PR2 register” in lines 4 to 5 of “11.14.1 ISP Setting” and lines 4 to 5 of “27.5.1 ISP Setting” is corrected as follows:

“PM2 register”

•Page 145 of 464, description lines 1 to 3 of “13. DMAC” is corrected as follows:

“More concretely, they are a write access to the DSR bit in the DMiSL2 register (i = 0 to 3) and an interrupt request output from a function specified in bits DSEL4 to DSEL0 in the DMiSL register, and in bits DSEL 24 to DSEL20 in the DMiSL2 register.”

•Page 149 of 464, description of Note 2 in Figure 13.4 is partially deleted as follows:

“This bit should be set after all other DMAC-associated registers are set.” (The second sentence is deleted).

•Page 149 of 464, description is added as Note 3 for bits BWi0, BWi1, USAi, and UDAi in Figure 13.4 as follows:

“Set bits MDi1 and MDi0 to 00b before rewriting these bits.”

•Page 149 of 464, description of Note 2 in Figure 13.5 is corrected as follows:

“When this register is set to 000000h, any new DMA transfer request is unacceptable.”

•Page 149 of 464, description of Note 3 in Figure 13.5 is deleted

•Pages 157 and 450 of 464, description of notes on “13.4.1 DMAC-associated Register Settings” and “27.6.1 DMAC-associated Register Settings” is corrected as follows:

“•Set the DMAC-associated registers while bits MDi1 and MDi0 (i = 0 to 3) in the DMDi register are 00b (DMA transfer disabled). Then, set bits MDi1 and MDi0 to 01b (single transfer) or 11b (repeat transfer) at the end of the setup procedure. This procedure is also applied to rewriting bits UDAi, USAi, and BWi1 and BWi0 in the DMDi register.

•In case the DMAC-associated registers are to be rewritten while DMA transfer is enabled, disable the peripheral function as DMA request source so that no DMA transfer request is generated, then set bits MDi1 and MDi0 in the DMDi register of the corresponding channel to 00b (DMA transfer disabled).

•Once a DMA transfer request is accepted, DMA transfer cannot be disabled even if setting bits MDi1 and MDi0 in the DMDi register to 00b (DMA transfer disabled). Do not change the settings of any DMAC-associated registers other than bits MDi1 and MDi0 until the DMA transfer is completed.

•Wait six or more peripheral clocks to set bits MDi1 and MDi0 in the DMDi register to 01b (single transfer) or 11b (repeat transfer) after setting registers DMiSL and DMiSL2."

•Page 158 of 464, description "64 Kbyte-space" in Table 14.1 is corrected as follows:
"64-Mbyte space"

•Page 163 of 464, description "FE00000000h" in line 3 of "14.3 Transfer Data" is corrected as follows:
"FE000000h"

•Page 163 of 464, description "Any interrupt cannot be accepted during data transfer." in line 8 of "14.3.3 Calculation Transfer" is deleted.

•Page 164 of 464, description after line 3 of "14.4.2 Burst Transfer", "No interrupt is accepted during burst transfer being performed." is added.

•Page 164 of 464, description of values "CADR1 and CADR0" in (2) of "14.4.4 Chained Transfer" is corrected as follows:
CADR.

•Page 165 of 464, description of values "CADR1 and CADR0" in Figure 14.4 is corrected as follows:
CADR.

•Page 165 of 464, description "IADR1 and IADR0" in line 2 of "14.4.5 End-of-transfer Interrupt" is corrected as follows:
IADR.

•Page 171 of 464, description "TAiGH" and "TAiGL" in Figure 16.1 is corrected as follows:
"TAiTGH" and "TAiTGL", respectively

•Page 173 of 464, description "TBiS bit" as an input of an AND gate in Figure 16.3 is corrected as follows:
"TAiS"

•Page 188 of 464, description "FEh" as value of m for "8-bit PWM" in Table 16.5 is corrected as follows:
"FFh"

•Page 189 of 464, description of reset value in Figure 16.16 is corrected as follows:
"0000 0000b"

•Page 192 of 464, description for the title of Figure 16.21 is corrected as follows:
"Registers TB0MR to TB5MR"

•Page 206 of 464, description of RW symbol for INV05 bit in Figure 17.2 is corrected as follows:
"RO"

•Page 209 of 464, description of reset value in Figure 17.5 is corrected as follows:
"XX11 1111b"

•Page 212 of 464, description of reset value in Figure 17.8 is corrected as follows:
"00XX 0000b"

•Pages 224 and 225 of 464, description “CRS” in Figures 18.1 and 18.2 is deleted

•Page 234 of 464, description of Note 2 in Figure 18.12 is corrected as follows:
“To use the SS function, the CRD bit in the UiC0 register”

•Page 258 of 464, a circuit for bits ACKD and ACKC is added to Figure 18.31

•Page 270 of 464, description “$\overline{SS}$ pin” in the title of Figure 18.37 is corrected as follows:
“$\overline{SSi}$ pin”

•Pages 273 and 455 of 464, description of the third bullet point in “18.5.2.2 Receive Operation” and “27.9.2.2 Receive Operation” as below is deleted
“•The following two conditions must be satisfied to use continuous receive mode (UiRRM bit in the U0C1 register is set to 1).
- The CKDIR bit in the UiMR register is set to 1 (external clock selected)
- The RTS function is not enabled
To receive data continuously under other conditions, set the UiRRM bit to 0 (continuous receive mode disabled), and write dummy data to the UiTB register every time a receive operation is completed.”

•Page 304 of 464, description “BT0R: Bit in the IIO7IR register” is added to Figure 23.1

•Page 305 of 464, description “BT1R: Bit in the IIO4IR register” is added to Figure 23.2

•Page 306 of 464, description “BT2R, PO2jR, IE0R to IE2R, SIO2TR, SIO2RR: registers IIO3IR and IIO5IR to IIO11R” is added to Figure 23.3

•Page 306 of 464, description of note symbol “(3)” in Figure 23.3 is deleted

•Pages 336, 338, and 340 of 464, description of variable “i”s in “23.3.4 Bit Modulation PWM Output Mode (for Group 2)”, “23.3.5 Real-Time Port Output Mode (RTP Output Mode) (for Group 2)”, and “23.3.6 Parallel Real-Time Port Output Mode (RTP Output Mode) (for Group 2)” is corrected as follows:
“fBT2”, “G2FE register”, “G2BCR1 register”, “PO2jR bit”, “G2POCR register”, and “G2POj register”

•Page 341 of 464, description of bit symbols in Figure 23.32 is corrected as follows:
“PO20R bit”, “PO21R bit”, and “PO22R bit”

•Page 394 of 464, description “FFFF800h” in line 3 of “25.3.5.5 Block Erase Command” is corrected as follows:
“FFFFF800h”

•Pages 403 and 458 of 464, description of the third bullet point of EW1 mode in “25.6.5 Notes on Interrupts” and “27.11.5 Notes on Interrupts” is corrected as follows:
“When the interrupt handler has ended, set the EWM bit in the FMR0 register to 1 (set as EW1 mode) and the LBD bit in the FMR1 register to 1 (lock bit protection disabled) to re-execute the rewrite operation.”

•Page 413 of 464, typical and maximum values for $f_{SO(PLL)}$ in Table 26.12 “Electrical Characteristics of Oscillator” are corrected as follows:

Symbol	Characteristic	Measurement condition	Value			Unit
			Min.	Typ.	Max.	
$f_{SO(PLL)}$	PLL clock self-oscillation frequency		35	55	80	MHz

•Pages 424 and 436 of 464, respective minimum values for $t_{w(ADH)}$ in Tables 26.31 and 26.54 “A/D Trigger Input” are corrected as follows:

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{w(ADH)}$	$\overline{\text{ADTRG}}$ input high level pulse width Hardware trigger input high level pulse width	$\frac{3}{\phi_{AD}}$		ns

•Pages 426 and 438 of 464, description of “Characteristic” for $t_{su(S\text{-}ALE)}$ in Tables 26.35 and 26.58 “External Bus Timing (Multiplexed bus)” is corrected as follows:

“Chip-select setup time for ALE”

•Page 433 of 464, description of symbols “$t_{w(H)}$,” “$t_{w(L)}$”, “t_r”, and “t_f” in “Table 26.43 External Clock Input” is corrected as follows:

“$t_{w(XH)}$”, “$t_{w(XL)}$”, “$t_{r(X)}$”, and “$t_{f(X)}$”