To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-16C-A174A/E	Rev.	1.00
Title	Errata to R32C/111 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	R32C/111 Group	Lot No.	Reference Document	R32C/111 Group Hardware Manual Rev. 1.00 (REJ09B0424-0100)		

This document describes corrections to the R32C/111 Group Hardware Manual, Rev. 1.00.
The corrections indicated in red list as follows:

- Page 51 of 464, description in Figure 6.3 “Low Voltage Detector Block Diagram” is corrected as follows:
  “VDEN, LVDIEN, LVDF, VMF: Bits in the LVDC register”

- Page 62 of 464, description for the CM02 bit in Figure 8.3 “CM0 Register” is corrected as follows:

Bit Symbol	Bit Name	Function	RW
CM02	Peripheral Clock Source Stop Bit (3)	0: Peripheral clock source not stopped in wait mode 1: Peripheral clock source stopped in wait mode (4)	RW

- Page 62 of 464, description of Note 4 in Figure 8.3 is corrected as follows:
  “fC32 and f2n whose clock source is main clock do not stop.”

- Page 71 of 464, lines 19 to 21, description in “8.1.3 PLL Clock” is corrected as follows:
  “The waiting time of $t_{LOCK(PLL)}$ is required after changing the setting until the PLL clock oscillation has stabilized while the main clock oscillation is stable.“

- Page 75 of 464, lines 5 and 6 of (1), description in “8.5 Peripheral Clock” is corrected as follows:
  “f1, f8, f32, and f2n whose clock source is peripheral clock source stop in low power mode or when the CM02 bit is set to 1 (peripheral clock source stopped in wait mode) to enter wait mode.”

- Page 84 of 464, lines 8 and 9, description in “8.7.2.4 Exiting Wait Mode” is corrected as follows:
  “When this bit is set to 1 (peripheral clock source stopped in wait mode), peripheral functions using f1, f8, f32, f2n (when the clock source is the peripheral clock source), or fAD stop operating.”

- Page 87 of 464, the whole description of “8.9.2.1 Wait Mode” is deleted.

- Page 87 of 464, description of the first bullet in “8.9.2.2 Stop Mode” is deleted.

- Page 130 of 464, Table 11.7 “Interrupt Sequence Execution Time” is corrected as follows:

Interrupt	Execution Time in Terms of CPU clock
Peripheral	13 + α cycles (2)
INT instruction	11 cycles
NMI	10 cycles
Watchdog timer Oscillator stop detection Low voltage detection	11 cycles
Undefined instruction	12 cycles
Overflow	12 cycles
BRK instruction (relocatable vector table)	16 cycles
BRK instruction (fixed vector table)	19 cycles
BRK2 instruction	19 cycles
Fast interrupt	11 cycles

•Page 132 of 464, the priority order in 11.8 “Interrupt Priority” is corrected as follows:

Watchdog timer
Reset > Oscillator stop detection > NMI > Peripherals
Low voltage detection

•Page 146 of 464, description of Note 1 in Figure 13.3 “Registers DM0SL2 to DM3SL2” is corrected as follows:

“The bit settings of bits DSEL24 to DSEL20 should be changed while bits MDi1 and MDi0 in the DMDi register of the corresponding channel are set to 00b (DMA transfer disabled).”

•Page 160 of 464, description in Figure 14.2 “DMAC II Index” is corrected as follows:

“For example, when the calculation transfer is not used, the transfer destination address should be set to BASE + 8.”

•Page 259 of 464, description in Table 18.10 “Register Settings in I^2C Mode (i = 0 to 6)” is corrected as follows:

UiC1	7 to 5	Set the bits to 000b
	UiIRS	Set the bit to 1

•Page 368 of 464, description of Note 1 in Figure 24.18 “PUR1 Register” is corrected as follows:

“However, the pull-up resistors are enabled for ports P4_0 to P4_3 when these pins function as the I/O ports with 8-bit bus or multiplexed bus format.”

•Page 382 of 464, description for the FCA bit in Figure 25.7 “FMR0 Register” is corrected as follows:

Bit Symbol	Bit Name	Function	RW
FCA	Final Command Accept Busy Flag	0: Final command accept ready 1: Final command accept busy	RO

•Pages 393 to 397 of 464, flowcharts in Figures 25.14 to 25.18 are corrected as follows:

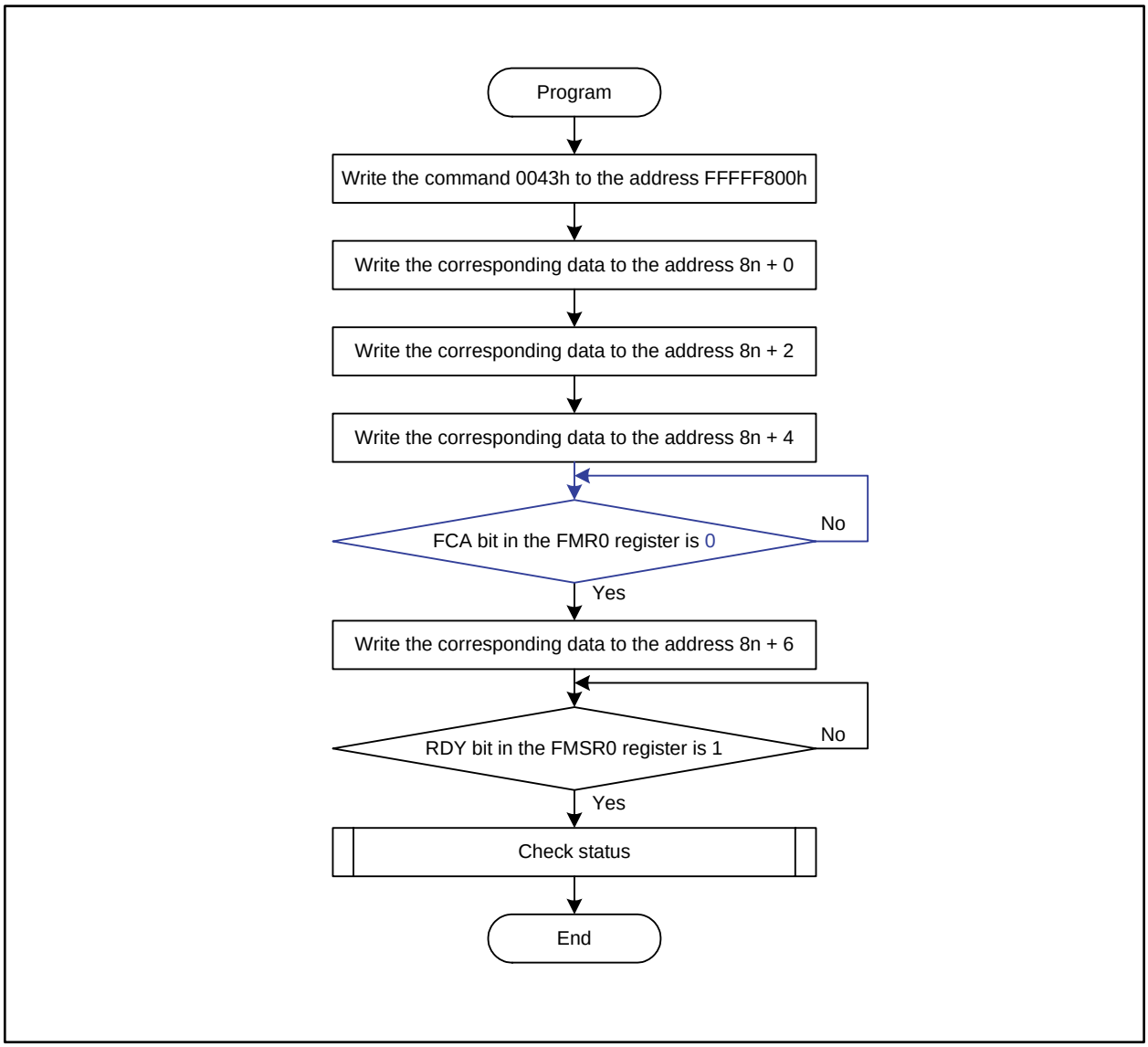

Figure 25.14 Program Command Flow

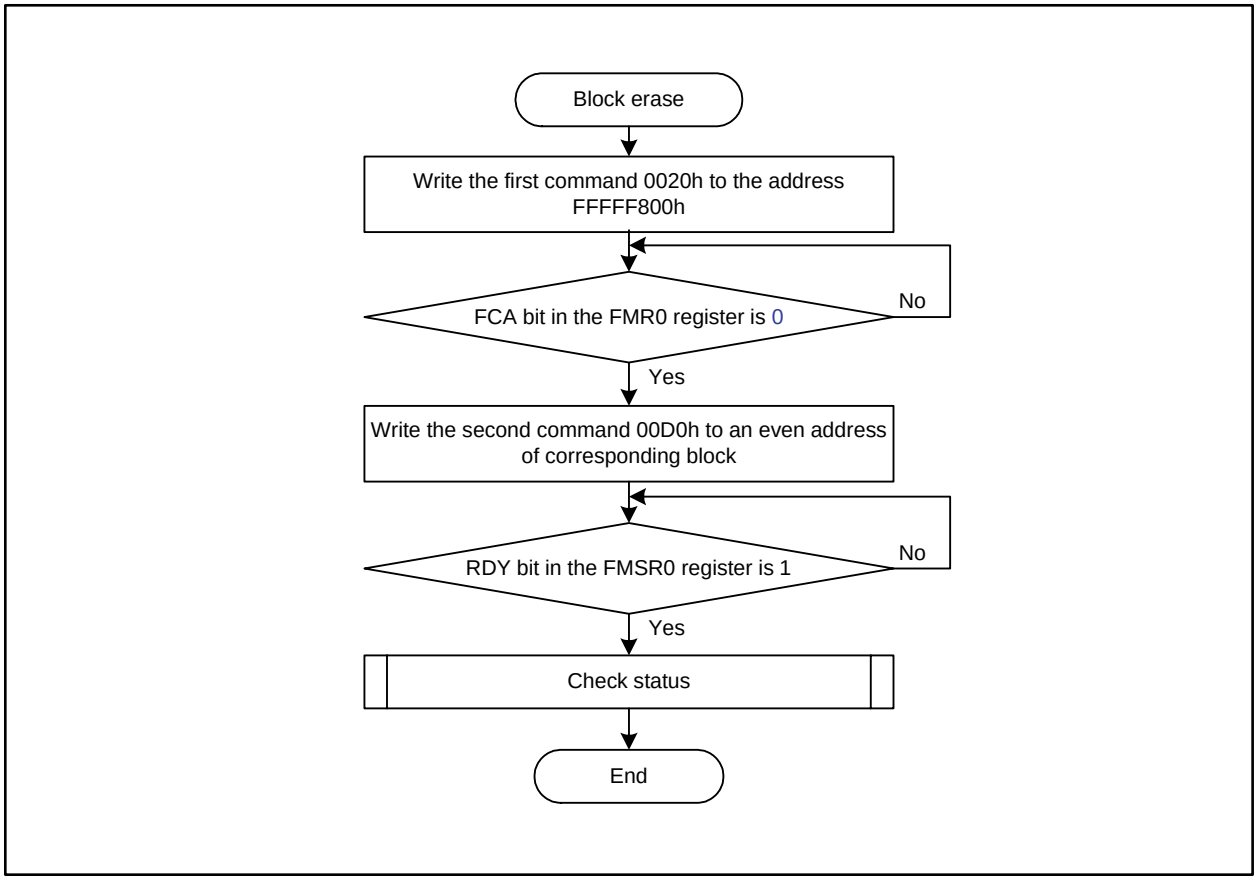

Figure 25.15 Block Erase Command Flow

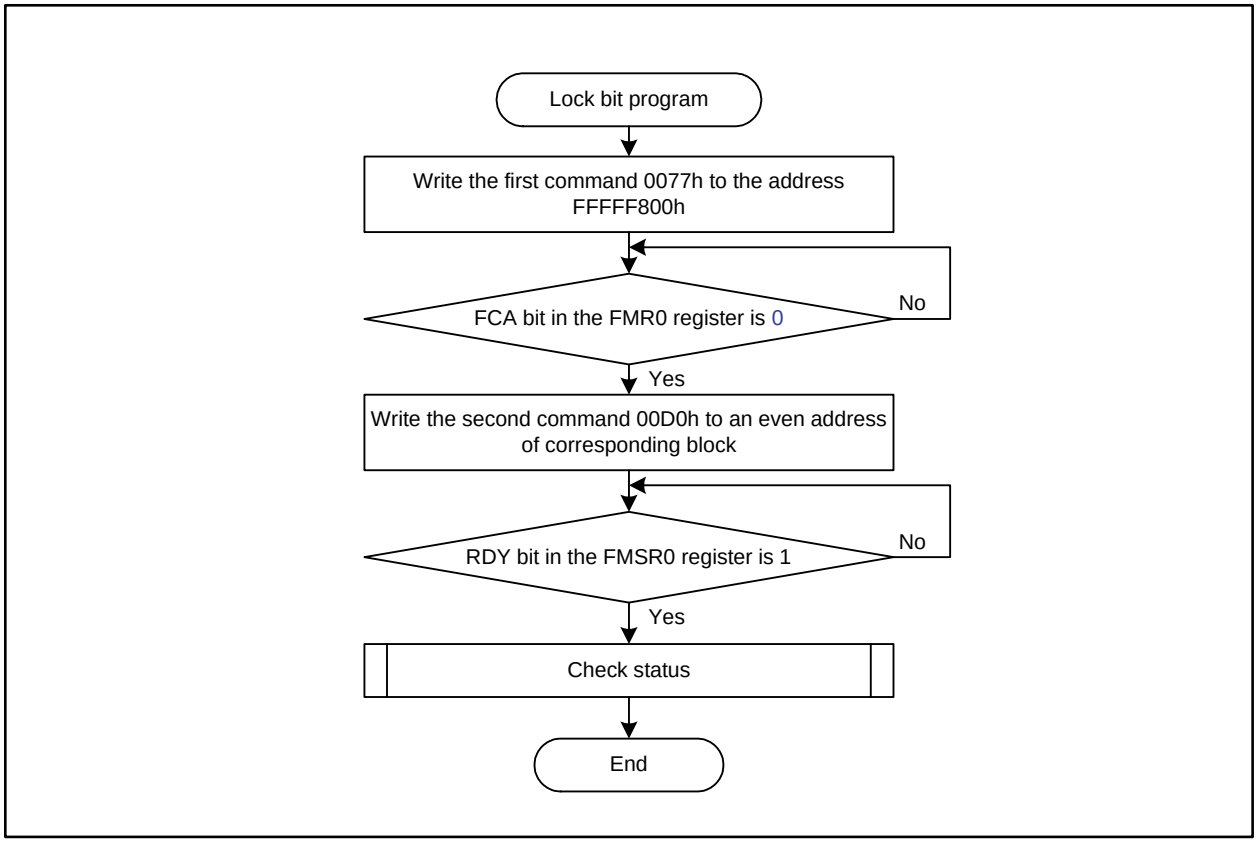

Figure 25.16 Lock Bit Program Command Flow

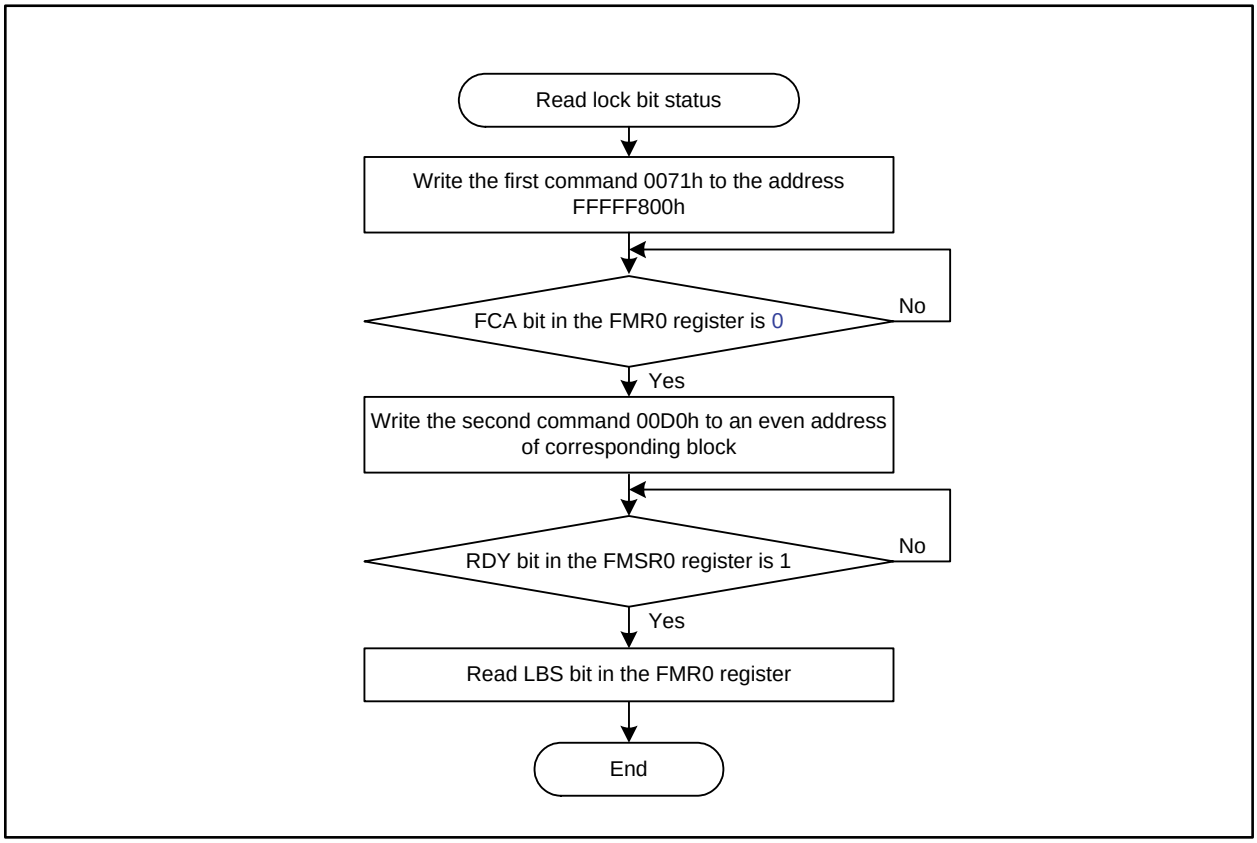

Figure 25.17 Read Lock Bit Status Command Flow

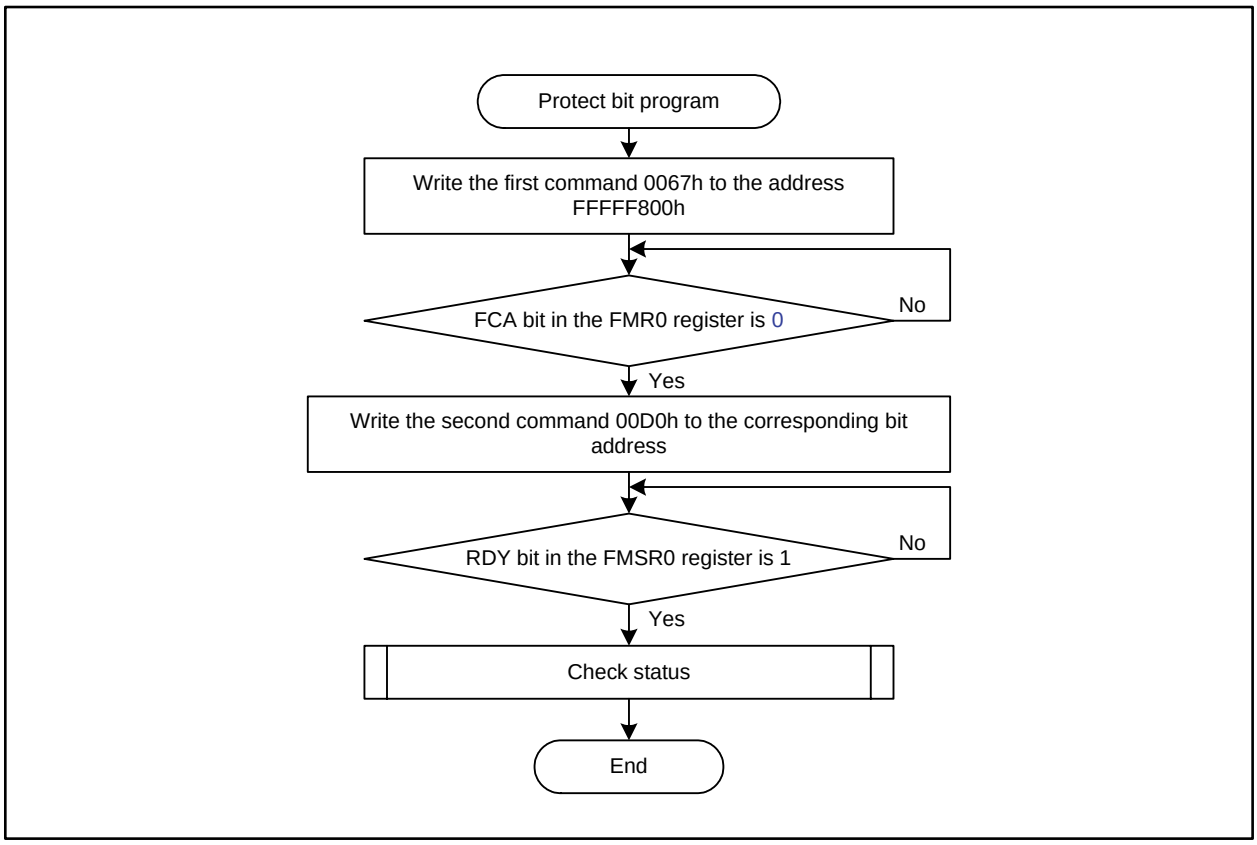

Figure 25.18 Protect Bit Program Command Flow

•Pages 424 and 436 of 464, respective minimum values for tsu(D-C) in Tables 26.30 and 26.53 “Serial Interface” are corrected as follows:

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{su(D-C)}$	RXDi input setup time	80		ns

•Pages 426 and 438 of 464, respective minimum values for th(W-D) in Tables 26.35 and 26.58 “External Bus Timing (Multiplexed bus)” are corrected as follows:

Symbol	Characteristic	Measurement condition	Value		Unit
			Min.	Max.	
$t_{h(W-D)}$	Data hold time after write	Refer to Figure 26.6	$0.5 \times t_{c(Base)}$		ns

•Page 446 of 464, the whole description of “27.3.2.1 Wait Mode” is deleted.

•Page 446 of 464, description of the first bullet in “27.3.2.2 Stop Mode” is deleted.