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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0072A/E	Rev.	1.00
Title	Errata to LVL bit setting value for Serial Communications Interface channels 0, 1 and Ethernet MAC controller of Direct Memory Access Controller of RZ/A2M Group Products		Information Category	Technical Notification		
Applicable Product	RZ/A2M Group	Lot No. All	Reference Document	RZ/A2M Group User's Manual: Hardware Rev.3.00 (R01UH0746EJ0300)		

This document describes corrections to LVL bit setting value for the Serial Communications Interface channels 0, 1 and Ethernet MAC controller of Direct Memory Access Controller of the RZ/A2M group.

[LVL bit setting value (after change)]

Table 9.4 On-Chip Module Requests

DMA Transfer Request Source	DMA Transfer Request Signal	Transfer Source	Transfer Destination	DMARSn/nS		CHCFG_n/nS *1						
				MID	RID	TM	AM[2:0]	LVL	HIEN	LOEN	REQD	SEL[2:0]
Serial communication interface channel 0	RXI0 (Receive FIFO data full)	RDR0	Arbitrary	1011_1000	10	0	010	0	1	0	0	Ch0:000 Ch1:001 Ch2:010 Ch3:011 Ch4:100 Ch5:101 Ch6:110 Ch7:111 Ch8:000 Ch9:001 Ch10:010 Ch11:011 Ch12:100 Ch13:101 Ch14:110 Ch15:111
	TXI0 (Transmit FIFO data empty)	Arbitrary	TDR0	1011_1000	01	0	010	0	1	0	1	
Serial communication interface channel 1	RXI1 (Receive FIFO data full)	RDR1	Arbitrary	1011_1001	10	0	010	0	1	0	0	
	TXI1 (Transmit FIFO data empty)	Arbitrary	TDR1	1011_1001	01	0	010	0	1	0	1	
Ethernet MAC controller	IPLS (pulse timer output detection)	Arbitrary	Arbitrary	1011_1010	11	0	001	0	1	0	0/1	