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Tì	tle	The e charao Produ	rrata of DAC, ADC and Electrical cteristics on the RA6T2 Group MC cts	U	Information Category	Technical Notification					
				Lot No.							
Appli	cable	DAGT	2 Group		Reference	RA6T2 Group User's Manual :					
Pro	duct	RAU I	2 Group	All	Document	Hardware Rev.1.30					
This document describes the errata of DAC, ADC and Electrical characteristics in the RA6T2 Group User's											
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Table 36.2 Association between ADC functions and ADC operation mode

Function		SAR mode	9	Oversamp	ling mode	Hybrid mo	de	
		Single scan mode	Continuous scan mode	Single scan mode	Continuous scan mode	Single scan mode	Continuous scan mode	Background continuous scan mode
Analog input	Single-ended input	1	1	1	1	1	1	1
	Differential input	_* ¹	_*1	1	1	1	1	1
	Programmable gain amplifier	1	1	1	1	1	1	1
	Channel-dedicated sample-and-hold circuit	1	-	-	-	1	1	1
Diagnosis function/extended	Disconnection detection assist function	1	1	1	1	1	1	-
analog function	Self-diagnosis	1	1	1	-	1	-	-
	Internal reference voltage	1	1	1	1	1	1	1
	Temperature sensor	1	1	1	1	1	1	1
	D/A converter (DA0 to DA3)	1	1	1	1	1	1	1
Scanning operation	Group priority operation	1	1	-	-	-	-	-
	Multiple A/D converter synchronous operation	1	1	1	1	1	1	1
Digital calculation	Digital filter function	_	_	✓ * ²	✓ * ²	✓ * ²	✓ * ²	✓*2
	User's gain/offset adjustment function	1	1	1	1	1	1	1
	Addition/average function	1	1	1	1	1	1	1
	Limiter clip function	1	1	1	1	1	1	1
	Compare match function	1	1	1	1	1	1	1
FIFO function		1	1	1	1	1	1	1

Note 1. As an exception, only in the self-diagnosis operation, the Differential input mode is supported.

Note 2. Use of the digital filter function is required when in Oversampling mode and Hybrid mode.



Table 36.2 Association between ADC functions and ADC operation mode

Function	SAR mode	9	Oversamp	ling mode	Hybrid mo	Hybrid mode			
		Single scan mode	Continuous scan mode	Single scan mode	Continuous scan mode	Single scan mode	Continuous scan mode	Background continuous scan mode	
Analog input	Single-ended input	1	1	1	1	1	1	1	
	Differential input	_* ¹	_*1	1	1	1	1	1	
	Programmable gain amplifier	1	~	1	1	1	1	1	
	Channel-dedicated sample-and-hold circuit	1	-	-	-	1	1	1	
Diagnosis function/extended	Disconnection detection assist function	1	✓	1	1	1	1	-	
analog function	Self-diagnosis	1	1	1	-	1	_* ³	_*3	
	Internal reference voltage	1	1	1	1	1	1	1	
	Temperature sensor	1	1	1	1	1	1	1	
	D/A converter (DA0 to DA3)	1	1	1	1	1	1	1	
Scanning operation	Group priority operation	1	1	-	-	-	-	-	
	Multiple A/D converter synchronous operation	1	1	1	1	1	1	1	
Digital calculation	Digital filter function	-	I	✓*2	✓ *2	✓ *2	✓ *2	✓*2	
	User's gain/offset adjustment function	1	~	1	1	1	1	1	
	Addition/average function	1	1	1	1	1	1	1	
	Limiter clip function	1	1	1	1	1	1	1	
	Compare match function	1	1	1	1	1	1	1	
FIFO function		1	✓	✓	1	✓	✓	1	

Note 1. As an exception, only in the self-diagnosis operation, the Differential input mode is supported.

Note 2. Use of the digital filter function is required when in Oversampling mode and Hybrid mode.

Note 3. As an exception, Continuous scan mode and Background continuous scan mode are supported only when using dummy conversion channels with the channel-dedicated sample-and-hold circuit. For details, see "36.3.16.3(1) Limitations on usage of channel-dedicated sample-and-hold circuit in Hybrid mode.







After correction





Table 36.12 Example of the scanning operation in Hybrid mode - Continuous scan mode

step	Operation
1	When a software trigger or a trigger from a peripheral module is input, the scanning operation of the scan group
	corresponding to the trigger is started.
	When scanning operation starts, ADGRSR.ACTGRn ($n = 0$ to 8) corresponding to that scan group is set to 1.
	ADSR.ADACTm(m = 0, 1) bit corresponding to the A/D converter performing the A/D conversion is also set to 1.
2	In Hybrid mode, the scanning operation is performed while switching analog channels every time oversampling
	is performed.
3	After the oversampling corresponding to the number of TAPs of the digital filter and the number of
	A/D-converted value addition/averaging times is performed to each analog channel, A/D conversion data is
	output. (The time taken for the oversampling required to obtain the first A/D conversion data is called the initial
	delay time.)
	The A/D conversion data is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If
	FIFO is used, A/D conversion data is also stored in FIFO data register (ADFIFODRk ($k = 0$ to 8)).
4	If the scan end interrupt is enabled, the scan end interrupt corresponding to that scan group is generated when
	the A/D conversion of all virtual channels assigned to that scan group is completed.
5	The second and subsequent rounds of scanning operations are performed while the oversampling data stored in
	the digital filter is retained.
	Each one time oversampling or each multiple times oversampling corresponding to the number of A/D-converted
	value addition/averaging times is performed for each analog channel, the next A/D conversion data is output.
	(The time taken for the oversampling required to obtain the second and subsequent A/D conversion data in
	continuous scan operation is called the group delay time.)
	The A/D conversion data is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If
	FIFO is used, A/D conversion data is also stored in FIFO data register (ADFIFODRk ($k = 0$ to 8)).
6	If the scan end interrupt is enabled, the scan end interrupt corresponding to that scan group is generated when
	the A/D conversion of all virtual channels assigned to that scan group is completed.
7	Thereafter, until the A/D conversion stop process is performed, Step 5 to 6 are repeated, and the scanning
	operation continues. To stop the A/D conversion, you must follow to section 36.5.4. Force Stops the A/D
	Conversion Operation.



Table 36.12 Example of the scanning operation in Hybrid mode - Continuous scan mode

step	Operation
1	When a software trigger or a trigger from a peripheral module is input, the scanning operation of the scan group
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	When scanning operation starts, ADGRSR.ACTGRn ($n = 0$ to 8) corresponding to that scan group is set to 1.
	ADSR.ADACTm(m = 0, 1) bit corresponding to the A/D converter performing the A/D conversion is also set to 1.
2	In Hybrid mode, the scanning operation is performed while switching analog channels every time oversampling
	is performed.
3	After the oversampling corresponding to the number of TAPs of the digital filter and the number of
	A/D-converted value addition/averaging times is performed to each analog channel, A/D conversion data is
	output. (The time taken for the oversampling required to obtain the first A/D conversion data is called the initial
	delay time.)
	The A/D conversion data is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If
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4	If the scan end interrupt is enabled, the scan end interrupt corresponding to that scan group is generated when
	the A/D conversion of all virtual channels assigned to that scan group is completed.
5	In scanning operation after the initial delay time has elapsed, each time oversampling is performed for each
	analog channel, the data in the digital filter is updated. The updated A/D conversion data for each analog
	channel can be output each one time oversampling or each multiple times oversampling corresponding to the
	number of A/D-converted value addition/averaging times is performed.
	The A/D conversion data is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2, 5 to 8)). If
	FIFO is used, A/D conversion data is also stored in FIFO data register (ADFIFODRk ($k = 0$ to 8)).
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	the A/D conversion of all virtual channels assigned to that scan group is completed.
7	Thereafter, until the A/D conversion stop process is performed, Step 5 to 6 are repeated, and the scanning
	operation continues. To stop the A/D conversion, you must follow to section 36.5.4. Force Stops the A/D
	Conversion Operation.



Before co	orrection	<u>1</u>												
A/D Conversion of	onfiguration													
An	alog Channel 0 (AN000)]	Virtu	al Channel 0	\square									
An	alog Channel 2 (AN002)	_]	Virtu	al Channel 1			Scan Gro	.p 0 qu		A/D Co	nverter Unit	0		
An	alog Channel 4		Virtu	al Channel 2]		
	(/ 11004)		L]									
A/D Conversion of	peration Scan s	tart processin	g											
Start Trigger	fo	r Scan Group	0											
ADACT0		 •												
ACTGR0	(1)	-												4th
		initial sca	nning opera	ation				(5) 2nd sca	nning opera	tion 🔸	(7) 3rd scan	ning operati	(7) 	scanning operation
Scan Group							Sca	an Group 0						
Analog Channel		AN000	AN002	AN004		0 VC1	AN004	AN000	AN002	AN004	AN000	AN002	AN004	AN000
		(2)			<u> </u>			(5)			(7)			
		AN000	AN002	AN004		0 AN002	AN004	AN000	AN002	AN004	AN000	AN002		AN000
A/D Converter	Idle	SPL CNV	SPL CNV	SPL CNV		NV SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV
						(3)	\		(5)	\				
ADDR0						A/D c	(3)	sult of AN00	00 A/D c	(5)	esult of AN00	0 A/D con	rersion result of A	
ADDR2							A/D o	onversion re	esult of AN00	02 A/D c	onversion re	sult of AN00	2 A/D conv of AN002	
ADDR4								A/D c	conversion re	esult of ANO	04 A/D α	onversion re	sult of AN004	1
A/D Scan end interrupt 0									terrupt gener	ated		errupt genera	1160	
(ADC_ADI0) Note, VC : V	/irtual Channel													
SPL : Sampli CNV : Conve	ing state ersion state													
Figure 36.1	2 Example	of the	scanni	ng opera	ation in	Hybrid m	node –	Contin	uous so	can mo	de			



After cor	rection								
A/D Conversion	configuration								
A	nalog Channel 0 (AN000)	►	Virtual Channel 0						
A	nalog Channel 2 (AN002)	_ •	Virtual Channel 1		Scan Group 0		A/D Conve	erter Unit 0 C0)	
Ai	nalog Channel 4 (AN004)	►	Virtual Channel 2					,	
	. ,								
A/D Conversion	operation Scan st	art processing							
Start Trigger	for	 r Scan Group (0						
ADACT0		 							
ACTGR0	(1)	·			(5)		(7)		4th (7) scanning
Seen Crown		initial scan	ning operation			nd scanning oper	ation ()	3rd scanning operation	operation
Virtual Channel		VC0	VC1 VC2	VC0 VC1	VC2	VC0 VC1	VC2	VC0 VC1 VC	2 VC0
Analog Channel		AN000	AN002 AN004	AN000 AN00	2 AN004 A	N000 AN002	AN004	AN000 AN002 AN0	04 AN000
		(2)	Initial de	lay time	(5)	Scan conversi	(7) on time	Scan conversion time	. 1
		AN000	AN002 AN004			AN002	AN004	AN000 AN002 AN0	D4 AN000
A/D Converter operation	Idle	SPL CNV S	SPL CNV SPL CNV	SPL CNV SPL C	NV SPL CNV SP	_ CNV SPL CN	IV SPL CNV S	PL CNV SPL CNV SPL	CNV SPL CNV
ADDR0				(3) A/I	D conversion result of	(5) of AN000 A/D	conversion result	t of AN000 A/D conversion re	sult of AN0 00
ADDR2					(3) A/D conve	rsion result of AN	(5) 002 A/D conv	version result of AN002	D conversion result AN002
ADDR4						, (3) A/D conversion	result of AN004	(5) A/D conversion result of A	N004
A/D Scan end						(4) Interrupt gen	erated	(6) Interrupt generated	П
interrupt 0 (ADC_ADI0)									
Note. VC: SPL:Samp	Virtual Channel ling state								
Figure 36.1	2 Example	of the s	canning operat	tion in Hybrid	mode – Co	ntinuous s	scan mode)	



Table 36.13 Example of the scanning operation in Hybrid mode – Background continuous scan mode

Step	Operation
1	When a software trigger or a trigger from a peripheral module is input, the scanning operation of the scan group
	corresponding to the trigger is started.
	When scanning operation starts, ADGRSR.ACTGRn ($n = 0$ to 8) corresponding to that scan group is set to 1.
	ADSR.ADACTm (m = 0, 1) bit corresponding to the A/D converter performing the A/D conversion is also set to
	1.
2	In Hybrid mode, the scanning operation is performed while switching analog channels every time oversampling
	is performed.
3	After the oversampling corresponding to the number of TAPs of the digital filter and the number of
	A/D-converted value addition/averaging times is performed to each analog channel, A/D conversion data
	becomes in ready to be output.
	(The time taken for the oversampling required to obtain the first A/D conversion data is called the initial delay
	time. In the background continuous scan operation, A/D conversion data can be obtained after the initial delay
	time has elapsed from the start of the scanning operation.)
4	The second and subsequent rounds of scanning operations are performed while the oversampling data stored in
	the digital filter is retained. Each time oversampling is performed for each analog channel, the data in the digital
	filter is updated. Each one time oversampling or each multiple times oversampling corresponding to the number
	of A/D-converted value addition/averaging times is performed for each analog channel, the next A/D conversion
	data becomes in ready to be output.
	(The time taken for the oversampling required to obtain the second and subsequent A/D conversion data in
	continuous scan operation is called the group delay time. In background continuous scan operation, after the
	initial delay time has elapsed from the start of the scanning operation, the updated A/D conversion data can be
	btained every time the group delay time elapses.)
5	When an A/D conversion start trigger is input during background continuous scanning operation, the most
	recent A/D conversion data at that time is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2,
	5 to 8)). If FIFO function is set to enabled, A/D conversion data is also stored in the FIFO data register
	(ADFIFODRk (k = 0 to 8)).
6	If scan end interrupt is set to enable, scan end interrupt is generated.
7	Thereafter, until the A/D conversion stop process is performed, Background continuous scanning operation (Step
	4) is repeated. And whenever the A/D conversion start trigger is input during Background continuous scanning
	operation, the A/D conversion data is output (Step 5 and Step 6). To stop A/D conversion, you must follow to
	section 36.5.4. Force Stops the A/D Conversion Operation.



Table 36.13 Example of the scanning operation in Hybrid mode - Background continuous scan mode

Step	Operation
1	When a software trigger or a trigger from a peripheral module is input, the scanning operation of the scan group
	corresponding to the trigger is started.
	When scanning operation starts, ADGRSR.ACTGRn ($n = 0$ to 8) corresponding to that scan group is set to 1.
	ADSR.ADACTm (m = 0, 1) bit corresponding to the A/D converter performing the A/D conversion is also set to
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2	In Hybrid mode, the scanning operation is performed while switching analog channels every time oversampling
	is performed.
3	After the oversampling corresponding to the number of TAPs of the digital filter and the number of
	A/D-converted value addition/averaging times is performed to each analog channel, A/D conversion data
	becomes in ready to be output.
	(The time taken for the oversampling required to obtain the first A/D conversion data is called the initial delay
	time. In the background continuous scan operation, A/D conversion data can be obtained after the initial delay
	time has elapsed from the start of the scanning operation.)
4	In scanning operation after the initial delay time has elapsed, each time oversampling is performed for each
	analog channel, the data in the digital filter is updated. The updated A/D conversion data for each analog
	channel can be output each one time oversampling or each multiple times oversampling corresponding to the
	number of A/D-converted value addition/averaging times is performed.
5	When an A/D conversion start trigger is input during background continuous scanning operation, the most
	recent A/D conversion data at that time is stored in the data register (ADDRi (i = 0 to 28), ADEXDRj (j = 0 to 2,
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	(ADFIFODRk (k = 0 to 8)).
6	If scan end interrupt is set to enable, scan end interrupt is generated.
7	Thereafter, until the A/D conversion stop process is performed, Background continuous scanning operation (Step
	4) is repeated. And whenever the A/D conversion start trigger is input during Background continuous scanning
	operation, the A/D conversion data is output (Step 5 and Step 6). To stop A/D conversion, you must follow to
	section 36.5.4. Force Stops the A/D Conversion Operation.



	figuration				_								
Analo (og Channel 0 (AN000)		→ Virtu	ual Channel 0									
Analog	g Channel 2 (AN002)		→ Virtu	ual Channel 1]		Scan Grou	ip 0		A/D Cor	verter	Unit 0	
Analo	og Channel 4		→ Virtu	ual Channel 2	1								
/D Conversion ope	eration												
	Scan si	tart processi	ng										
Start Trigger -	fo	r Scan Group	р 0						(5) Start Tr	igger			
ADACT0	\square	<u>_</u>											
ACTGR0	(1)	•						(4)				7)	4th sca
		initial sca	anning opera	ation				2nd sca	nning operat	tion 🔸	•	⁷ 3rd scanning o	operation →
Scan Group – Virtual Channel					VCO	VC1	Sca	n Group 0	VC1			0 //C1	
Analog Channel		AN000	AN002	AN004	AN000	AN002	AN004	AN000	AN002	AN004	ANO	00 AN002	AN004 A
-	((2)	. <u> </u>	Initial dela	ay time		(4)	G	iroup delay ti	me		Group delav t	ime
		AN000	AN002	AN004	AN000	AN0 02	AN004	AN000	AN0 02	AN004	ANO	00 AN002	AN004 A
A/D Converter operation	Idle	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL	CNV SPL CNV	SPL CNV SPL
				(((3)	A/D Conv	ersion data				
ADDR0								ready to b	e output		((5) A/D conversio	on result of AN000
-												(5)	on requit of ANOO
-											((5)	ITTESUL OF ANOUZ
ADDR4 –											—((A/D conversion)	on result of AN004
A/D Scan end interrupt 0 _											•		
Note. VC: Virtu	ual Channel												
SPL : Sampling	state on state												
CNV : Conversio		e of the	scanni	ng operat	ion in H	ybrid m	node –	Backgı	round c	ontinuo	us s	can mode	Э
gure 36.13	Example												
gure 36.13	Example												
igure 36.13	Example												
gure 36.13	Example												
igure 36.13	Example												
igure 36.13	Example												
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igure 36.13	Example												
igure 36.13	Example												



	n configuration				_									
	Analog Channel ((AN000)	0	► Virtu	ual Channel 0										
	Analog Channel 2 (AN002)	2	► Virtu	ual Channel 1]		Scan Gro	up 0 qu		A/D Cor	nverter Unit ADC0)	0		
	Analog Channel 4 (AN004)	4	► Virtu	ual Channel 2	7									
VD Conversio	n operation													
	Scar	n start processi →	ng											
Start Trigg	er	for Scan Grou	р 0						(5) Start Tr	igger	7			
ADAC	то													
ACTGI	R0	<u> </u>						(4)			(7)			4th scanning
0		initial sc	anning opera	ation			•	2nd scar	nning operat	ion 🔸	∢ 3n	d scanning o	peration +	operation
Virtual Chanr	up 	VC0	VC1	VC2	VC0	VC1	VC2	VC0	VC1	VC2		VC1	VC2	VC0
Analog Chanr		AN000	AN002	AN004	AN000	AN002	AN004	AN000	AN002	AN004	AN000	AN002	AN004	AN00(
		(2)		Initial de	elay time		(4) Scar	n conversior	n time	(7) Sca	n conversion	time	
		AN000	AN002	AN004	AN000	AN0 02	AN004	AN000	AN0 02	AN004	AN000	AN002	AN004	AN000
A/D Convert operati	er Idle	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CNV	SPL CN
				(((3)	A/D Conve	ersion data					
الم الم								ready to be	e output		(5) /D.conversion	n result of A	NOOO
											(5))	in result of A	14000
ADDF	~~										(A	/D conversion)	n result of A	N002
ADDF											(A	/D conversion	n result of A	N004
	nd										<u> (6</u>) Interrupt ge	enerated	
A/D Scan ei interrupt	0													
A/D Scan er interrupt (ADC_ADI	0 0)													
A/D Scan ei interrupt (ADC_ADI Note. VC SPL : San CNV : Cor	0 0) : Virtual Channel npling state nversion state													
A/D Scan ei interrup: (ADC_ADI Note. VC SPL : Sar CNV : Con igure 36.	: Virtual Channel npling state nversion state 13 Examp	ole of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode)	
A/D Scan e interrup (ADC_ADI Note. VC SPL : Sar CNV : Co igure 36.	: 0 0) :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode)	
A/D Scan ei interrup (ADC_ADi Note. VC SPL : Sar CNV : Co igure 36.	:0 :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode)	
A/D Scan e interrup (ADC_AD) Note. VC SPL : Sar CNV : Co igure 36.	: 0 :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode	•	
A/D Scan e interrup (ADC_AD) Note. VC SPL : Sar CNV : Co igure 36.	: 0 0) :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode	9	
A/D Scan ei interrup: (ADC_AD) Note. VC SPL: Sar CNV: Co igure 36.	:0 :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode)	
A/D Scan e interrup (ADC_AD) Note. VC SPL : Sar CNV : Co igure 36.	:0 :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode	3	
A/D Scan e interrup (ADC_AD) Note. VC SPL : Sar CNV : Co igure 36.	: 0 0) :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode	2	
A/D Scan e interrup: (ADC_AD) Note. VC SPL: Sar CNV: Co igure 36.	:0 :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode)	
A/D Scan e interrup (ADC_AD) Note. VC SPL : Sar CNV : Co igure 36.	: 0 :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode	2	
A/D Scan e interrup (ADC_AD) Note. VC SPL : Sar CNV : Co igure 36.	: 0 :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode)	
A/D Scan e interrup: (ADC_AD) Note. VC SPL : Sar CNV : Co igure 36.	:0 :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode)	
A/D Scan e interrup (ADC_AD) Note. VC SPL : Sar CNV : Co igure 36.	: 0 :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode	2	
A/D Scan e interrup: (ADC_AD) Note. VC SPL : Sar CNV : Co igure 36.	:0 :: Virtual Channel npling state nversion state 13 Examp	le of the	scanni	ng opera	tion in H	ybrid m	node –	Backgr	ound c	ontinuc	ous sca	n mode		



Table 36.16 List of operation mode for which the self-diagnostic function is available

Operation mode – Scan mode	Self-diagnosis Function						
SAR mode - Single scan mode	1						
SAR mode - Continuous scan mode	-						
Oversampling mode - Single scan mode	1						
Oversampling mode - Continuous scan mode	-						
Hybrid mode - Single scan mode							
Hybrid mode - Continuous scan mode	-						
Hybrid mode - Background continuous scan mode							
lote: ✓: Available, —: Not Available							

After correction

Table 36.16 List of operation mode for which the self-diagnostic function is available

Operation mode – Scan mode	Self-diagnosis Function					
SAR mode - Single scan mode	1					
SAR mode - Continuous scan mode	\checkmark					
Oversampling mode - Single scan mode	✓					
Oversampling mode - Continuous scan mode	-					
Hybrid mode - Single scan mode						
Hybrid mode - Continuous scan mode	_*1					
Hybrid mode - Background continuous scan mode	_*1					

Note: 🖌: Available, —: Not Available

Note 1. As an exception, Continuous scan mode and Background continuous scan mode are supported only when using dummy conversion channels with the channel-dedicated sample-and-hold. For details, see "36.3.16.3(1) Limitations on usage of channel-dedicated sample-and-hold circuit in Hybrid mode.





mode



Figure 36.21 Basic operation of channel-dedicated sample-and-hold circuit in Hybrid mode – Continuous scan mode









Table 36.51 Initial setup procedure

No.	Step	Description
1	Release module-stop	Release the module-stop bit for ADC in MSTPCR register.
2	I/O port configuration	Set ASEL bit of the pin used as analog input to 1.
3	Synchronous operation configuration	Set the synchronous operation function. The synchronous operation function is enabled at the initial value of the register after reset release. If the synchronous operation function is not used, be sure to disable the synchronous operation function (ADSYCR.ADSYDISm = 1 (m = 0, 1)).
4	ADCLK configuration	Set the clock source and division ratio for ADCLK. Then, set ADCLKENR.CKEN bit to 1, and wait for ADCLK to supply (ADCLKSR.CLKSR = 1).
5	A/D conversion configuration	Configure the A/D conversion settings.
6	Wait for operation stabilization	Wait until the operating stabilization times specified in the Electrical Characteristics have elapsed.
7	Self-calibration	Self-calibration must be executed prior to starting A/D conversion. Set up for self-calibration and execute it. For details, see section 36.3.8. Self-calibration.
8	Trigger configuration	To start A/D conversion by a trigger from peripheral modules, configure the triggers for each scan group.
9	Start of A/D conversion	When a software trigger or a trigger from peripheral modules is input, A/D conversion (scanning operation) starts.

After correction

Table 36.51 Initial setup procedure

No.	Step	Description
1	Release module-stop	Release the module-stop bit for ADC in MSTPCR register.
2	I/O port configuration	Set ASEL bit of the pin used as analog input to 1.
3	Synchronous operation configuration	Set the synchronous operation function. The synchronous operation function is enabled at the initial value of the register after reset release. If the synchronous operation function is not used, be sure to disable the synchronous operation function (ADSYCR.ADSYDISm = 1 (m = 0, 1)).
4	ADCLK configuration	Set the clock source and division ratio for ADCLK. *1 Then, set ADCLKENR.CKEN bit to 1, and wait for ADCLK to supply (ADCLKSR.CLKSR = 1).
5	A/D conversion configuration	Configure the A/D conversion settings.
6	Wait for operation stabilization	Wait until the operating stabilization times specified in the Electrical Characteristics have elapsed.
7	Self-calibration	Self-calibration must be executed prior to starting A/D conversion. Set up for self-calibration and execute it. For details, see section 36.3.8. Self-calibration.
8	Trigger configuration	To start A/D conversion by a trigger from peripheral modules, configure the triggers for each scan group.
9	Start of A/D conversion	When a software trigger or a trigger from peripheral modules is input, A/D conversion (scanning operation) starts.

Note 1. When GPTCLK is selected, release the GPT module stop state using the module stop register E (MSTPCRE). For details, see section 10, Low Power Modes.



Table 36.52 Procedure for changing ADCLK setting

No.	Step	Description
1	Disable trigger input	Disables the trigger input from the peripheral module. (Write ADTRGENR.STTRGENn = $0 (n = 0 \text{ to } 8)$)
2	Stop A/D conversion	Check that all A/D converter is stopped. When A/D conversion is in progress, wait until all A/D conversion is completed or forcibly stop A/D conversion operation. For details about forcibly stop A/D conversion operation, see section 36.5.4. Force Stops the A/D Conversion Operation.
3	Stop ADCLK supplies	Set ADCLKENR.CKEN bit to 0. Then, wait for ADCLK to stop (ADCLKSR.CLKSR = 0).
4	Change ADCLK setting	Change the clock-source and the division ratio for ADCLK
5	Started supplying ADCLK	Set ADCLKENR.CKEN bit to 1, and wait for ADCLK to supply (ADCLKSR.CLKSR = 1).
6	Change the A/D conversion configuration	 Change the following settings according to the changed ADCLK frequency. Successive approximation time for A/D converter Number of sampling states for A/D conversion Number of sampling states and hold mode switching states for channel-dedicated sample-and-hold circuit ^{*1} Number of states for self-calibration operation (A/D converter and channel-dedicated sample-and-hold circuit ^{*1}) Synchronous operation period ^{*2} Disconnection detection assist period ^{*3} If other settings related to A/D conversion are also to be changed, change them in this step.
7	Wait for operation stabilization	Wait until the operating stabilization times specified in the section 46, Electrical Characteristics have elapsed.
8	Self-calibration	Execute self-calibration operation prior to starting A/D conversion. For details, see section 36.3.8. Self-calibration.
9	Trigger configuration	To start A/D conversion by a trigger from peripheral modules, configure the triggers for each scan group.
10	Start of A/D conversion	When a software trigger or a trigger from peripheral modules is input, A/D

Note 3. Setting is not required when disconnection detection assist function is not used.



Table 36.52 Procedure for changing ADCLK setting

No.	Step	Description
1	Disable trigger input	Disables the trigger input from the peripheral module. (Write ADTRGENR.STTRGENn = $0 (n = 0 \text{ to } 8)$)
2	Stop A/D conversion	Check that all A/D converter is stopped. When A/D conversion is in progress, wait until all A/D conversion is completed or forcibly stop A/D conversion operation. For details about forcibly stop A/D conversion operation, see section 36.5.4. Force Stops the A/D Conversion Operation.
3	Stop ADCLK supplies	Set ADCLKENR.CKEN bit to 0. Then, wait for ADCLK to stop (ADCLKSR.CLKSR = 0).
4	Change ADCLK setting	Change the clock-source and the division ratio for ADCLK. *4
5	Started supplying ADCLK	Set ADCLKENR.CKEN bit to 1, and wait for ADCLK to supply (ADCLKSR.CLKSR = 1).
6	Change the A/D conversion configuration	Change the following settings according to the changed ADCLK frequency.
		 Successive approximation time for A/D converter
		 Number of sampling states for A/D conversion
		 Number of sampling states and hold mode switching states for channel- dedicated sample-and-hold circuit ^{*1}
		 Number of states for self-calibration operation (A/D converter and channel- dedicated sample-and-hold circuit ^{*1})
		 Synchronous operation period ^{*2}
		• Disconnection detection assist period ⁺³ If other settings related to A/D conversion are also to be changed, change them in this step.
7	Wait for operation stabilization	Wait until the operating stabilization times specified in the section 46, Electrical Characteristics have elapsed.
8	Self-calibration	Execute self-calibration operation prior to starting A/D conversion. For details, see section 36.3.8. Self-calibration.
9	Trigger configuration	To start A/D conversion by a trigger from peripheral modules, configure the triggers for each scan group.
10	Start of A/D conversion	When a software trigger or a trigger from peripheral modules is input, A/D conversion (scanning operation) starts.

Note 1. Setting is not required when channel-dedicated sample-and-hold circuit is not used.

Note 2. No change is required when synchronous operation setting is disabled (ADSYCR, ADSYDISm = 1 (m = 0, 1))

Note 3. Setting is not required when disconnection detection assist function is not used.

Note 4. When GPTCLK is selected, release the GPT module stop state using the module stop register E (MSTPCRE). For details, see section 10, Low Power Modes.



Table 36.56 A/D conversion processing time

Item	·		Symbol	Processing Time						
Channel-	Sampling time		t_{SH_SPL}	ADSHSTRm.SHSST[7:0] × ADCLK						
dedicated	Hold mode swif	tching time	$t_{\text{SH}_{\text{HLD}}}$	ADSHSTRm.SHHST[2:0] \times ADCLK						
sample-and-hold	Sampling mode switching time		t _{sH_D}	(ADSYCR.ADSYCYC[10:0] - 1) × ADCLK						
processing time	(only when Hyl	brid mode)								
Disconnection deter	ct assist processi	ing time	t _{DDA}	[When disconnection detect assist function is disabled]						
				• 0						
				[When disconnection detect assist function is enabled]						
				ADSGDCRn.ADNDIS[3:0] × ADCLK						
A/D conversion	Sampling time		t _{AD_SPL}	ADSSTRp.SSTq[9:0] × ADCLK						
time	Successive app	proximation time	t _{AD_CNV}	ADCNVSTR.CSTm[5:0] × ADCLK						
A/D conversion	SAR mode	When ADCLK = $PCLKA(1 + c_{1}) = c_{1}k^{*1}$	t _{ADDP}	[When A/D-converted value addition/averaging function is						
data processing	(Not using	PCLKA/1 is set 1								
ume	function)			 O ADCLK + 2 PCLKA [When A/D-converted value addition/averaging function is 						
	Turiction)			[when A D-converted value addition/averaging function is						
				• 7 ADCLK + 2 PCLKA						
		Other than above	-	[When A/D-converted value addition/averaging function is						
				not used]						
				● 7 ADCLK + (5~6 PCLKA)						
				[When A/D-converted value addition/averaging function is						
				used]						
				● 8 ADCLK + (5~6 PCLKA)						
	Oversampling	When ADCLK =		[When A/D-converted value addition/averaging function is						
	mode or	PCLKA/1 is set ^{*1}		not used]						
	Hybrid mode			• 8 ADCLK + 2 PCLKA						
	(Using with			[When A/D-converted value addition/averaging function is						
	digital filter									
	function)	Other than shows	-	• 9 ADCLK + 2 PCLKA						
		Other than above		[when A/D-converted value addition/averaging function is						
				\bullet 9 ADCLK + 5~6 PCLKA						
				When A/D-converted value addition/averaging function is						
				used]						
				• 10 ADCLK + 5 \sim 6 PCLKA						
Total A/D	Channel conver	rsion time ^{*2}	t _{ADCH_S}	$(t_{DDA} + t_{AD_SPL} + t_{AD_CNV}) \times N_{ADC} \times ADCLK$						
conversion time	Scan conversio	n time ^{*4}	t _{scan_s}	[When channel-dedicated sample-and-hold circuit is not						
(SAR mode) ^{*3}				used]						
				 Σt_{ADCH_S} 						
				[When channel-dedicated sample-and-hold circuit is used]						
				• $t_{SH_SPL} + t_{SH_HLD} + \Sigma t_{ADCH_S}$						
Total A/D	Oversampling p	period	t _{ov_os}	$(t_{DDA} + t_{AD_SPL} + t_{AD_CNV}) \times ADCLK$						
conversion time	version time Channel conversion time		t _{ADCH_O}	$(t_{DDA} + t_{AD_SPL} + t_{AD_CNV}) \times (N_{TAP} + N_{ADC}) \times ADCLK$						
(Oversampling		*⊏								
mode)	Scan conversio	n time ⁻⁵	t _{scan_o}	Σt _{adch_0}						
Total A/D	Channel-dedica	ated	t _{HY_SH}	t _{SH_SPL} + t _{SH_HLD} + t _{SH_D}						
conversion time	sample-and-ho	ld processing time								
(Hybrid mode) ^{*3}	in Hybrid mode	2								
	Oversampling p	period	t _{HY_OS}	$(t_{DDA} + t_{AD_SPL} + t_{AD_CNV}) \times ADCLK$						



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Scan	Initial delay	t_{HY_ID}	[When channel-dedicated sample-and-hold circuit is not
conversion			used]
time			• ($N_{TAP} + N_{ADC}$) × Σt_{HY_OS} *6
			[When channel-dedicated sample-and-hold circuit is used]
			• ($t_{HY_{SH}} \times (N_{ADC} + N_{TAP}) - t_{SH_D}$) + ($N_{TAP} + N_{ADC}$) ×
			Σt_{HY_OS} *6
	Group delay	t _{HY_GD}	[When channel-dedicated sample-and-hold circuit is not
			used]
			●Σt _{HY_OS} ^{*6}
			[When channel-dedicated sample-and-hold circuit is used]
			 t_{HY_SH} + Σt_{HY_OS} *6

Note: $n = 0 \sim 8$, m = 0, 1, $p = 0 \sim 7$, $q = 0 \sim 15$

 N_{ADC} : This value is the number of the times of the addition/averaging according to the setting value of ADDOPCRBx.ADC[3:0] (x = 0 to 36). If A/D-converted value addition/averaging function is not used, this value is 1.

 N_{TAP} : This value is the number of TAP of the digital filter that selected in ADDOPCRAx.DFSEL[2:0] (x = 0 to 36) and ADDFSRm.DFSELy[1:0] (m = 0, 1, y = 0 to 4).

 $N_{\mbox{\scriptsize SGCH}}$: This value is the number of the channels in the scan group.

Note 1. When ADCLKCR.CLKSEL[1:0] = 10b and ADCLKCR.DIVR[2:0] = 000b are set.

Note 2. It does not include the channel-dedicated sample-and-hold processing time.

Note 3. It does not include the A/D conversion data processing time.

Note 4. This is the sum of the channel conversion times (t_{ADCH_O}) that calculated from the conversion settings for each analog channel assigned to the scan group. If channel-dedicated sample-and-hold circuits are used, channel-dedicated sample-and-hold processing times (t_{SH_SPL} and t_{SH_HLD}) are also added. Note 5. This is the sum of the channel conversion times (t_{ADCH_O}) that calculated from the conversion settings for each analog channel assigned to the scan group. Note 6. This is the sum of the oversampling period (t_{HY_OS}) that calculated from the conversion settings for each analog channel assigned to the scan group.

After correction

Table 36.56 A/D conversion processing time

Item			Symbol	Processing Time							
Channeldedicated	Sampling time		t_{SH_SPL}	ADSHSTRm.SHSST[7:0] \times ADCLK							
sample-and-hold	Hold mode swi	tching time	$t_{\text{SH}_{\text{HLD}}}$	ADSHSTRm.SHHST[2:0] × ADCLK							
processing time	Sampling mode	e switching time	t_{SH_D}	$(ADSYCR.ADSYCYC[10:0] - 1) \times ADCLK$							
	(only when Hyl	brid mode)									
Disconnection dete	ect assist processi	ing time	t _{DDA}	[When disconnection detect assist function is disabled]							
				[When disconnection detect assist function is enabled]							
				 ADSGDCRn.ADNDIS[3:0] × ADCLK 							
A/D conversion	Sampling time		t _{AD_SPL}	ADSSTRp.SSTq[9:0] × ADCLK							
time	Successive app	proximation time	t _{AD_CNV}	ADCNVSTR.CSTm[5:0] × ADCLK							
A/D conversion	SAR mode	When ADCLK =	t _{ADDP}	[When A/D-converted value addition/averaging function is							
data processing	(Not using	PCLKA/1 is set ^{*1}		not used]							
time	digital filter			• 6 ADCLK + 2 PCLKA							
	function)			[When A/D-converted value addition/averaging function is							
				used]							
				• 7 ADCLK + 2 PCLKA							
		Other than above		[When A/D-converted value addition/averaging function is							
				not used]							
				● 7 ADCLK + (5~6 PCLKA)							
				[When A/D-converted value addition/averaging function is							
				used]							
				● 8 ADCLK + (5~6 PCLKA)							
	Oversampling	When ADCLK =		[When A/D-converted value addition/averaging function is							
	mode or	PCLKA/1 is set ^{*1}		not used]							
	Hybrid mode			• 8 ADCLK + 2 PCLKA							
	(Using with			[When A/D-converted value addition/averaging function is							
	digital filter			used							



	function)			• 9 ADCLK + 2 PCLKA
		Other than above		[When A/D-converted value addition/averaging function is
				• 9 ADCLK + 5 \sim 6 PCLKA
				[When A/D-converted value addition/averaging function is
				used]
				• 10 ADCLK + 5~6 PCLKA
Total A/D	Channel conve	rsion time ^{*2}	t _{ADCH_S}	$(t_{DDA} + t_{AD_SPL} + t_{AD_CNV}) \times N_{ADC} \times ADCLK$
conversion time (SAR mode) ^{*3}	Scan conversio	on time ^{*4}	t _{scan_s}	[When channel-dedicated sample-and-hold circuit is not used]
				• Stadch_s
				[When channel-dedicated sample-and-hold circuit is used]
				• $t_{SH_SPL} + t_{SH_HLD} + \Sigma t_{ADCH_S}$
Total A/D	Oversampling	period	t _{ov_os}	$(t_{DDA} + t_{AD_SPL} + t_{AD_CNV}) \times ADCLK$
conversion time	Channel conve	rsion time	t _{ADCH_O}	$(t_{DDA} + t_{AD_SPL} + t_{AD_CNV}) \times (N_{TAP} + N_{ADC}) \times ADCLK$
mode) ^{*3}	Scan conversion	on time ^{*5}	t _{scan_o}	Σt_{ADCH_0}
Total A/D	Channel-dedic	ated	t _{HY_SH}	$t_{SH_SPL} + t_{SH_HLD} + t_{SH_D}$
conversion time	sample-and-ho	old processing time		
(Hybrid mode) ^{*3}	in Hybrid mod	e		
	Oversampling	period	t _{HY_OS}	$(t_{DDA} + t_{AD_SPL} + t_{AD_CNV}) \times ADCLK$
	Scan	Initial delay	t_{HY_ID}	[When channel-dedicated sample-and-hold circuit is not
	conversion			used]
	time			• ($N_{TAP} + N_{ADC}$) × Σt_{HY_OS} *6
				[When channel-dedicated sample-and-hold circuit is used]
				$ \bullet (t_{HY_SH} \times (N_{ADC} + N_{TAP}) - t_{SH_D}) + (N_{TAP} + N_{ADC}) \times $
			<u> </u>	Σt _{HY_OS} σ
		After initial delay	t _{scan_hy}	[When channel-dedicated sample-and-hold circuit is not
		ume		useu]
				When channel-dedicated cample-and-hold circuit is used
				• $t_{\mu\nu, s\mu} + \Sigma t_{\mu\nu, os}^{*6}$
1	1		1	

Note: $n = 0 \sim 8$, m = 0, 1, $p = 0 \sim 7$, $q = 0 \sim 15$

N_{ADC} : This value is the number of the times of the addition/averaging according to the setting value of ADDOPCRBx.ADC[3:0] (x = 0 to 36). If

A/D-converted value addition/averaging function is not used, this value is 1.

NTAP : This value is the number of TAP of the digital filter that selected in ADDOPCRAx.DFSEL[2:0] (x = 0 to 36) and ADDFSRm.DFSELy[1:0] (m = 0, 1,

y = 0 to 4).

 $N_{\mbox{\scriptsize SGCH}}$: This value is the number of the channels in the scan group.

Note 1. When ADCLKCR.CLKSEL[1:0] = 10b and ADCLKCR.DIVR[2:0] = 000b are set.

Note 2. It does not include the channel-dedicated sample-and-hold processing time.

Note 3. It does not include the A/D conversion data processing time.

Note 4. This is the sum of the channel conversion times (t_{ADCH_O}) that calculated from the conversion settings for each analog channel assigned to the scan group. If channel-dedicated sample-and-hold circuits are used, channel-dedicated sample-and-hold processing times (t_{SH_SPL} and t_{SH_HLD}) are also added. Note 5. This is the sum of the channel conversion times (t_{ADCH_O}) that calculated from the conversion settings for each analog channel assigned to the scan group. Note 6. This is the sum of the oversampling period (t_{HY_OS}) that calculated from the conversion settings for each analog channel assigned to the scan group.



A/D Conversion Start Trigger		ter	d'r						
Analog Channel i Idle (ANi) Analog	Image: service								
Channel j (ANkj) Analog Channel k (ANk)	Idle //Discharge Sampline Cor	tops tap_set tap_set <thtap_set< th=""> <thtap_set< th=""> <thtap_< td=""><td>Idle Idle</td><td>/Discharge Sampling Conversion</td><td>Precharge /Discharge Sampling Conversion</td><td>le </td><td>/Discharge Sampling Conversio</td><td>n Idle Precharge Sampling Conversion</td><td>ldie</td></thtap_<></thtap_set<></thtap_set<>	Idle Idle	/Discharge Sampling Conversion	Precharge /Discharge Sampling Conversion	le 	/Discharge Sampling Conversio	n Idle Precharge Sampling Conversion	ldie
ADDRiADDRi				ANi data	t _{ADDP} → ANj data	tanne	ANi data	ANj data	tanne
ADDRk	g channel number.					ANk data			ANk data

Figure 36.55 A/D conversion processing time (Hybrid mode)

After correction



Figure 36.55 A/D conversion processing time (Hybrid mode)



	A/D Conversion Start Trigger		•																					
(4	A/D conversion status DSR.ADACTm)						t _{HY_ID}											C	t _{HY_GD}					
				t _{ну_вн}											-									
			Sampling mode		Hold mode																			
			tshjspil tshje	1.0			t _{SH_P}	1																
Ch	annel-dedicated ample-and-hold	Idle	Sampling Hol	9	Hold + Output		Idle	Sampli	ing Hold			Hold +	+ Output			Idle Sa	Impling Hold			Hold + Output			Idle	Sampling
	circuit operation			t _{HY_OS}	tHY_OS	t _{HY_OS}																		
~	Analog																	, ,						
ÐQ	Channel i (ANi)		Idle	Sampling Conversion		Idle		ld	ie	Sampling	Conversion				Idle			Sampling	Conversion		lo	le		
onvei	Analog				AD_SPL AD_CNV																			
tero	Channel j (ANi)		Idle		Sampling Conversion	Idle			Idk	le		Sampling	Conversion				Idle			Sampling Conversio		Idi	9	
perat	Analog					$\xrightarrow{t_{AD_SPL}}$ $\xrightarrow{t_{AD_CNV}}$		1																
9	Channel k (ANk)			Idle		Sampling Conversion	Idle			Idle	9			Sampling	Conversion			Idle			Sampling	Conversion		Idle
	(,											t _{ADDP}							.	tadde				
	ADDRi												ANi data							ANi data				
Da														t _{ADDP}							t _{ADDP}			
la Re	ADDRj														ANj data							ANj data		
gister																tADDP.							t _{ADDP}	
60	ADDRk															A	Nk data							ANk data
	Note: i. i. k : An	v analon chan	nel number					1																U

Figure 36.56 A/D conversion processing time (Hybrid mode with channel-dedicated sample-and-hold circuit)

After correction



Figure 36.56 A/D conversion processing time (Hybrid mode with channel-dedicated sample-and-hold circuit)



36.10.1 Prohibitation of Changing the Operation Settings During A/D Conversion Operation The registers related to the operation setting of the A/D converter should be set while all A/D converters are stopped (ADSR.ADACTm = 0 and ADSR.CALACTm = 0 (m = 0, 1)). Changing (writing) of registers except for those listed below is prohibited during A/D conversion. If the operation setting is changed during A/D conversion, operation is not guaranteed.

[Registers that can be written while the A/D converter is operating]

- Status clear registers
 - Status clear registers related to A/D converter operation
 - (ADERSCR, ADCALSCR, ADCALENDSCR, ADSCANENDSCR)

After correction

36.10.1 Prohibition of Changing the Operation Settings During A/D Conversion Operation The registers related to the operation setting of the A/D converter should be set while all A/D converters are stopped (ADSR.ADACTm = 0 and ADSR.CALACTm = 0 (m = 0, 1)). Changing (writing) of registers except for those listed below is prohibited during A/D conversion. If the operation setting is changed during A/D conversion, operation is not guaranteed.

[Registers that can be written while the A/D converter is operating]

- Status clear registers
 - Status clear registers related to A/D converter operation (ADERSCR, ADCALENDSCR, ADSCANENDSCR)

Before correction

Table 37.1 DAC12 specifications

Parameter	Specifications
Resolution	12 bits
Output channels	4 channels
Module-stop function	Module-stop state can be set to reduce power consumption
Event link function (input)	The DA0, DA1, DA2 and DA3 conversion can be started on input of
	an event signal
D/A output amplifier control function	Controls whether the output amplifier (for both amplifier-through
	and amplifier-bias controls) is used
Destination of D/A output control function	Controls whether the output to the external pin or to the internal
	modules (ACMPHS) is used
TrustZone Filter	Security attribution can be set

After correction

Table 37.1 DAC12 specification	າຣ
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Parameter	Specifications
Resolution	12 bits
Output channels	4 channels
Module-stop function	Module-stop state can be set to reduce power consumption
Event link function (input)	The DA0, DA1, DA2 and DA3 conversion can be started on input of
	an event signal
D/A output amplifier control function	Controls whether the output amplifier (for both amplifier-through
	and amplifier-bias controls) is used
Destination of D/A output control function	Controls whether the output to the external pin or to the internal
	modules (ACMPHS and ADC) is used
TrustZone Filter	Security attribution can be set





Figure 37.1 DAC12 block diagram





Figure 37.1 DAC12 block diagram



Table 37.5 D/A conversion and analog output control

DACR		DAAMPCR	DAASWCR	Channel i	Amplifier	Analog external	Analog internal
DAE	DAOEi	DAAMPi	DAASWi	operation	operation of channel i	output of channel i ^{*1}	output of channel i ^{*2}
0	0	х	х	Stop	Stop	Hi-Z	Hi-Z
0	1	0	0	Run	Stop	Amplifier-through	Hi-Z
0	1	0	1	Run	Stop	Hi-Z	Amplifier-through
0	1	1	0	Run	Run	Amplifier output	Hi-Z
0	1	1	1	Run	Run	Hi-Z	Hi-Z
1	х	0	0	Run	Stop	Amplifier-through	Hi-Z
1	х	0	1	Run	Stop	Hi-Z	Amplifier-through
1	Х	1	0	Run	Run	Amplifier output	Hi-Z
1	х	1	1	Run	Run	Hi-Z	Hi-Z

Note. x : Don't care

Note 1. output to pin Note 2. output to ACMPHS

After correction

Table 37.5 D/A conversion and analog output control

DACR		DAAMPCR	DAASWCR	Channel i	Amplifier	Analog external	Analog internal
DAE	DAOEi	DAAMPi	DAASWi	operation	operation of channel i	output of channel i ^{*1}	output of channel i ^{*2}
0	0	х	х	Stop	Stop	Hi-Z	Hi-Z
0	1	0	0	Run	Stop	Amplifier-through	Hi-Z
0	1	0	1	Run	Stop	Hi-Z	Amplifier-through
0	1	1	0	Run	Run	Amplifier output	Hi-Z
0	1	1	1	Run	Run	Hi-Z	Hi-Z
1	х	0	0	Run	Stop	Amplifier-through	Hi-Z
1	х	0	1	Run	Stop	Hi-Z	Amplifier-through
1	х	1	0	Run	Run	Amplifier output	Hi-Z
1	х	1	1	Run	Run	Hi-Z	Hi-Z

Note. x : Don't care

Note 1. output to pin Note 2. output to ACMPHS and ADC



Table 46.36 A/D conversion characteristics (Oversampling mode and Hybrid mode)

Parameter					Тур	Max	Unit	Test condition
Oversamplin	Analog input	log input Single-ended input voltage			-	VREFH0	V	-
g mode and Hybrid mode	voltage range	Differential in	put voltage ^{*1}	-VREFH0	-	+VREFH0	V	-
	Resolution			-	-	16	bit	-
	Oversampling period	Oversampling mode		0.16	-	-	μs	 ADCLK: 50 MHz Sampling time: 3 ADCLK Successive approximation time: 5 ADCLK Without disconnection detection assist function
		Hybrid mode	Hybrid mode		-	-	μs	 ADCLK: 50 MHz Sampling time: 4 ADCLK Successive approximation time: 5 ADCLK Without disconnection detection assist function
	Digital filter	Sinc filter	Initial delay	-	22	-	Fos	-
	characteristics *2		Group delay	-	11	-		-
			Normalized Cutoff Frequency	-	0.033	-	Fin/F os	-
		Minimum phase filter	Initial delay	-	22	-	Fos	-
			Group delay	-	2	-		-
			Normalized Cutoff Frequency	-	0.116	-	Fin/F os	-
			Passband ripple	-	<±0.01	-	dB	-

Note: Fos is oversampling frequency.

Note 1. Differential input voltage is (AINP - AINN) ● AINP is input voltage of ANx, and VREFL0 ≤ AINP ≤ VREFH0.

• AINN is input voltage of ANy, and VREFL0 \leq AINN \leq VREFH0. (x = 2i, y = 2i +1, i = 0, 1, 2... (any integer)) Note 2. See Figure 46.50 and Figure 46.51.

Table 46.36 A/D conversion characteristics (Oversampling mode and Hybrid mode)

Parameter	Min	Тур	Max	Unit	Test condition			
Oversamplin	Analog input	Single-ended	input voltage	VREFL0	-	VREFH0	V	-
g mode and	voltage range	Differential in	put voltage ^{*1}	-VREFH0	-	+VREFH0	V	-
Hybrid mode	Resolution			-	-	16	bit	-
	Oversampling period	Oversampling mode		0.16	-	-	μs	 ADCLK: 50 MHz Sampling time: 3 ADCLK Successive approximation time: 5 ADCLK
								 Without disconnection detection assist function Signal source impedance: 50 Ω or less
		Hybrid mode	*3	0.18	-	-	μs	 ADCLK: 50 MHz Sampling time: 4 ADCLK Successive approximation time: 5 ADCLK Without disconnection detection assist function Signal source impedance: 50 Ω or less
	Digital filter	Sinc filter	Initial delay	-	22	-	/Fos	-
	characteristics		Group delay	-	11	-		-
	*2		Normalized Cutoff Frequency	-	0.033	-	Fin/F os	-
		Minimum	Initial delay	-	22	-	7 Fos	-
		phase filter	Group delay	-	2	-		-
			Normalized Cutoff Frequency	-	0.116	-	Fin/F os	-
				Passband ripple	-	<±0.01	-	dB

Note: Fos is oversampling frequency.

When in Hybrid mode, Fos is 1/ (the sum of the oversampling periods of each analog channel assigned to the scan group). Note 1. Differential input voltage is (AINP - AINN)

• AINP is input voltage of ANx, and VREFL0 \leq AINP \leq VREFH0. • AINN is input voltage of ANy, and VREFL0 \leq AINP \leq VREFH0. (x = 2i, y = 2i +1, i = 0, 1, 2... (any integer)) Note 2. See Figure 46.50 and Figure 46.51.

Note 3. Value per channel.

