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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-RX*-A088A/E	Rev.	1.00
Title	Disclosed Registers for the Flash Memory in the RX111 Group		Information Category	Technical Notification		
Applicable Product	RX111 Group	Lot No. All	Reference Document	RX111 Group User's Manual: Hardware Rev.1.00 (R01UH0365EJ0100)		

This document describes disclosed registers for the flash memory in RX111 Group User's Manual: Hardware.

Table 1.1 Added Registers for the Flash Memory

No.	Register Name	Symbol	Address	Number of Bits
1	Flash Start-Up Setting Monitor Register	FSCMR	007F C0B0h	16
2	Flash Access Window Start Address Monitor Register	FAWSMR	007F C0B2h	16
3	Flash Access Window End Address Monitor Register	FAWEMR	007F C0B4h	16
4	Flash Initial Setting Register	FISR	007F C0B6h	8
5	Flash Extra Area Control Register	FEXCR	007F C0B7h	8
6	Flash Error Address Monitor Register L	FEAML	007F C0B8h	8
7	Flash Error Address Monitor Register H	FEAMH	007F C0BAh	8
8	Protection Unlock Register	FPR	007F C0C0h	8
9	Protection Unlock Status Register	FPSR	007F C0C1h	8
10	Flash Read Buffer Register L	FRBL	007F C0C2h	16
11	Flash Read Buffer Register H	FRBH	007F C0C4h	16
12	Flash P/E Mode Control Register	FPMCR	007F FF80h	8
13	Flash Area Select Register	FASR	007F FF81h	8
14	Flash Processing Start Address Register L	FSARL	007F FF82h	8
15	Flash Processing Start Address Register H	FSARH	007F FF84h	8
16	Flash Control Register	FCR	007F FF85h	8
17	Flash Processing End Address Register L	FEARL	007F FF86h	16
18	Flash Processing End Address Register H	FEARH	007F FF88h	8
19	Flash Reset Register	FRESETR	007F FF89h	8
20	Flash Status Register 0	FSTATR0	007F FF8Ah	8
21	Flash Status Register 1	FSTATR1	007F FF8Bh	8
22	Flash Write Buffer Register L	FWBL	007F FF8Ch	16
23	Flash Write Buffer Register H	FWBH	007F FF8Eh	16
24	Flash P/E Mode Entry Register	FENTRYR	007F FFB2h	16

Bit assignments and descriptions for the registers listed in Table 1.1 are added as follows:

1. Flash Start-Up Setting Monitor Register (FSCMR)

Address(es): 007F C0B0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SASMF	—	—	—	—	—	—	—	—
Value after reset:	0	1	1	1	1	1	1	The value set by the user	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0.	R
b8	SASMF	Start-Up Area Setting Monitor Flag	0: Setting to start up using the alternative area 1: Setting to start up using the default area	R
b14 to b9	—	Reserved	These bits are read as 1. Writing to these bits has no effect.	R
b15	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

2. Flash Access Window Start Address Monitor Register (FAWSMR)

Address(es): 007F C0B2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—										
Value after reset:	0	0	0	0	0	0	The value set by the user									

3. Flash Access Window End Address Monitor Register (FAWEMR)

Address(es): 007F C0B4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—										
Value after reset:	0	0	0	0	0	0	The value set by the user									

4. Flash Initial Setting Register (FISR)

Address(es): 007F C0B6h

	b7	b6	b5	b4	b3	b2	b1	b0
	SAS[1:0]		—	PCKA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PCKA[4:0]	Peripheral Clock Notification	These bits are used to set the frequency of the FlashIF clock (FCLK).	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	SAS[1:0]	Start-Up Area Select	b7 b6 0 X: The start-up area is selected according to the start-up area settings of the extra area. 1 0: The start-up area is switched to the default area temporarily. 1 1: The start-up area is switched to the alternate area temporarily.	R/W

5. Flash Extra Area Control Register (FEXCR)

Address(es): 007F C0B7h

	b7	b6	b5	b4	b3	b2	b1	b0
	OPST	—	—	—	—	CMD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	CMD[2:0]	Software Command Setting	b2 b0 0 0 1: Start-up area information program 0 1 0: Access window information program Settings other than above are prohibited.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	OPST	Processing Start	0: Processing stops. 1: Processing starts.	R/W

6. Flash Error Address Monitor Register L (FEAML)

Address(es): 007F C0B8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7. Flash Error Address Monitor Register H (FEAMH)

Address(es): 007F C0BAh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—				
Value after reset:	0	0	0	0	0	0	0	0

8. Protection Unlock Register (FPR)

Address(es): 007F C0C0h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

9. Protection Unlock Status Register (FPSR)

Address(es): 007F C0C1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PERR	Protect Error Flag	0: No error 1: An error occurs.	R
b7 to b1	—	Reserved	These bits are read as 0.	R

10. Flash Read Buffer Register L (FRBL)

Address(es): 007F C0C2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11. Flash Read Buffer Register H (FRBH)

Address(es): 007F C0C4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

12. Flash P/E Mode Control Register (FPMCR)

Address(es): 007F FF80h

	b7	b6	b5	b4	b3	b2	b1	b0
	FMS2	LVPE	—	FMS1	RPDIS	—	FMS0	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	FMS0	Flash Operating Mode Select 0	FMS2 FMS1 FMS0 0 0 0: ROM read mode 0 1 1: Discharge mode 1 1 1 1: Discharge mode 2 1 0 1: ROM P/E mode 0 1 0: E2 DataFlash P/E mode Settings other than above are prohibited.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	RPDIS	ROM P/E Disable	0: ROM programming/erasure enabled 1: ROM programming/erasure disabled	R/W
b4	FMS1	Flash Operating Mode Select 1	See the FMS0 bit.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	LVPE	Low-Voltage P/E Mode Enable	0: Low-voltage P/E mode disabled 1: Low-voltage P/E mode enabled	R/W
b7	FMS2	Flash Operating Mode Select 2	See the FMS0 bit.	R/W

13. Flash Area Select Register (FASR)

Address(es): 007F FF81h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EXS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EXS	Extra Area Select	0: User area or data area 1: Extra area	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

14. Flash Processing Start Address Register L (FSARL)

Address(es): 007F FF82h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15. Flash Processing Start Address Register H (FSARH)

Address(es): 007F FF84h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—				
Value after reset:	0	0	0	0	0	0	0	0

16. Flash Control Register (FCR)

Address(es): 007F FF85h

	b7	b6	b5	b4	b3	b2	b1	b0
	OPST	STOP	—	DRC	CMD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CMD[3:0]	Software Command Setting	b3 b0 0 0 0 1: Program 0 0 1 1: Block erase 0 1 0 1: Consecutive read 1 0 1 1: Blank check Settings other than above are prohibited.	R/W
b4	DRC	Data Read Completion	0: Data is not read or next data is requested. 1: Data reading is completed.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	STOP	Forced Processing Stop	When this bit is set to 1, the processing being executed can be forcibly stopped.	R/W
b7	OPST	Processing Start	0: Processing stops. 1: Processing starts.	R/W

17. Flash Processing End Address Register L (FEARL)

Address(es): 007F FF86h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

18. Flash Processing End Address Register H (FEARH)

Address(es): 007F FF88h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—				
Value after reset:	0	0	0	0	0	0	0	0

19. Flash Reset Register (FRESETR)

Address(es): 007F FF89h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	FRESET
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FRESET	Flash Reset	0: Flash control circuit reset is released. 1: Flash control circuit is reset.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

20. Flash Status Register 0 (FSTATR0)

Address(es): 007F FF8Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	EILGLERR	ILGLERR	BCERR	—	PRGERR	ERERR
Value after reset:	x	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ERERR	Erase Error Flag	0: Erasure terminates normally. 1: An error occurs during erasure.	R
b1	PRGERR	Program Error Flag	0: Programming terminates normally. 1: An error occurs during programming.	R
b2	—	Reserved	This bit is read as 0.	R
b3	BCERR	Blank Check Error Flag	0: Blank checking terminates normally. 1: An error occurs during blank checking.	R
b4	ILGLERR	Illegal Command Error Flag	0: No illegal software command or illegal access is detected. 1: An illegal command or illegal access is detected.	R
b5	EILGLERR	Extra Area Illegal Command Error Flag	0: No illegal command or illegal access to the extra area is detected. 1: An illegal command or illegal access to the extra area is detected.	R
b7, b6	—	Reserved	These bits are read as 0.	R

21. Flash Status Register 1 (FSTATR1)

Address(es): 007F FF8Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	EXRDY	FRDY	—	—	—	—	DRRDY	—
Value after reset:	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0.	R
b1	DRRDY	Data Read Ready Flag	0: No valid data in FRBH and FRBL registers 1: Valid data in FRBH and FRBL registers	R
b2	—	Reserved	This bit is read as 1.	R
b5 to b3	—	Reserved	These bits are read as 0.	R
b6	FRDY	Flash Ready Flag	0: Other than below 1: 00h can be written to the FCR register (processing to complete the software command).	R
b7	EXRDY	Extra Area Ready Flag	0: Other than below 1: 00h can be written to the FEXCR register (processing to complete the software command).	R

22. Flash Write Buffer Register L (FWBL)

Address(es): 007F FF8Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

23. Flash Write Buffer Register H (FWBH)

Address(es): 007F FF8Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

24. Flash P/E Mode Entry Register (FENTRYR)

Address(es): 007F FFB2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FEKEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRY0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FENTRY0	ROM P/E Mode Entry 0	0: ROM is in read mode. 1: ROM can be placed in P/E mode.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	FENTRYD	E2 DataFlash P/E Mode Entry	0: E2 DataFlash is in read mode. 1: E2 DataFlash can be placed in P/E mode.	R/W
b15 to b8	FEKEY[7:0]	Key Code	The FEKEY[7:0] bits are used to control rewiring of the FENTRYR register. When rewriting the value of the lower-order 8 bits, set the FEKEY[7:0] bits to AAh at the same time (write this register in 16 bits). The FEKEY[7:0] bits are read as 00h.	R/W