

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation.

Product Category	MPU & MCU	Document No.	TN-16C-A210A/E	Rev.	1.00
Title	Descriptions changed in M16C/5LD Group, M16C/56D Group User's Manual		Information Category	Technical Notification	
Applicable Product	M16C/5LD and M16C/56D Groups	Lot No.	Reference Document	M16C/5LD Group, M16C/56D Group User's Manual: Hardware Rev.1.20	
		—			

Some specifications of the M16C/5LD and M16C/56D Groups have been changed. MCU usage and setting procedures have also been added or changed.

➔: Indicates the titles in the M16C/5LD Group, M16C/56D Group User's Manual: Hardware Rev.1.20.

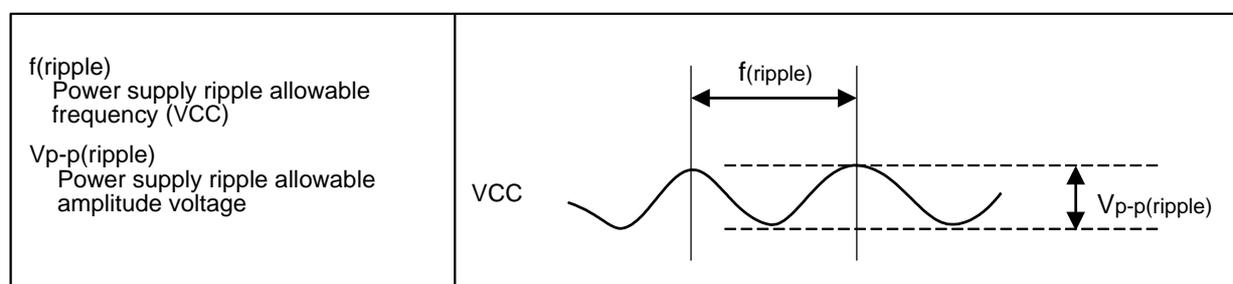
1. Specification Changes

1.1 Clock

➔ 8.9.5 PLL Frequency Synthesizer

To use the PLL frequency synthesizer, stabilize the supply voltage within the acceptable range of power supply ripple. The following table shows the acceptable range of power supply ripple and the figure shows the voltage fluctuation timing.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
$f(\text{ripple})$	Power supply ripple allowable frequency (VCC)			10	kHz
$V_{p-p}(\text{ripple})$	Power supply ripple allowable amplitude voltage	(VCC = 5 V)		0.5	V
		(VCC = 3 V)		0.3	V
$V_{CC}(\Delta V / \Delta T)$	Power supply ripple rising/falling gradient	(VCC = 5 V)		0.3	V/ms
		(VCC = 3 V)		0.3	V/ms



1.2 G1BT Register in Timer S

➔ 18.2.5 Base Timer Register (G1BT)

Do not write to this register.

The G1BT register becomes 0000h when the BTS bit in the G1BCR1 register is set to 0 (base timer reset). This function works same as before without any change.

2. Changes on Usage Note

2.1 Interrupt Request When Selecting Time Measurement Function

➔ 18.5.6 Interrupt Request When Selecting Time Measurement Function

When the FSC_j bit ($j = 0$ to 7) in the G1FS register is set to 1 (time measurement function selected), and the IFE_j bit in the G1FE register is also set to 1, the G1IR_j bit in the G1IR register, or the IR bit in the ICOCiIC register ($i = 0, 1$) or ICOCHjIC register ($j = 0$ to 3) may become 1 (interrupt requested) after a maximum of two fBT1 cycles.

When using the IC/OC interrupt i or IC/OC channel j interrupt, set bits FSC_j and IFE_j to 1, then perform the following.

- (1) Wait for two or more fBT1 cycles.
- (2) Set the IR bit in the ICOCiIC register and/or ICOCHjIC register to 0.
- (3) Wait for three or more fBT1 cycles after the time measurement function is selected. Set the G1IR register to 00h after the IR bit in the ICOCiIC register is set to 0.

3. Additions and Changes on Usage and Setting Procedures

3.1 Flash Memory

3.1.1 User Boot Mode Program

➔ 26.11.4.1 User Boot Mode Program in Notes on Flash Memory

Following notes have been added to the user boot mode description:

- When using user boot mode, make sure to allocate the program to be executed to program ROM 2.
- The LVDAS bit in the OFS1 address and bits WDTRCS1 and WDTRCS0 in the OFS2 address are disabled in boot mode.
- When restarting the MCU in user boot mode after starting it in user boot mode, RAM becomes undefined.
- If addresses 13FF8h to 13FFBh are all 00h, the MCU does not enter standard serial I/O mode. Therefore, the programmer or on-chip debugger cannot be connected.
- As the reset sequence differs, the time necessary for starting the program is longer than in single-chip mode.
- Functions in user boot mode cannot be debugged by the on-chip debugging emulator or full spec emulator.
- While using user boot mode, do not change the input level of the pin used for user boot entry. However, if there is a possibility that the input level may change, perform the necessary processes in user boot mode, then restart the MCU in single-chip mode before the input level changes.
- To use user boot mode after standard serial I/O mode, turn off the power when exiting standard serial I/O mode, and then turn on the power again (cold start). The MCU enters user boot mode under the right conditions.

3.1.2 Procedures When Suspend Function is Enabled

➔ 26.8.1.1 Suspend Function (EW0 Mode), 26.8.2.1 Suspend Function (EW1 Mode)

The procedure for enabling the suspend function has been modified. The modified figures and modifications are shown below. Post modification and premodification examples of the program flowcharts in EW0 mode are shown on the next page.

Modified Figures

- Program Flowchart in EW0 Mode (Suspend Function Enabled)
- Block Erase Flowchart in EW0 Mode (Suspend Function Enabled)
- Lock Bit Program Flowchart in EW0 Mode (Suspend Function Enabled)

Modifications

- The timing to set the I flag to 1 (interrupt enabled) has been changed.
- The determination flag used in maskable interrupt routine has been changed from bits FMR32 or FMR33 to the FMR00 bit.

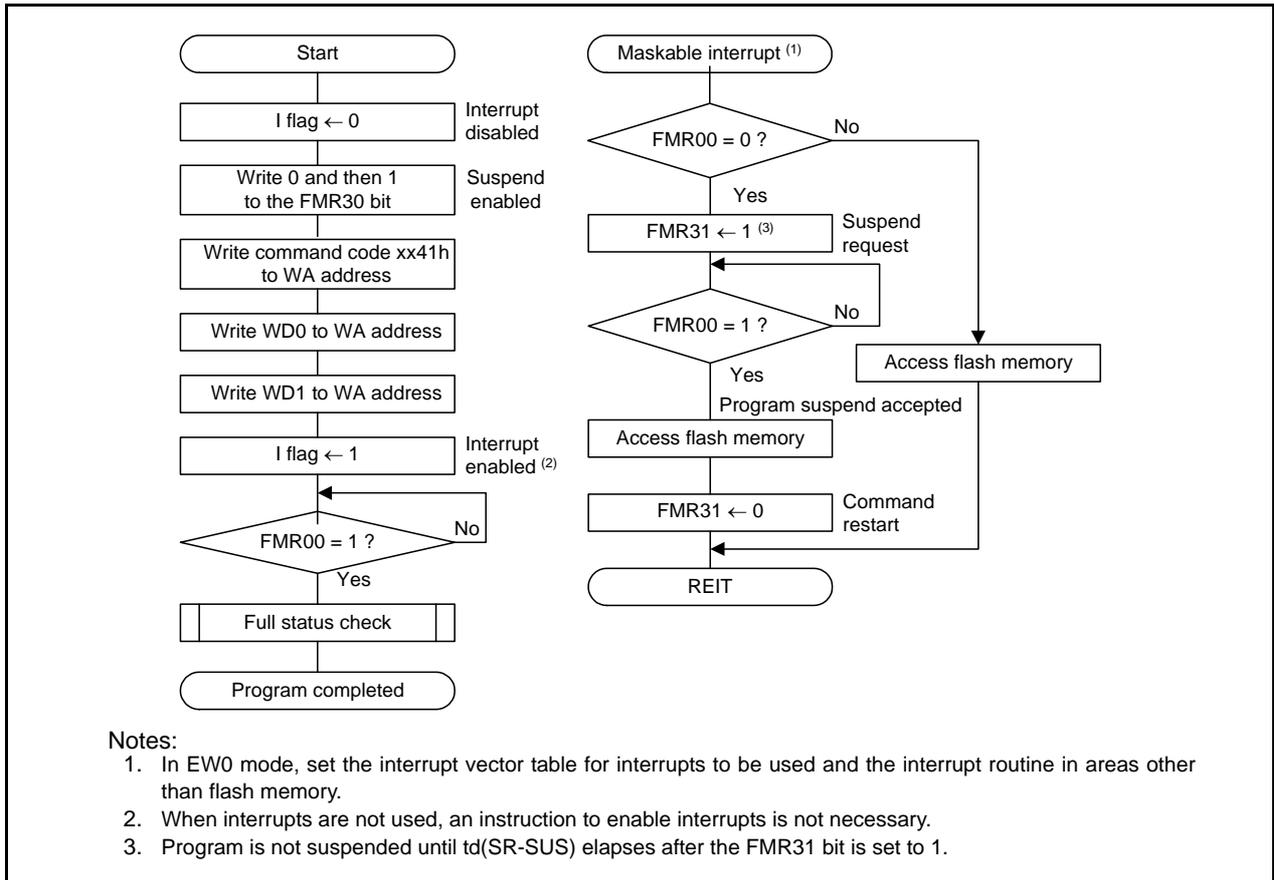
Modified figures

- Program Flowchart in EW1 Mode (Suspend Function Enabled)
- Block Erase Flowchart in EW1 Mode (Suspend Function Enabled)
- Lock Bit Program Flowchart in EW1 Mode (Suspend Function Enabled)

Modification

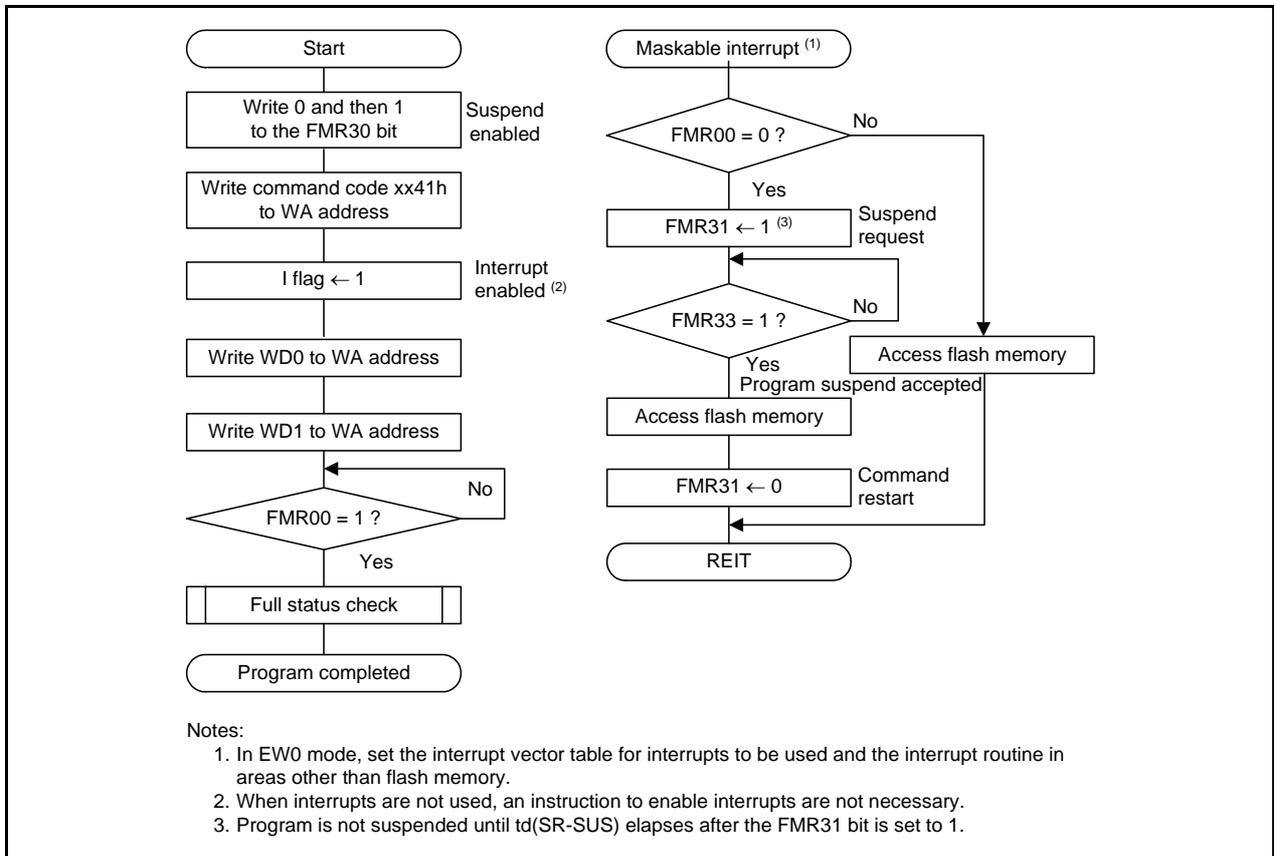
- The timing to set the I flag to 1 (interrupt enabled) has been changed.

Post modification



Program Flowchart in EW0 Mode (Suspend Function Enabled)

Premodification



Program Flowchart in EW0 Mode (Suspend Function Enabled)

4. Additions and Changes on Electrical Characteristics

4.1 Recommended Operating Condition for VCC

➔ 27.1.2 Recommended Operating Conditions

The characteristic of the minimum value for the V_{CC} power supply has been modified.

Symbol	Characteristic	Standard				Unit
		Min.		Typ.	Max.	
		Before	After			
V _{CC}	Supply voltage	3.0	2.7		5.5	V

4.2 Voltage Detector 2

➔ 27.1.5 Voltage Detector and Power Supply Circuit Electrical Characteristics

The characteristics of Vdet2_0 to Vdet2_3, and Vdet2_5 to Vdet2_7 for voltage detector 2 have been added.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2_0	Voltage detection level Vdet2_0	When V _{CC} is falling		3.21		V
Vdet2_1	Voltage detection level Vdet2_1			3.36		V
Vdet2_2	Voltage detection level Vdet2_2			3.51		V
Vdet2_3	Voltage detection level Vdet2_3			3.66		V
Vdet2_5	Voltage detection level Vdet2_5			3.96		V
Vdet2_6	Voltage detection level Vdet2_6			4.10		V
Vdet2_7	Voltage detection level Vdet2_7			4.25		V

4.3 Power Supply Circuit Timing Characteristics

➔ 27.1.5 Voltage Detector and Power Supply Circuit Electrical Characteristics

The maximum value of t_{d(W-S)} has been modified.

Symbol	Parameter	Measuring Condition	Standard				Unit
			Min.	Typ.	Max.		
					Before	After	
t _{d(W-S)}	Low power mode wait mode release time	V _{CC} = 3.0 V to 5.5V			150	300	μs

4.4 Oscillator

➔ 27.1.6 Oscillator Electrical Characteristics

The characteristic of the dedicated 125 kHz on-chip oscillator for the watchdog timer has been added.

Symbol	Characteristic	Standard			Unit
		Min.	Typ.	Max.	
f _{WDT}	Dedicated 125 kHz on-chip oscillator for the watchdog timer oscillation frequency	100	125	150	kHz

4.5 Hysteresis V_{T+} - V_{T-} for TA0IN and others

➔ 27.2.1 Electrical Characteristics (VCC = 5 V)

The maximum value of the following V_{T+} - V_{T-} hysteresis has been changed.

Symbol	Parameter	Measuring Condition	Standard				Unit
			Min.	Typ.	Max.		
					Before	After	
V_{T+} - V_{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB2IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS3, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0	0.2		2.5	$0.4V_{CC}$	V

➔ 27.3.1 Electrical Characteristics (VCC = 3 V)

The maximum value of the following V_{T+} - V_{T-} hysteresis has been changed.

Symbol	Parameter	Measuring Condition	Standard				Unit
			Min.	Typ.	Max.		
					Before	After	
V_{T+} - V_{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB2IN, INT0 to INT5, NMI, ADTRG, CTS0 to CTS3, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0			1.8	$0.4V_{CC}$	V

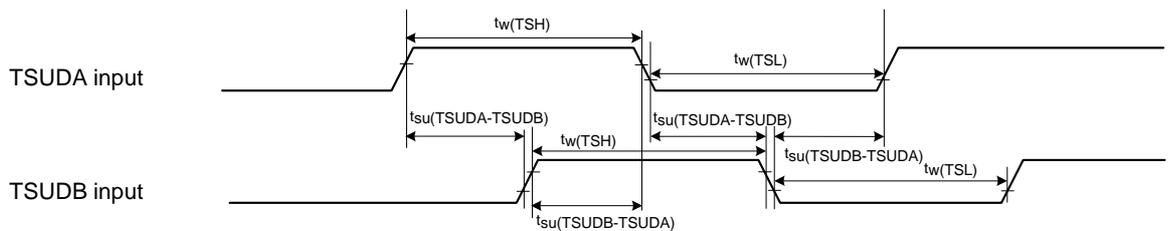
4.6 Two-Phase Pulse in Timer S

➔ 27.2.2.5 Timer S Input, 27.3.2.5 Timer S Input

The characteristics of two-phase pulse input in two-phase pulse signal processing mode have been added. Also the pin name TSUDA has been added to P8_0, and TSUDB to P8_1.

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		μ s
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		μ s
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		μ s
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		μ s

Two-phase pulse input in two-phase pulse signal processing mode



Note:

- When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.