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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A869A/E	Rev.	1.00
Title	Description Omitted from the Hardware Manual Regarding the Condition for Clearing the TEND Bit, TDRE Bit, and RDRF Bit in the SSU Module		Information Category	Technical Notification		
Applicable Product	SH7280 Series	Lot No. All lots	Reference Document	SH7280 Group, SH7243 Group User's Manual: Hardware (R01UH0229EJ0300)		

In the description of the condition for clearing the TEND bit, TDRE bit, and RDRF bit in the SSU module of the above products, a statement of the need to set the FCLRM bit was unfortunately omitted. Therefore, we will be amending the descriptions.

[Contents]

18.3.5 SS Status Register (SSSR)

Erroneous:

Bit	Bit Name	Initial Value	R/W	Description
3	TEND	0	R/W	Transmit End [Setting conditions] • When the last bit of transmit data is transmitted while the TENDSTS bit in SSCR2 is cleared to 0 and the TDRE bit is set to 1 • After the last bit of transmit data is transmitted while the TENDSTS bit in SSCR2 is set to 1 and the TDRE bit is set to 1 [Clearing conditions] • When writing 0 after reading TEND = 1 • When writing data to SSTDR
2	TDRE	1	R/W	Transmit Data Empty Indicates whether or not SSTDR contains transmit data. [Setting conditions] • When the TE bit in SSER is 0 • When data is transferred from SSTDR to SSTRSR and SSTDR is ready to be written to. [Clearing conditions] • When writing 0 after reading TDRE = 1 • When writing data to SSTDR with TE = 1 • When transmit data is written to SSTDR while the DMAC is activated by an SSTXI. • When transmit data is written to SSTDR while the DISEL bit in MRB of the DTC is 0 if the DMAC/DTC is activated by an SSTXI interrupt and then DMAC is activated.
1	RDRF	0	R/W	Receive Data Register Full Indicates whether or not SSRDR contains receive data. [Setting condition] • When receive data is transferred from SSTRSR to SSRDR after successful serial data reception [Clearing conditions] • When writing 0 after reading RDRF = 1 • When reading receive data from SSRDR • When transmit data is read into SSRDR while the DISEL bit in MRB of the DTC is 0 if the DMAC/DTC is activated by an SSRXI interrupt and then DTC is activated

Corrected:

Bit	Bit Name	Initial Value	R/W	Description
3	TEND	0	R/W	Transmit End [Setting conditions] • When the last bit of transmit data is transmitted while the TENDSTS bit in SSCR2 is cleared to 0 and the TDRE bit is set to 1 • After the last bit of transmit data is transmitted while the TENDSTS bit in SSCR2 is set to 1 and the TDRE bit is set to 1 [Clearing conditions] • When writing 0 after reading TEND = 1 • When writing data to SSTDR with FCLRM =1 • When transmit data is written to SSTDR while the DMAC is activated by an SSTXI with FCLRM =1. • When the DTC is activated by an SSTXI interrupt and transmit data is written to SSTDR while the DISEL bit in MRB of the DTC is 0 (except when DTC transfer counter value is H'0000)*1
2	TDRE	1	R/W	Transmit Data Empty Indicates whether or not SSTDR contains transmit data. [Setting conditions] • When the TE bit in SSER is 0 • When data is transferred from SSTDR to SSTRSR and SSTDR is ready to be written to. [Clearing conditions] • When writing 0 after reading TDRE = 1 • When writing data to SSTDR with TE = 1 and FCLRM = 1 • When transmit data is written to SSTDR while the DMAC is activated by an SSTXI with FCLRM =1. • When the DTC is activated by an SSTXI interrupt and transmit data is written to SSTDR while the DISEL bit in MRB of the DTC is 0 (except when DTC transfer counter value is H'0000)*1
1	RDRF	0	R/W	Receive Data Register Full Indicates whether or not SSRDR contains receive data. [Setting condition] • When receive data is transferred from SSTRSR to SSRDR after successful serial data reception [Clearing conditions] • When writing 0 after reading RDRF = 1 • When reading receive data from SSRDR with FCLRM =1 • When receive data is read from SSRDR while the DMAC is activated by an SSRXI with FCLRM =1. • When the DTC is activated by an SSRXI interrupt and receive data is read into SSRDR while the DISEL bit in MRB of the DTC is 0 (except when DTC transfer counter value is H'0000)*1

Note: *1 Clearing the FCLRM bit to 0 enables transfer by the DTC.

18.4.5 SSU Mode

Erroneous:

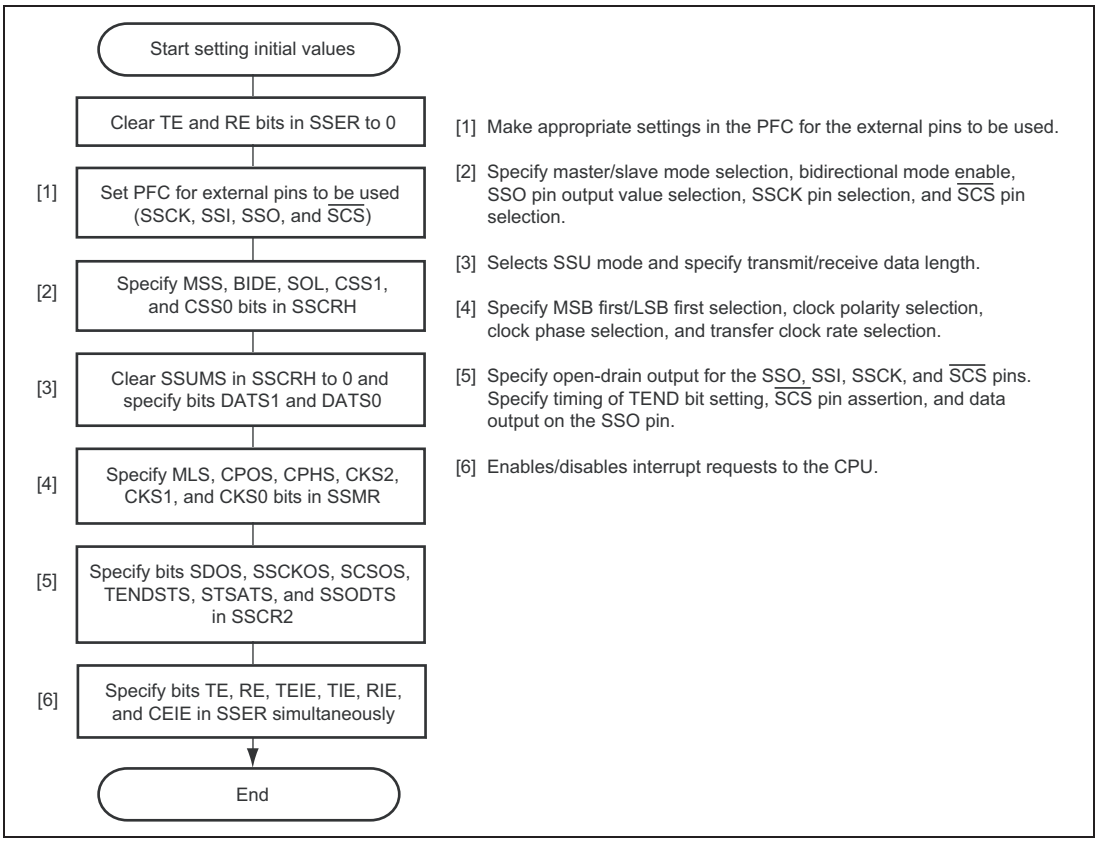

Figure 18.4 Example of Initial Settings in SSU Mode

Corrected:

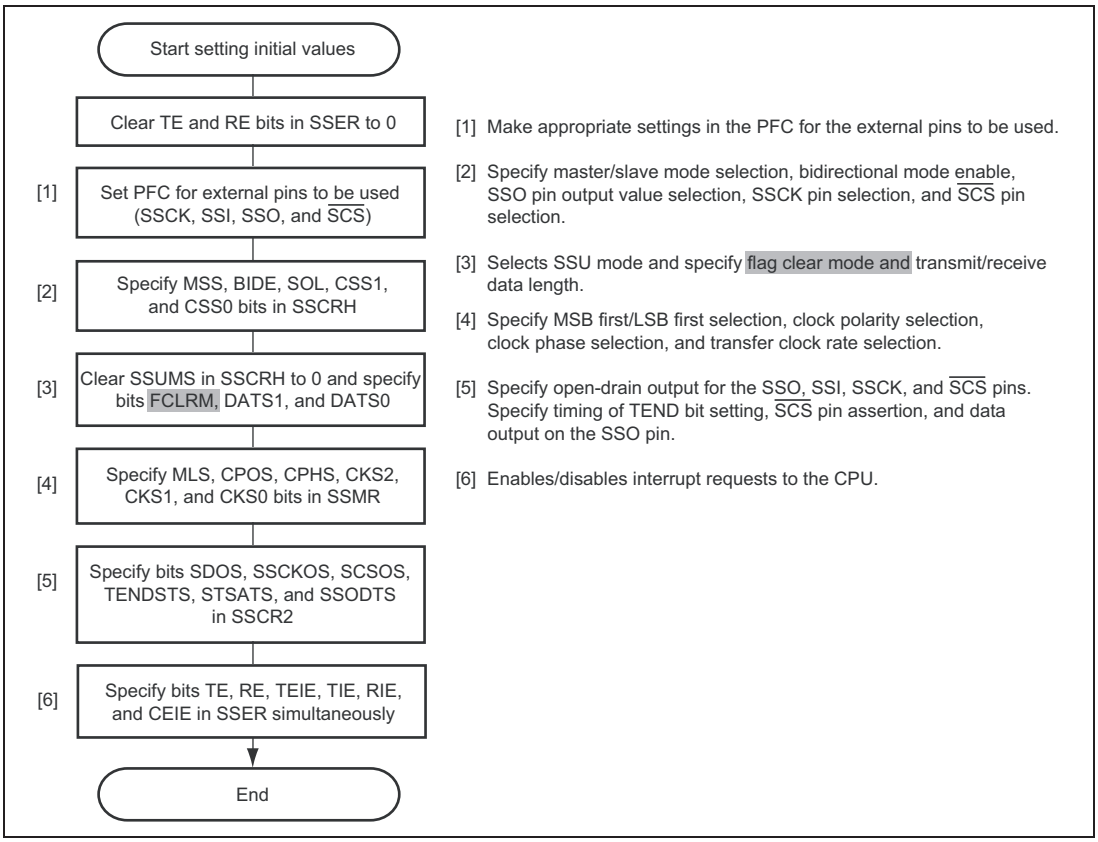

Figure 18.4 Example of Initial Settings in SSU Mode

18.4.7 Clock Synchronous Communication Mode

Erroneous:

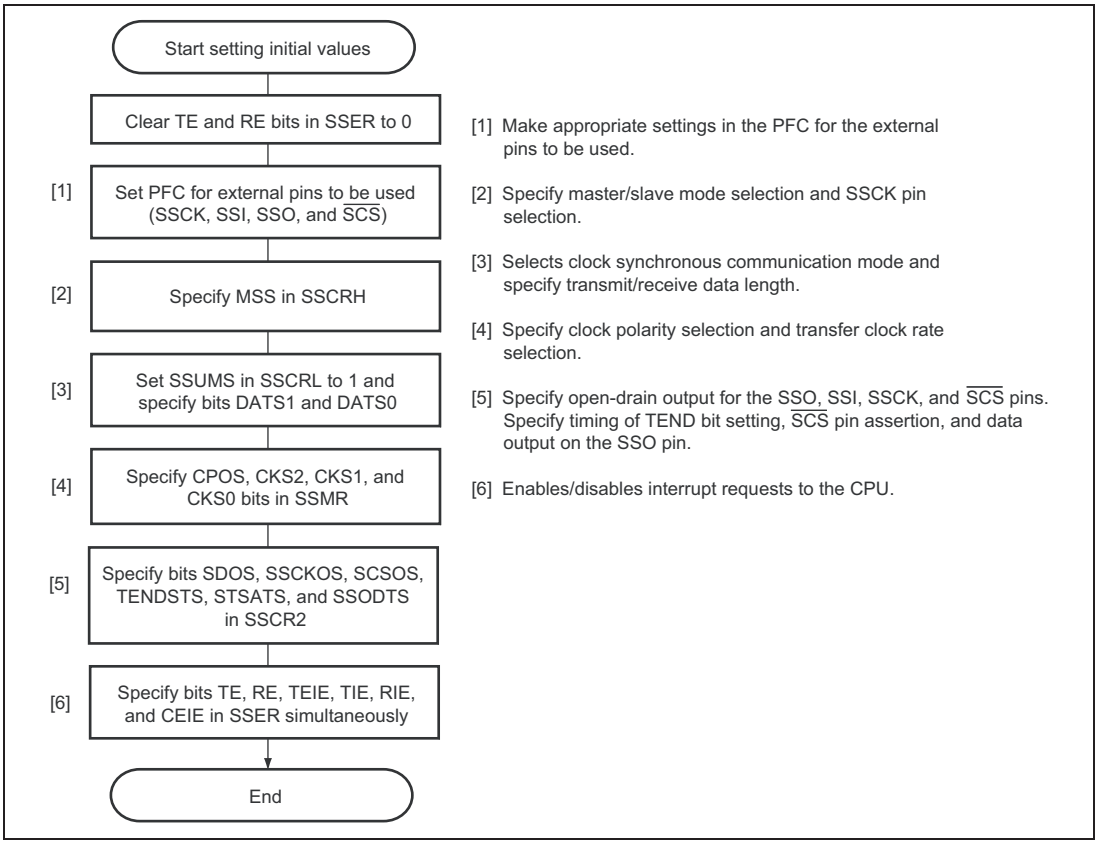

Figure 18.12 Example of Initial Settings in Clock Synchronous Communication Mode

Corrected:

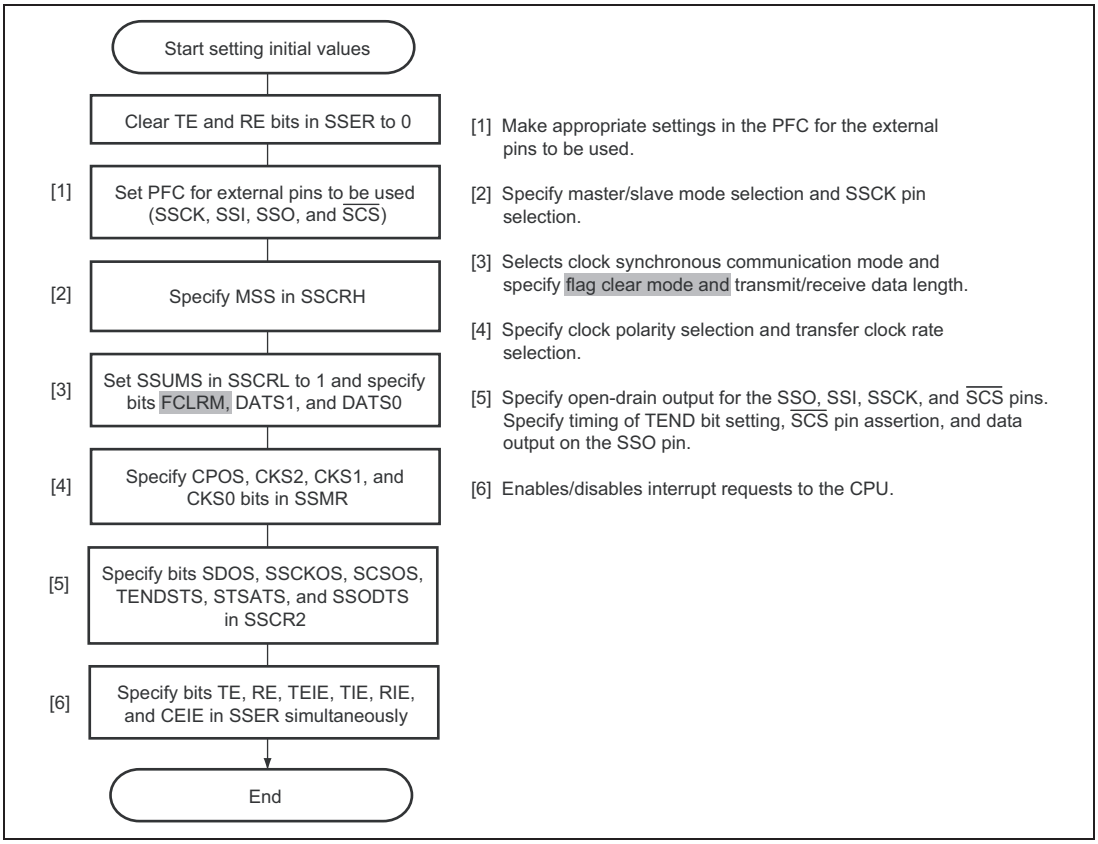

Figure 18.12 Example of Initial Settings in Clock Synchronous Communication Mode