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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-RH8-B0506A/E	Rev.	1.00	
Title	Description change of specification of Embed Voltage Regulator (eVR)	Information Category	Technical Notification			
		Lot No.		· RH850/P1x-C Group Use		
Applicable Product	RH850/P1x-C, RH850/P1L-C,	All lot	Reference Document	Hardware, R01UH04 • RH850/P1L-C Group Hardware, R01UH04	490EJ014 o User's I	40 Manual:

This technical update reports the following issue of Embedded Voltage Regulator (eVR).

1. Phenomenon

The specification of Embedded Voltage Regulator (eVR) was revised as the result of discussion with customer based on customer's PCB design experience.

Therefore, the descriptions of the eVR characteristics are updated in the User's manual Hardware. Please consider this content to use the applicable products.

2. User's Manual Update

The following descriptions will be modified in the User's Manual (Red character)

2-1 RH850/P1x-C

Section 36 Electrical Specifications

36.3.2 Embedded Voltage Regulator (eVR) Characteristics

Table 36.7 Embedded Voltage Regulator (eVR) Characteristics

<Before>

Table 36.7 Embedded Voltage Regulator (eVR) Characteristics*1

Item	Symbol	Comment	Condition	MIN.	TYP.	MAX.	Unit
Total capacitance connected	CRVCLT	D3 (QFP)	*3	240	500	720	nF
to the VCL pins of a device*2		D3 (BGA-292)	*3	240	500	720	nF
ESR of external buffer capacitance	RESR	ESR of one CRVCL capacitor	f0 = 100kHz			50	mΩ

Note 1. Please refer to **Table 36.6**, for the slew rate specification of the supply voltage.

Note 2. The total capacitance for the device has to be distributed evenly to all VCL pins.

Note 3. Disconnection of a capacitor to a VCL pin or ball is acceptable. For details refer to **Section 2**, **Pin Functions**.

<After>

Table 36.7 Embedded Voltage Regulator (eVR) Characteristics*1

Item	Symbol	Comment	Condition	MIN.	TYP.	MAX.	Unit
	CRVCLT	D3 (QFP)	*3 *4	240	500	720	nF
to the VCL pins of a device*2 *	5 10	D3 (BGA-292)	*3 *4	240	500	720	nF

- Note 1. Please refer to Table 36.6, for the slew rate specification of the supply voltage.
- Note 2. The total capacitance for the device has to be distributed evenly to all VCL pins.
- Note 3. Disconnection of a capacitor to a VCL pin or ball is acceptable. For details refer to **Section 2, Pin Functions**.
- Note 4. Minimum and maximum value of CRVCLT include disconnection of a capacitor, initial tolerance and deratings of temperature, voltage and aging.
- Note 5. Low ESR ceramic capacitor (e.g., X7R, X8R) must be used.
- Note 6. Each capacitor must place to each VCL and VSS pin as close as possible to avoid unproper operation such as worse EMC performance and unintended CVM detection. And proper operation should be verified under actual conditions prior. It is strongly recommended that effective ESR for each capacitor including PCB trace is less than $75 \text{m}\Omega$. This value is confirmed by Bosch's field experience with two digit million ECUs. Effective ESR should be measured between VCL and related VSS pin.

2-2 RH850/P1L-C

Section 31 Electrical Specifications

31.3.2 Embedded Voltage Regulator (eVR) Characteristics

Table 31.7 Embedded Voltage Regulator (eVR) Characteristics

<Before>

Table 31.7 Embedded Voltage Regulator (eVR) Characteristics^{*1}

Item	Symbol	Comment	Condition	MIN.	TYP.	MAX.	Unit
Internal core voltage	VDD			1.20	1.25	1.35	V
Total capacitance connected	CRVCLT	D1 (QFP80)		180	400	600	nF
to the VCL pins of a device*2		D1 (QFP100)		180	400	600	nF
		D2 (QFP100)		180	400	600	nF
		D2 (QFP144)	*3	240	500	720	nF
ESR of external buffer capacitance	RESR	ESR of one CRVCL capacitor	f0 = 100kHz			50	mΩ

- Note 1. Please refer to **Table 31.6**, for the slew rate specification of the supply voltage.
- Note 2. The total capacitance for the device has to be distributed evenly to all VCL pins.
- Note 3. Disconnection of a capacitor to a VCL pin or ball is acceptable. For details refer to **Section 2**, **Pin Functions**.

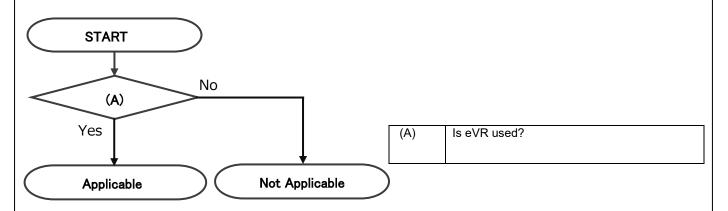
<After>

Table 31.7 Embedded Voltage Regulator (eVR) Characteristics*1

Item	Symbol	Comment	Condition	MIN.	TYP.	MAX.	Unit
Internal core voltage	VDD			1.20	1.25	1.35	V
	CRVCLT	D1 (QFP80)	*7	180	400	600	nF
to the VCL pins of a device*2 *5		D1 (QFP100)	*7	180	400	600	nF
		D2 (QFP100)	*7	180	400	600	nF
		D2 (QFP144)	*3 *4	240	500	720	nF

- Note 1. Please refer to Table 31.6, for the slew rate specification of the supply voltage.
- Note 2. The total capacitance for the device has to be distributed evenly to all VCL pins.
- Note 3. Disconnection of a capacitor to a VCL pin or ball is acceptable. For details refer to **Section 2**, **Pin Functions**.
- Note 4. Minimum and maximum value of CRVCLT include disconnection of a capacitor, initial tolerance and deratings of temperature, voltage and aging.
- Note 5. Low ESR ceramic capacitor (e.g., X7R, X8R) must be used.
- Note 6. Each capacitor must place to each VCL and VSS pin as close as possible to avoid unproper operation such as worse EMC performance and unintended CVM detection. And proper operation should be verified under actual conditions prior. It is strongly recommended that effective ESR for each capacitor including PCB trace is less than $75m\Omega$. This value is confirmed by Bosch's field experience with two digit million ECUs. Effective ESR should be measured between VCL and related VSS pin.
- Note 7. Minimum and maximum value of CRVCLT include initial tolerance and derating of temperature, voltage and aging.

3. User's Manual Update



4. Future Action

For the user's manual, the descriptions of red characters will be released by errata.

<Reference Documents>

Series	Group	Document Title	Rev.	Document Number
RH850	P1x-C	RH850/P1x-C Group User's Manual: Hardware	1.40	R01UH0490EJ0140
RH850	P1L-C	RH850/P1L-C Group User's Manual: Hardware	1.20	R01UH0591EJ0120