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# RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-RH8-B0195A/E	Rev.	1.00	
Title	Description change of PBGxx Error Address Register		Information Category	Technical Notification		
Applicable Product	RH850/C1H RH850/C1M	Lot No.	Reference Document	RH850/C1x User's Manual: Hardware Rev.1.60(R01UH0414EJ0160)		

There are description changes in the RH850/C1x User's Manual and this RENESAS Technical update describes these changes.

#### 1. Contents of modification

Section 27 Safety, 27.4.3 PBG, (4) ERRSLVxxADDR — PBGxx Error Address Register (Page 2113 of 2373) Change the description of the red frame below to the description of the blue frame.

### · Original contents:

## (4) ERRSLVxxADDR — PBGxx Error Address Register

ERRSLVxxADDR holds the address of the illegal access rejected with the PBGxx.

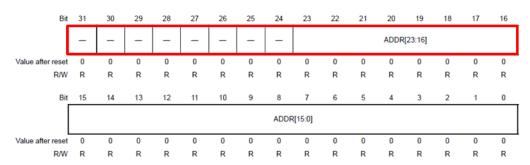


Table 27.97 ERRSLVxxADDR Register Contents

Bit Position	Bit Name	Function
31 to 24	_	Reserved. These bits are always read as 0. The write value should also be 0.
23 to 0	ADDR[23:0]	When an illegal access occurs, the access address is calculated by addition of FF00 $0000_{\rm H}$ to read value of these bits.

- · Modification contents:
  - (4) ERRSLVxxADDR PBGxx error address register

ERRSLVxxADDR holds the address of the illegal access rejected with the PBGxx

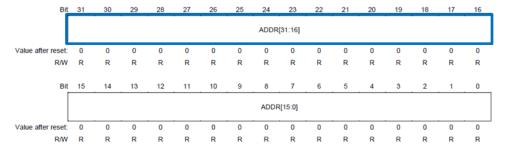


Table 27.97 ERRSLVxxADDR Register Contents

Bit Position	Bit Name	Function
31 to 0	ADDR[31:0]	Address at which an error has occurred.  CAUTION
		ADDR[31:24] of PBG 2 to 5 are fixed to 0. Access address is calculated by addition of FF00 $0000_{\text{H}}$ to read value of these bits.

## 2. Final handling

With the next User's Manual revision, we will modify the descriptions shown.