To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1st, 2010
Renesas Electronics Corporation

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Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	23th, June, 1998	No.	TN-PSC-334A/E
THEME	The corrections (3) of HD64572 SCA-II User's Manual .		
CLASSIFICATION	☐ Spec. change ☐ Limitation on Use ☐ Supplement of Documents ■ Correction		
PRODUCT NAME	HD64572FL33 , HD64572AFL33	Lot No.etc.	All lots
REFERENCE DOCUMENTS	———	Effective Date	forever
		From	Now

There are some misprint and insufficiency of Usage Notes ,Notes in HD64572 SCA-II User's Manual, please make correct it described as below.
Please, take notice of this HITACHI SEMICONDUCTOR TECHNICAL UPDATE.

Section 1 Overview

1.7 Overview of Functions

1.7.6 Maximum Bit Rates ··· page 30

(Current)

Table 1-4 shows the maximum bit rates supported by the MSCI in the SCA-II.

Table 1-4 Maximum Bit Rates

(Corrected)

Table 1-4-1 and Table 1-4-2 shows the maximum bit rates supported by the MSCI in the SCA-II.

HD64572FL33(25Mbps)

Table 1-4-1 Maximum Bit Rates

(Current)

			Maximum Bit Rate (bps)								
					Clock Extraction					
					Sampling Clock: External*4			Sampling Clock: BRG*5, *6		
fφ	Protocol Mode	Clock Mode*7	External Clock	BRG	×8	×16	×32	×8	×16	×32
33.3MHz	Asynchronous	1/64	208K*1	260K*3	—	—	—	—	—	—
		1/32	416K*1	521K*3	—	—	—	—	—	—
		1/16	832K*1	1042K*3	—	—	—	—	—	—
		1/1	13.3M*1	11.1M*8	—	—	—	—	—	—
	Byte synchronous	1/1	25.0M*2	16.7M*3	4.16M*9	2.5M	1.25M	4.16M	2.08M	1.04M
	Bit synchronous	1/1	25.0M*2	16.7M*3	4.16M*9	2.5M	1.25M	4.16M	2.08M	1.04M

(Corrected)

			Maximum Bit Rate (bps)								
					Clock Extraction					
					Sampling Clock: External*4			Sampling Clock: BRG*5, *6		
fφ	Protocol Mode	Clock Mode*7	External Clock	BRG	×8	×16	×32	×8	×16	×32
33.3MHz	Asynchronous	1/64	208K*1	260K*3	—	—	—	—	—	—
		1/32	416K*1	521K*3	—	—	—	—	—	—
		1/16	832K*1	1042K*3	—	—	—	—	—	—
		1/1	13.3M*1	11.1M*8	—	—	—	—	—	—
	Byte synchronous	1/1	25.0M*2	16.7M*3	4.16M*9	2.5M	1.25M	4.16M	2.08M	1.04M
	Bit synchronous	1/1	25.0M*2	16.7M*3	4.16M*9	2.5M	1.25M	4.16M	2.08M	1.04M
	Transparent	1/1	25.0M*2	16.7M*3	4.16M*9	2.5M	1.25M	4.16M	2.08M	1.04M

HD64572AFL33 (30Mbps)

Table 1-4-2 Maximum Bit Rates

			Maximum Bit Rate (bps)								
					Clock Extraction					
					Sampling Clock: External*4			Sampling Clock: BRG*5, *6		
f ϕ	Protocol Mode	Clock Mode*7	External Clock	BRG	×8	×16	×32	×8	×16	×32
33.3MHz	Asynchronous	1/64	208K*1	260K*3	—	—	—	—	—	—
		1/32	416K*1	521K*3	—	—	—	—	—	—
		1/16	832K*1	1042K*3	—	—	—	—	—	—
		1/1	13.3M*1	11.1M*8	—	—	—	—	—	—
	Byte synchronous	1/1	30.0M*2	16.7M*3	4.16M*9	2.5M	1.25M	4.16M	2.08M	1.04M
	Bit synchronous	1/1	30.0M*2	16.7M*3	4.16M*9	2.5M	1.25M	4.16M	2.08M	1.04M
	Transparent	1/1	30.0M*2	16.7M*3	4.16M*9	2.5M	1.25M	4.16M	2.08M	1.04M

Notes : f ϕ : System clock frequency

1. f ϕ ÷2.5× (clock mode)
2. f ϕ ÷1.11× (clock mode)
3. f ϕ ÷2× (clock mode)
4. 40 Mbps÷ (sampling clock multiplier)
5. f ϕ ÷ (sampling clock multiplier)
6. Same maximum bit rate when receive clock noise is suppressed
7. Specified by MSCI mode register 1 (MD1)
8. f ϕ ÷3
9. f ϕ ÷8, in×8 mode, a clock up to the same frequency as f ϕ (33.3 MHz) can be input as the external clock.

Section 3 System Controller

3.6 Wait Controller

3.6.5 Usage Note ··· page 101

(Current)

If wait state insertion by register control and wait state insertion by means of the WAIT pin occur simultaneously, the number of wait states specified by the register are inserted. If there is a WAIT pin request for a number of states exceeding that specified by the register, wait states are added in accordance with this request.

(Corrected)

If wait state insertion by register control and wait state insertion by means of the WAIT pin occur simultaneously, the number of wait states specified by the register are inserted. If there is a WAIT pin request for a number of states exceeding that specified by the register, wait states are added in accordance with this request.

The number of wait states insertion by Wait Control Registers H, M, L (WCRH, WCRM, WCRL) and the number of wait states insertion by means of the WAIT pin are equal to or smaller than Back-Off Length Register (BOLR) set value.

When the number of wait states insertion by Wait Control Registers H, M, L (WCRH, WCRM, WCRL) and the number of wait states insertion by means of the WAIT pin are equal to or greater than Back-Off Length Register (BOLR) set value, normal DMA operation is not guaranteed.

Section 5 Multiprotocol Serial Communication Interface (MSCI)

5.2 Registers

5.2.5 MSCI Control Register (CTL)

Bit 7 — Underrun Request Control (URCT) ··· page 173

(Current)

URCT	Description
0	DMA requests are halted when underrun occurs with URSKP=0.
1	DMA requests continue to be issued when underrun occurs with URSKP=0.

(Corrected)

URCT	Description
0	DMA request and DMA critical request are halted when underrun occurs with URSKP=0.
1	DMA request continue to be issued when underrun occurs with URSKP=0.

Bit 6 — Underrun Remaining Data Skip (URSKP)

(Current)

When underrun occurs, the UDRN bit is set to 1 in status register 1 (ST1), the TX disable state is entered, and writing from the MPU to the transmit buffer is disabled. Writing to the transmit buffer is enabled again by clearing the UDRN bit to 0.

(Corrected)

When underrun occurs, the UDRN bit is set to 1 in status register 1 (ST1), the Idle state is entered, and writing from the MPU to the transmit buffer is disabled. Writing to the transmit buffer is enabled again by clearing the UDRN bit to 0.

(Current)

URSKP	URCT	Description
0	0	When underrun occurs, DMA requests are halted and transfer is aborted.
	1	When underrun occurs, the remaining data in the frame following the underrun is retained and transferred to the TX FIFO. As a result, this data is transferred as a separate frame from that prior to the underrun.
1	*	When underrun occurs, the remaining data in the frame is skipped. In chained-block transfer mode, the remaining data in the frame following underrun is skipped, and the DMAC continues transfer from the start of the next frame. In single transfer mode, the remaining data in the frame following underrun is skipped, and the DMAC stops.

* : Don't care

(Corrected)

URSKP	URCT	Description
0	0	When underrun occurs, DMA request and DMA critical request are halted and transfer is aborted.
	1	When underrun occurs, only DMA request continue to be issued and the remaining data in the frame following the underrun is retained and transferred to the TX FIFO. As a result, this data is transferred as a separate frame from that prior to the underrun.
1	0	When underrun occurs, only DMA request continue to be issued. In chained-block transfer mode, the remaining data in the frame following underrun is skipped, and the DMAC continues transfer from the start of the next frame. In single transfer mode, if underrun occurs, the remaining data in the frame following the underrun is retained and transferred to the TX FIFO. As a result, this data is transferred as a separate frame from that prior to the underrun.
	1	When underrun occurs, DMA request and DMA critical request continus to be issued. In chained-block transfer mode, the remaining data in the frame following underrun is skipped, and the DMAC continues transfer from the start of the next frame. In single transfer mode, if underrun occurs, the remaining data in the frame following the underrun is retained and transferred to the TX FIFO. As a result, this data is transferred as a separate frame from that prior to the underrun.

5.2.42 MSCI C Transmit DMA Request Control Register 1 (TNR1)
Bits 13 to 8 — TX DMA Request Control 1 (TNR15 - TNR10) : ··· page 269

(Current)

・Asynchronous/byte synchronous/bit synchronous/transparent mode

Bits TNR15 — TNR10 determine the condition for canceling an MSCI transmit DMA request. When the number of data bytes in the transmit buffer is equal to or greater than the TNR15 — TNR10 set value +1, the MSCI cancels its transmit DMA requst. Any value from 00H to 3FH can be set.

When (TNR15 — TNR10 set value)≦(TNR05 — TNR00 set value), the operation is the same as when (TNR15 — TNR10 set value)=(TNR05 — TNR00 set value)(a request is canceled immediately after completion of the DMA transfer initiated by that request).

(Corrected)

・Asynchronous/byte synchronous/bit synchronous/transparent mode

Bits TNR15 — TNR10 determine the condition for canceling an MSCI transmit DMA request. When the number of data bytes in the transmit buffer is equal to or greater than the TNR15 — TNR10 set value +1, the MSCi cancels its transmit DMA requst*. Any value from 00H to 3FH can be set**.

Notes : * When (TNR15 — TNR10 set value)<(TNR05 — TNR00 set value), when the number of data bytes in the transmit buffer is equal to or greater than the TNR05 — TNR00 set value +1, the MSCI cancels its transmit DMA request.

** When Burst Enable (COTE) of DMA Priority Control Register (PCR) set to "1", TNR15 — TNR10 set from 00H to34H.
When TNR15 — TNR10 set value is equal to or greater than 35H, normal transmit DMA operation is not guaranteed.

Section 6 Direct Memory Access Controller(DMAC)

6.2 Registers

6.2.7 DMA Status Register (DSR)

Bit 26/18/10/2 — Underrun Frame/Receive Error Frame (UDRF/REF)

Usage Notes : ··· page 362

(Current)

If the URSKP bit is 1, the transfer is aborted and data is skipped up to a descriptor with the EOM bit set to 1 in the status information ([4] , [5]). At this time, the UDR bit is set to 1 in the status information of the skipped descriptor.

(Corrected)

If the URSKP bit is 1, the transfer is aborted and data is skipped up to a descriptor with the EOM bit set to 1 in the status information ([4] , [5]). At this time, the UDR bit is set to 1 in the status information of the skipped descriptor*3.

Notes : 1. If the URSKP bit is set to 1 in the MSCI's internal control register (CTL) while the

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2. If underrun occurs when the URSKP bit is 0 (no skip) in chained-block transfer mode,

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3. When using the underrun skip mode, please use the EDA to prevent the over-access of the descriptors, and please use the ownership bit (OSB) and underrun bit (UDR) of the status of the descriptor to notice the underrun. And please check the data of the underrun frame, if the data is to be used again.

When the underrun occurs, the status may not be written by the DMAC into the descriptor. But, if the status is not written by the malfunction, the ownership bit is not written to "1", either.

The fact of the underrun is known by "0" of the ownership bit in the descriptor status which should have been accessed.

If the ownership bit is written to "1", the underrun bit of the status of the descriptor indicates the correct status.