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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A788A/E	Rev.	1.00
Title	Corrections to the Usage Notes and Hardware Manual concerning output waveform control during synchronous counter clear operations in the MTU2 and MTU2S complementary PWM mode.		Information Category	Technical Notification		
Applicable Product	See below	Lot No. All	Reference Document	See below		

This Technical Update corrects errors in the Usage Notes and Hardware Manual for the MTU2 and MTU2S circuits included in the applicable products listed below.

Usage Notes

In complementary PWM mode, when output waveform control during synchronous counter clearing is enabled (WRE in the TWCR register set to 1), the following problems may occur when condition (1) or condition (2), below, is satisfied.

- Dead time for the PWM output pins may be too short (or nonexistent).
- Active-level output from the PWM negative-phase pins may occur outside the correct active-level output interval

Condition (1): When synchronous clearing occurs in the PWM output dead time interval within initial output suppression interval (10) (figure 1).

Condition (2): When synchronous clearing occurs within initial output suppression interval (10) or (11) and TGRB_3 ≤ TDDR, TGRA_4 ≤ TDDR, or TGRB_4 ≤ TDDR is true (figure 2).

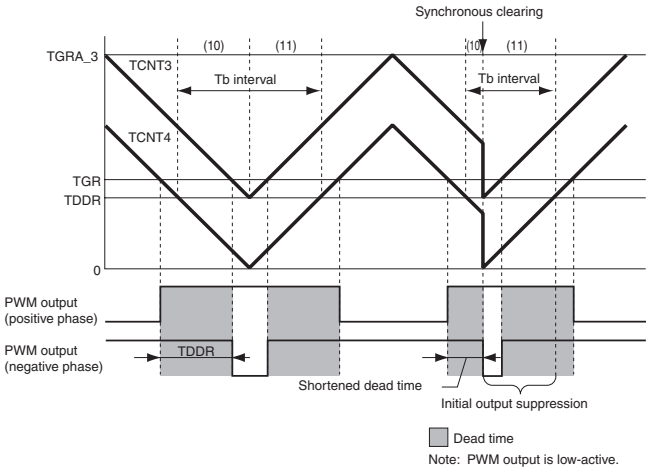

Figure 1 Condition (1) Synchronous Clearing Example

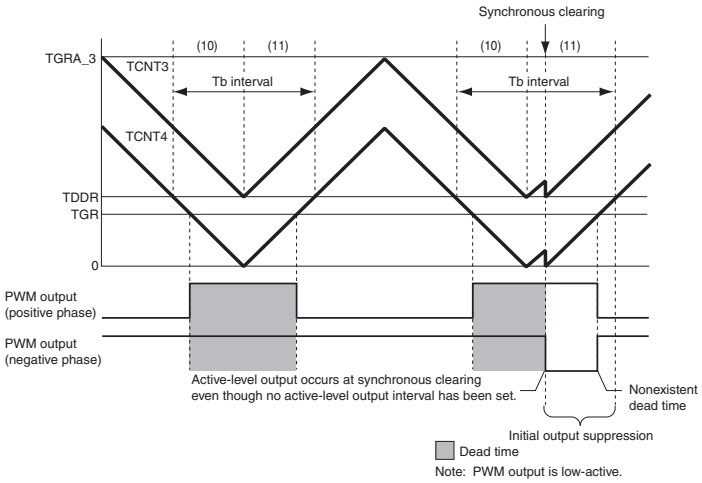

Figure 2 Condition (2) Synchronous Clearing Example

Workaround

The following workaround can be used to avoid these problems.

When using synchronous clearing, make sure to set compare registers TGRB_3, TGRA_4, and TGRB_4 to a value twice or more the setting of dead time data register TDDR.

Corrections to Hardware Manual Errors

This section corrects errors in the hardware manuals listed in the references (related documents) column. The following shows the correction for the SH7080 Series products, which is representative of the correction to these products.

The following correction applies to subsection 11.3.32, Timer Waveform Control Register (TWCR), in Section 11, Multifunction Timer Pulse Unit 1 (MTU2), in the SH7080 Group Hardware Manual.

Incorrect

Bit	Bit Name	Initial Value	R/W	Description
0	WRE	0	R/(W)	Waveform Retain Enable Selects the waveform output when synchronous counter clearing occurs in complementary PWM mode. The output waveform is retained only when synchronous clearing occurs within the Tb interval at the trough in complementary PWM mode. When synchronous clearing occurs outside this interval, the initial value specified in TOCR is output regardless of the WRE bit setting. The initial value is also output when synchronous clearing occurs in the Tb interval at the trough immediately after TCNT_3 and TCNT_4 start operation. For the Tb interval at the trough in complementary PWM mode, see figure 11.40. 0: Outputs the initial value specified in TOCR 1: Retains the waveform output immediately before synchronous clearing [Setting condition] • When 1 is written to WRE after reading WRE = 0

Correct

Bit	Bit Name	Initial Value	R/W	Description
0	WRE	0	R/(W)	Initial Output Suppression Enable Selects the waveform output when synchronous counter clearing occurs in complementary PWM mode. The initial output is suppressed only when synchronous clearing occurs within the Tb interval at the trough in complementary PWM mode. When synchronous clearing occurs outside this interval, the initial value specified in TOCR is output regardless of the WRE bit setting. The initial value is also output when synchronous clearing occurs in the Tb interval at the trough immediately after TCNT_3 and TCNT_4 start operation. For the Tb interval at the trough in complementary PWM mode, see figure 11.40. 0: Outputs the initial value specified in TOCR 1: Suppresses initial output [Setting condition] • When 1 is written to WRE after reading WRE = 0

[Applicable Products and Reference Documents]

Series	Group	Reference Document Title	Rev.	Document No.
SH7080	SH7083, SH7084, SH7085, SH7086	SH7080 Group Hardware Manual	4.00	REJ09B0181-0400
SH7137	SH7136, SH7137	SH7137 Group Hardware Manual	2.00	REJ09B0402-0200
SH7146	SH7146, SH7149	SH7146 Group Hardware Manual	3.00	REJ09B0229-0300
SH7147	SH7147	SH7147 Group Hardware Manual	3.00	REJ09B0230-0300
SH7200	SH7201	SH7201 Group Hardware Manual	2.00	REJ09B0321-0200
	SH7203	SH7203 Group Hardware Manual	3.00	REJ09B0313-0300
	SH7205	SH7205 Group Hardware Manual	2.00	REJ09B0372-0200
	SH7206	SH7206 Group Hardware Manual	3.00	REJ09B0191-0300
SH7210	SH7211	SH7211 Group Hardware Manual	3.00	REJ09B0344-0300
SH7216	SH7214, SH7216	SH7214 Group, SH7216 Group User's Manual: Hardware	2.00	REJ09B0543-0200
SH7239	SH7239, SH7237	SH7239 Group, SH7237 Group User's Manual: Hardware	1.00	R01UH0086EJ0100
SH7243	SH7243	SH7280 Group Hardware Manual	1.00	REJ09B0393-0100
SH7260	SH7261	SH7261 Group Hardware Manual	2.00	REJ09B0320-0200
	SH7262, SH7264	SH7262 Group SH7264 Group Hardware Manual	2.00	REJ09B0445-0200
	SH7263	SH7263 Group Hardware Manual	3.00	REJ09B0290-0300
	SH7265	SH7265 Group Hardware Manual	2.00	REJ09B0351-0200
SH7280	SH7285, SH7286	SH7280 Group Hardware Manual	1.00	REJ09B0393-0100
SH/Tiny	SH7124, SH7125	SH7125 Group SH7124 Group Hardware Manual	5.00	REJ09B0243-0500