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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-H8*-A423A/E	Rev.	1.00
Title	Corrections of the H8/36109 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	H8/36109 Group	Lot No. ALL	Reference Document	H8/36109 Group Hardware Manual(REJ09B0240-0150)		

We wish to notify you of the following corrections of the H8/36109 Group Hardware Manual.

1. 5.2.4 Clock Control/Status Register (CKCSR)

[Before correction]

Bit	Bit Name	Initial Value	R/W	Description
7	PMRJ1	0	R/W	OSC Pin Function Select 1 and 0
6	PMRJ0	0	R/W	PMRJ1 PMRJ0 OSC2 OSC1 0 0 I/O I/O 1 0 CLKOUT I/O 0 1 Hi-Z OSC1 (external clock input) 1 1 OSC2 OSC1

[After correction]

Bit	Bit Name	Initial Value	R/W	Description
7	PMRJ1	0	R/W	OSC Pin Function Select 1 and 0
6	PMRJ0	0	R/W	PMRJ1 PMRJ0 OSC2 OSC1 0 0 I/O I/O 1 0 CLKOUT I/O 0 1 (OPEN) OSC1 (external clock input) 1 1 OSC2 OSC1

2. 6.1.3 System Control Register 3 (SYSCR3)

[Before correction]

Bit	Bit Name	Initial Value	R/W	Description
7	STS3	1	R/W	Standby Timer Select 3 This bit selects the waiting time in combination with bits STS2 to STS0 in SYSCR1. The relationship between the register setting and waiting time is shown in table 6.1.
6 to 0	—	All 1	—	Reserved These bits are always read as 0.

[After correction]

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 1	—	Reserved These bits are always read as 0.
0	STS3	1	R/W	Standby Timer Select 3 This bit selects the waiting time in combination with bits STS2 to STS0 in SYSCR1. The relationship between the register setting and waiting time is shown in table 6.1.

3. 17.8.2 Mark State and Break Sending

[Before correction]

When the TXD or TXD2 bit in PMR1 or the TXD_3 bit in SMCR is 1, the TXD pin is used as an I/O port whose direction (input or output) and level are determined by PCR and PDR. This can be used to set the TXD pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both PCR and PDR to 1 and also set the TXD bit to 1. Then, the TXD pin becomes an I/O port, and 1 is output from the TXD pin. To send a break during serial transmission, first set PCR to 1 and clear PDR to 0, and then set the TXD bit to 1. At this time, regardless of the current transmission state, the TXD pin becomes an I/O port, and 0 is output from the TXD pin.

[After correction]

When the TXD or TXD2 bit in PMR1 or the TXD_3 bit in SMCR is 0, the TXD pin is used as an I/O port whose direction (input or output) and level are determined by PCR and PDR. This can be used to set the TXD pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both PCR and PDR to 1 and also clear the TXD bit to 0. Then, the TXD pin becomes an I/O port, and 1 is output from the TXD pin. To send a break during serial transmission, first set PCR to 1 and clear PDR to 0, and then set the TXD bit to 1. At this time, regardless of the current transmission state, the TXD pin becomes an I/O port, and 0 is output from the TXD pin.