This document describes corrections to the descriptions for the SUSRDY bit and the flow chart of the P/E suspend command in the “ROM (Flash Memory for Code Storage)” section of User’s Manual: Hardware for the applicable products mentioned above.

Page and section numbers are based on the RX62N Group and RX621 Group. Refer to the table on the last page for the corresponding page and section numbers in the RX62T Group and RX62G Group.

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Clearing conditions of the SUSRDY bit in section 38.2.5, Flash Status Register 0 (FSTATR0) are corrected as follows.

**Before Correction**

[Clearing conditions]
- The FCU has accepted a P/E suspend command.
- During programming/erasure process, the FCU enters the command-locked state.

**After Correction**

[Clearing conditions]
- The FCU has accepted a P/E suspend command.
- During programming/erasure process, the FCU enters the command-locked state.
- **When programming/erasure process has been completed.**
In Figure 38.19, Procedure for Programming/Erasure Suspension, a processing flow never escapes from the loop for a checking procedure if the programming/erasure processing completed before checking the SUSRDY bit. Therefore, a timeout processing and a breaking processing when the FRDY bit is 1 are to be added.

Before correction

![Procedure for Programming/Erasure Suspension Diagram]

**Figure 38.19  Procedure for Programming/Erasure Suspension**
Figure 38.19 Procedure for Programming/Erasure Suspension
## Reference Documents

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