This document describes corrections to the descriptions for the SUSRDY bit and the flow chart of the P/E suspend command in the “ROM (Flash Memory for Code Storage)” section of User’s Manual: Hardware for the applicable products mentioned above.

Page and section numbers are based on the RX210 Group. Refer to the table on the last page for the corresponding page and section numbers in the other groups.

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Clearing conditions of the SUSRDY bit in section 40.2.6, Flash Status Register 0 (FSTATR0) are corrected as follows.

**Before Correction**

[Clearing conditions]
- The FCU has accepted a P/E suspend command.
- During programming/erasure process, the FCU enters the command-locked state.

**After Correction**

[Clearing conditions]
- The FCU has accepted a P/E suspend command.
- During programming/erasure process, the FCU enters the command-locked state.
- When programming/erasure process has been completed.

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In Figure 40.18, Procedure for Programming/Erasure Suspension, a processing flow never escapes from the loop for a checking procedure if the programming/erasure processing completed before checking the SUSRDY bit.
Therefore, a timeout processing and a breaking processing when the FRDY bit is 1 are to be added.
Figure 40.18    Procedure for Programming/Erasure Suspension

Note 1.  tSEED:  Suspend delay time
Note 2.  tFCUR:  Reset pulse width during programming/erasure (see section 42, Electrical Characteristics)
Note 3.  tE2K:  Erasure time for a 2-Kbyte erasure block (see section 42, Electrical Characteristics)
Figure 40.18 Procedure for Programming/Erasure Suspension

Note 1. $t_{SEED}$: Suspend delay time
Note 2. $t_{FCUR}$: Reset pulse width during programming/erasure (see section 42, Electrical Characteristics)
Note 3. $t_{E2K}$: Erasure time for a 2-Kbyte erasure block (see section 42, Electrical Characteristics)
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