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RENESAS TECHNICAL UPDATE

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Product category	MPU/MCU	Document No.	TN-RX*-A095A/E	Rev.	1.00
Title	Corrections to Descriptions for the Mailbox Register and Transmit FIFO Control Register of CAN module in RX600 Series		Information category	Technical information	
Applicable products	RX62N Group, RX621 Group, RX62G Group, RX62T Group, RX630 Group, RX63N Group, RX631 Group, RX63T Group	Lot No. All	Reference document	RX62N Group/RX621 Group User's Manual: Hardware Rev.1.30 (R01UH0033JJ0130) RX62T Group/RX62G Group User's Manual: Hardware Rev.2.00 (R01UH0034JJ0200) RX630 Group User's Manual: Hardware Rev.1.50 (R01UH0040JJ0150) RX63N Group/RX631 Group User's Manual: Hardware Rev.1.70 (R01UH0041JJ0170) RX63T Group User's Manual: Hardware Rev.2.10 (R01UH0238JJ0210)	

This document describes corrections to descriptions in the "CAN Module" section of User's Manual: Hardware of the applicable products mentioned above.

1. Mailbox Register j (MBj) (j = 0 to 31)

   Note 1 of the data byte 0 to 7 (DATA0 to DATA7) of the Mailbox register j (MBj) (j = 0 to 31) is changed as indicated below.

   [False] Note1. If the mailbox has received a message with n bytes less than 8 bytes, the values of DATA0 to DATA7 in the mailbox are undefined.

   [Correct] Note1. If the mailbox has received a message with n bytes less than 8 bytes, the values of DATAn to DATA7 in the mailbox are undefined.

2. Transmit FIFO Control Register (TFCR)

   (Not applicable to RX62N group, RX621 group, RX62G group and RX62T group)

   Seventh and eighth lines of the description of the TFE bit (transmit FIFO enable bit) of the transmit FIFO control register (TFCR) are changed as indicated below.

   [False] Before setting the TFE bit to 1 again, ensure that the TFEST bit has been set to 1. After setting the TFE bit to 1, write transmit data into MB23.

   [Correct] Before setting the TFE bit to 1 again, ensure that the TFEST bit has been set to 1. After setting the TFE bit to 1, write transmit data into MB24.