Date: Feb. 25, 2014

RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-RX*-A089A/E	Rev.	1.00
Title	Corrections and Additions to the RX111 Group User's Manual: Hardware regarding I/O Ports		Information Category	Technical Notification		
Applicable Product	RX111 Group	Lot No. All	Reference Document	RX111 Group User's Manual: Hardware Rev.1.00 (R01UH0365EJ0100)		

This document describes corrections and additions to descriptions for I/O ports in RX111 Group User's Manual: Hardware.

1. Corrections

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Descriptions for the port direction register (PDR) in 18.3.1 are corrected as follows:

Before correction

PDR is used to select the input or output direction for individual pins of the corresponding port m when the pins are configured as the general I/O pins.

Each bit of PORTm.PDR corresponds to each pin of port m; I/O direction can be specified in 1-bit units. For software compatibility, 1 (output) can be written to the bits corresponding to port m on the 64-pin product but which do not exist on a product with fewer than 64 pins are reserved.

The PORT3.PDR.B5 bit is reserved, because the P35 pin is input only. The bit corresponding to a pin that does not exist is also reserved. A reserved bit is read as 0. The write value should be 0.

After correction

PDR is used to select the input or output direction for individual pins of the corresponding port m when the pins are configured as the general I/O pins.

PORTm.PDR is a direction register of port m. Each bit in this register corresponds to each pin of port m and I/O direction can be specified in 1-bit units. The bits corresponding to pins that are not listed in Table 18.1 and the PORT3.PDR.B5 bit of the input-only P35 pin are reserved. A reserved bit should be set to 0 or 1 according to Table 18.3. When setting a value to a reserved bit, access in byte units.

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Descriptions for the port output data register (PODR) in 18.3.2 are corrected as follows:

Before correction

PODR holds the data to be output from the pins used for general output ports.

Bits corresponding to port m on the 64 pin-product but which do not exist on a product with fewer than 64 pins are reserved. Write 0 to these bits.

The PORT3.PODR.B5 bit is reserved, because the P35 pin is input only. The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as 0. The write value should be 0.

After correction

PODR holds the data to be output from the pins used for general output ports.

The bits corresponding to pins that are not listed in Table 18.1 and the PORT3.PODR.B5 bit of the input-only P35 pin are reserved. A reserved bit is read as 0. The write value should be 0. When setting a value to a reserved bit, access in byte units.

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"R/W" in the R/W column of b0 to b7 in the table for the port input data register (PIDR) in 18.3.3 is corrected to "R".

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Descriptions for the port input data register (PIDR) in 18.3.3 are corrected as follows:

Before correction

PIDR indicates individual pin states of port m.
The pin states of port m can be read with the PORTm.PIDR, regardless of the values of PORTm.PDR and PORTm.PMR.
The NMI pin state is reflected in the P35 bit.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as undefined and cannot be modified.

After correction

PIDR indicates individual pin states of port m.
The pin states of port m can be read with the PORTm.PIDR, regardless of the values of PORTm.PDR and PORTm.PMR.
The NMI pin state is reflected in the P35 bit.
The bits corresponding to pins that are not listed in Table 18.1 are reserved. The read value of a reserved bit is undefined. Writing has no effect.

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Descriptions for the port mode register (PMR) in 18.3.4 are corrected as follows:

Before correction

Each bit of PORTm.PMR corresponds to each pin of port m; pin function can be specified in 1-bit units. Bits corresponding to port m on the 64 pin-product but which do not exist on a product with fewer than 64 pins are reserved. Write 0 to these bits.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as 0. The write value should be 0.

After correction

Each bit of PORTm.PMR corresponds to each pin of port m; pin function can be specified in 1-bit units.
The bits corresponding to pins that are not listed in Table 18.1 and the PORT3.PMR.B5 bit of the input-only P35 pin are reserved. A reserved bit is read as 0. The write value should be 0. When setting a value to a reserved bit, access in byte units.

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Descriptions for the open drain control register 0 (ODR0) in 18.3.5 are corrected as follows:

Before correction

Bits corresponding to port m on the 64 pin-product but which do not exist on a product with fewer than 64 pins are reserved. Write 0 to these bits.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as 0. The write value should be 0.

After correction

The bits corresponding to pins that are not listed in Table 18.1 are reserved. A reserved bit is read as 0. The write value should be 0. When setting a value to a reserved bit, access in byte units.

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Descriptions for the open drain control register 1 (ODR1) in 18.3.6 are corrected as follows:

Before correction

Bits corresponding to port m on the 64 pin-product but which do not exist on a product with fewer than 64 pins are reserved. Write 0 to these bits.
The PORT3.ODR1.B2 bit is reserved, because the P35 pin is input only. The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as 0. The write value should be 0.

After correction

The bits corresponding to pins that are not listed in Table 18.1 and the PORT3.ODR1.B2 bit of the input-only P35 pin are reserved. A reserved bit is read as 0. The write value should be 0. When setting a value to a reserved bit, access in byte units.

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Descriptions for the pull-up control register (PCR) in 18.3.7 are corrected as follows:

Before correction

While a pin is in the input state with the corresponding bit in PORTm.PCR set to 1, the pull-up resistor connected to the pin is enabled.
When a pin is set as a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the settings of PCR.
The pull-up resistor is also disabled in the reset state.
The PORT3.PCR.B5 bit is reserved. The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as 0. The write value should be 0.

After correction

While a pin is in the input state with the corresponding bit in PORTm.PCR set to 1, the pull-up resistor connected to the pin is enabled.
When a pin is set as a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the settings of PCR.
The pull-up resistor is also disabled in the reset state.
The bits corresponding to pins that are not listed in Table 18.1 and the PORT3.PCR.B5 bit are reserved. A reserved bit is read as 0. The write value should be 0. When setting a value to a reserved bit, access in byte units.

2. Additions

18.4 is added as follows:

18.4 Initialization of the Port Direction Register (PDR)

Initialize reserved bits in the PDR register according to Table 18.3 to Table 18.6.

- The blank columns in Table 18.3 to Table 18.6 indicate the bits corresponding to the pins listed in Table 18.1, I/O Port Specifications.
  The corresponding bits should be set to 1 (output) or 0 (input) depending on the user system.
  However, the PORT3.PDR.B5 bit of the input-only P35 pin is reserved.
  This bit should be set to 0 (input).
- The columns other than the blank columns in Table 18.3 to Table 18.6 indicate reserved bits.
  A reserved bit should be set to 0 (input) or 1 (output) according to Table 18.3 to Table 18.6.
  When setting a value to a reserved bit, access in byte units.

Table 18.3 PDR Register Settings in 64-Pin Packages

	PDR Register							
Port Symbol	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
PORT0	1	1		1		1	1	1
PORT1					1	1	1	1
PORT2			1	1	1	1	1	1
PORT3	1	1	0	1	1			
PORT4	1		1					
PORT5	1	1			1	1	1	1
PORTA	1		1			1		
PORTB				1		1		
PORTC								
PORTE								
PORTJ			1	1	1	1	1	1

Table 18.4 PDR Register Settings in 48-Pin Packages

Port Symbol	PDR Register							
	b7	b6	b5	b4	b3	b2	b1	b0
PORT0	1	1	1	1	1	1	1	1
PORT1					1	1	1	1
PORT2			1	1	1	1	1	1
PORT3	1	1	0	1	1	1	1	1
PORT4	1		1	1	1			
PORT5	1	1	1	1	1	1	1	1
PORTA	1		1			1		1
PORTB	1	1		1		1		
PORTC								
PORTE		1	1					
PORTJ			1	1	1	1	1	1

Table 18.5 PDR Register Settings in 40-Pin Packages

Port Symbol	PDR Register							
	b7	b6	b5	b4	b3	b2	b1	b0
PORT0	1	1	1	1	1	1	1	1
PORT1					1	1	1	1
PORT2			1	1	1	1	1	1
PORT3	1	1	0	1	1		1	1
PORT4	1		1	1	1			1
PORT5	1	1	1	1	1	1	1	1
PORTA	1		1			1		1
PORTB	1	1	1	1		1	1	
PORTC	1	1	1		1	1	1	1
PORTE	1	1	1					
PORTJ			1	1	1	1	1	1

Table 18.6 PDR Register Settings in 36-Pin Packages

Port Symbol	PDR Register							
	b7	b6	b5	b4	b3	b2	b1	b0
PORT0	1	1	1	1	1	1	1	1
PORT1					1	1	1	1
PORT2		1	1	1	1	1	1	1
PORT3	1	1	0	1	1	1	1	1
PORT4	1	1	1	1	1			1
PORT5	1	1	1	1	1	1	1	1
PORTA	1		1			1	1	1
PORTB	1	1	1	1		1	1	
PORTC	1	1	1		1	1	1	1
PORTE	1	1	1					
PORTJ			1	1	1	1	1	1