To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	MCU&MPU			No	TN-SH7-406A/E	Rev	1
THEME	Correction of SH7615 Hardware manual		Classification of Information	1. Spec change 2. Supplement of Documents 3. Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	HD6417615ARF	Lot No. ALL	Reference Documents	SH7615 Hardware Manual (ADE-602-198)Rev.1.0		Effective Date Permanent	

There are errors in writing SH7615 Hardware Manual as follows.

1. Section 7 Bus State Controller (BSC)
7.5.11 64Mbit Synchronous DRAM (2Mword×32Bit)Connection : page321
<Error>
Synchronous DRAM Mode Settings:To make mode settings for the synchronous DRAM, write to address X+H'FFBF0000 or X+H'FFBF8000 from the CPU..(X represents the setting value.)
Whether to use X+H'FFBF0000 or X+H'FFBF8000 determines on the synchronous DRAM used.

<Correct>
Synchronous DRAM Mode Settings:To make mode settings for the synchronous DRAM, write to address X+H'FFFF0000 or X+H'FFFF8000 from the CPU.(X represents the setting value.)
Whether to use X+H'FFFF0000 or X+H'FFFF8000 determines on the synchronous DRAM used.

2. Section 9 Ethernet Controller (EtherC)
9.2.8 PHY Interface Status Register (PSR) : page387
<Error>
Bit 0- Link Monitor(LMON):The link status can be read by connecting the LINK signal output from the PHY-LSI. For information on the polarity, refer to the specifications for the PHY-LSI to be connected.

<Correct>
Bit 0- Link Monitor(LMON):The link status can be read by connecting the LINK signal output from the PHY-LSI. For information on the polarity, refer to the specifications for the PHY-LSI to be connected.

Note: The LMON bit is set to 0 when the LNKSTA pin is at high level, and it is set to 1 when the LNKSTA pin is at low level.

3. Section 14 Serial Communication Interface with FIFO (SCIF)
14.3.4 Operation in Synchronous Mode : page606
<Error>
In synchronous mode, the SCIF receives data in synchronization with the fall of the serial clock.

<Correct>
In synchronous mode, the SCIF receives data in synchronization with the rise of the serial clock.