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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0078A/E	Rev.	1.00
Title	Correction for “Serial Peripheral Interface (SPI)” in RA2L1/RA2E1/RA2E2 User’s Manual		Information Category	Technical Notification		
Applicable Product	RA Family RA2L1/RA2E1/RA2E2 Group	Lot No. All lots	Reference Document	-Renesas RA2L1 Group User’s Manual: Hardware R01UH0853EJ0130 Rev.1.30 -Renesas RA2E1 Group User’s Manual: Hardware R01UH0852EJ0130 Rev.1.30 -Renesas RA2E2 Group User’s Manual: Hardware R01UH0919EJ0120 Rev.1.20		

The errata in the Chapter of “Serial Peripheral Interface (SPI)” are corrected.

The details are shown from the next page.

Group: RA2L1

Chapter 28. Serial Peripheral Interface (SPI)

Before）

Table 28.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	Two channels
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKB clock divided by 4 can be input as RSPCK (PCLKB divided by 4 is the maximum RSPCK frequency) Width at high level: 2 PCLKB cycles; width at low level: 2 PCLKB cycles

Table 28.4 Relationship between SPCR settings and SPI modes (1 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKn pins	Input	Output	Output/Hi-Z	Input	Output
MOSIn pin	Input	Output	Output/Hi-Z	Input	Output
MISOn pin	Output/Hi-Z	Input	Input	Output	Input
SSLn0 pins	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 pins	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Max transfer rate	PCLKB/4	PCLKB/2	PCLKB/2	PCLKB/4	PCLKB/2

After）

The “Bit rate” in slave mode is corrected as below in Table 28.1.

Table 28.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	Two channels
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKB clock divided by 6 can be input as RSPCK (PCLKB divided by 6 is the maximum RSPCK frequency) Width at high level: 3 PCLKB cycles; width at low level: 3 PCLKB cycles

The “Max transfer rate” in slave mode is corrected as below in Table 28.4.

Table 28.4 Relationship between SPCR settings and SPI modes (1 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKn pins	Input	Output	Output/Hi-Z	Input	Output
MOSIn pin	Input	Output	Output/Hi-Z	Input	Output
MISOn pin	Output/Hi-Z	Input	Input	Output	Input
SSLn0 pins	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 pins	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Max transfer rate	PCLKB/6	PCLKB/2	PCLKB/2	PCLKB/6	PCLKB/2

Group: RA2E1

Chapter 27. Serial Peripheral Interface (SPI)

Before)

Table 27.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	One channel
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKB clock divided by 4 can be input as RSPCK (PCLKB divided by 4 is the maximum RSPCK frequency) Width at high level: 2 PCLKB cycles; width at low level: 2 PCLKB cycles

Table 27.4 Relationship between SPCR settings and SPI modes (1 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKn pins	Input	Output	Output/Hi-Z	Input	Output
MOSIn pin	Input	Output	Output/Hi-Z	Input	Output
MISOn pin	Output/Hi-Z	Input	Input	Output	Input
SSLn0 pins	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 pins	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Max transfer rate	PCLKB/4	PCLKB/2	PCLKB/2	PCLKB/4	PCLKB/2

After)

The “Bit rate” in slave mode is corrected as below in Table 27.1.

Table 27.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	One channel
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKB clock divided by 6 can be input as RSPCK (PCLKB divided by 6 is the maximum RSPCK frequency) Width at high level: 3 PCLKB cycles; width at low level: 3 PCLKB cycles

The “Max transfer rate” in slave mode is corrected as below in Table 27.4.

Table 27.4 Relationship between SPCR settings and SPI modes (1 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKn pins	Input	Output	Output/Hi-Z	Input	Output
MOSIn pin	Input	Output	Output/Hi-Z	Input	Output
MISOn pin	Output/Hi-Z	Input	Input	Output	Input
SSLn0 pins	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 pins	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Max transfer rate	PCLKB/6	PCLKB/2	PCLKB/2	PCLKB/6	PCLKB/2

Group: RA2E2

Chapter 26. Serial Peripheral Interface (SPI)

Before)

Table 26.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	One channel
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKB clock divided by 4 can be input as RSPCK (PCLKB divided by 4 is the maximum RSPCK frequency) Width at high level: 2 PCLKB cycles; width at low level: 2 PCLKB cycles

Table 26.4 Relationship between SPCR settings and SPI modes

Mode	Slave (SPI operation)	Single-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	0	1
MODFEN bit setting	0 or 1	0	0	0
SPMS bit setting	0	0	1	1
RSPCKn pins	Input	Output	Input	Output
MOSIn pin	Input	Output	Input	Output
MISOn pin	Output/Hi-Z	Input	Output	Input
SSLn0 pins	Input	Output	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	—	—
Max transfer rate	PCLKB/4	PCLKB/2	PCLKB/4	PCLKB/2

After)

The “Bit rate” in slave mode is corrected as below in Table 26.1.

Table 26.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	One channel
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 32-bit transmit and receive buffers
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKB (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKB clock divided by 6 can be input as RSPCK (PCLKB divided by 6 is the maximum RSPCK frequency) Width at high level: 3 PCLKB cycles; width at low level: 3 PCLKB cycles

The “Max transfer rate” in slave mode is corrected as below in Table 26.4.

Table 26.4 Relationship between SPCR settings and SPI modes

Mode	Slave (SPI operation)	Single-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	0	1
MODFEN bit setting	0 or 1	0	0	0
SPMS bit setting	0	0	1	1
RSPCKn pins	Input	Output	Input	Output
MOSIn pin	Input	Output	Input	Output
MISOn pin	Output/Hi-Z	Input	Output	Input
SSLn0 pins	Input	Output	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	—	—
Max transfer rate	PCLKB/6	PCLKB/2	PCLKB/6	PCLKB/2