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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0093A/E	Rev.	1.00
Title	Correction for the pin's name of power supply & power supply ground about 12-Bit A/D Converter		Information Category	Technical Notification		
Applicable Product	RA Family RA2E2 Group	Lot No. All Lots	Reference Document	Renesas RA2E2 Group User's Manual: Hardware R01UH0919EJ0120 Rev.1.20		

RA2E2 doesn't have AVCC0 pin and AVSS0 pin for Analog power supply.

"AVCC0" should be corrected as "VCC" and "AVSS0" should be corrected as "VSS" of highlighted part in the following Tables, Figures and descriptions.

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Table 1.14 Pin functions (2 of 2)

Function	Signal	I/O	Description
SCI	SCKn (n = 9)	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn (n = 9)	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn (n = 9)	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn (n = 9)	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	SCLn (n = 9)	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn (n = 9)	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn (n = 9)	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn (n = 9)	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn (n = 9)	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn (n = 9)	Input	Chip-select input pins (simple SPI mode), active-low
I3C	SCLn (n = 0)	I/O	Input/output pins for the clock
	SDAn (n = 0)	I/O	Input/output pins for data
SPI	RSPCKA	I/O	Clock input/output pin
	SSLA0	I/O	Input or output pin for slave selection
	MOSIA	I/O	Input or output pins for data output from the master
	MISOA	I/O	Input or output pins for data output from the slave
Analog power supply	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12.

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28. 12-Bit A/D Converter (ADC12)

28.1 Overview

The reference power supply pin (VREFH0), the analog block power supply pin (AVCC0), or the internal reference voltage can selected as the high-potential reference voltage. The reference power supply ground pin (VREFL0) or the analog block power supply ground pin (AVSS0) can be selected as the low-potential reference voltage. If the internal reference voltage is selected as the high-potential reference voltage, A/D conversion of the temperature sensor or internal reference voltage is prohibited.

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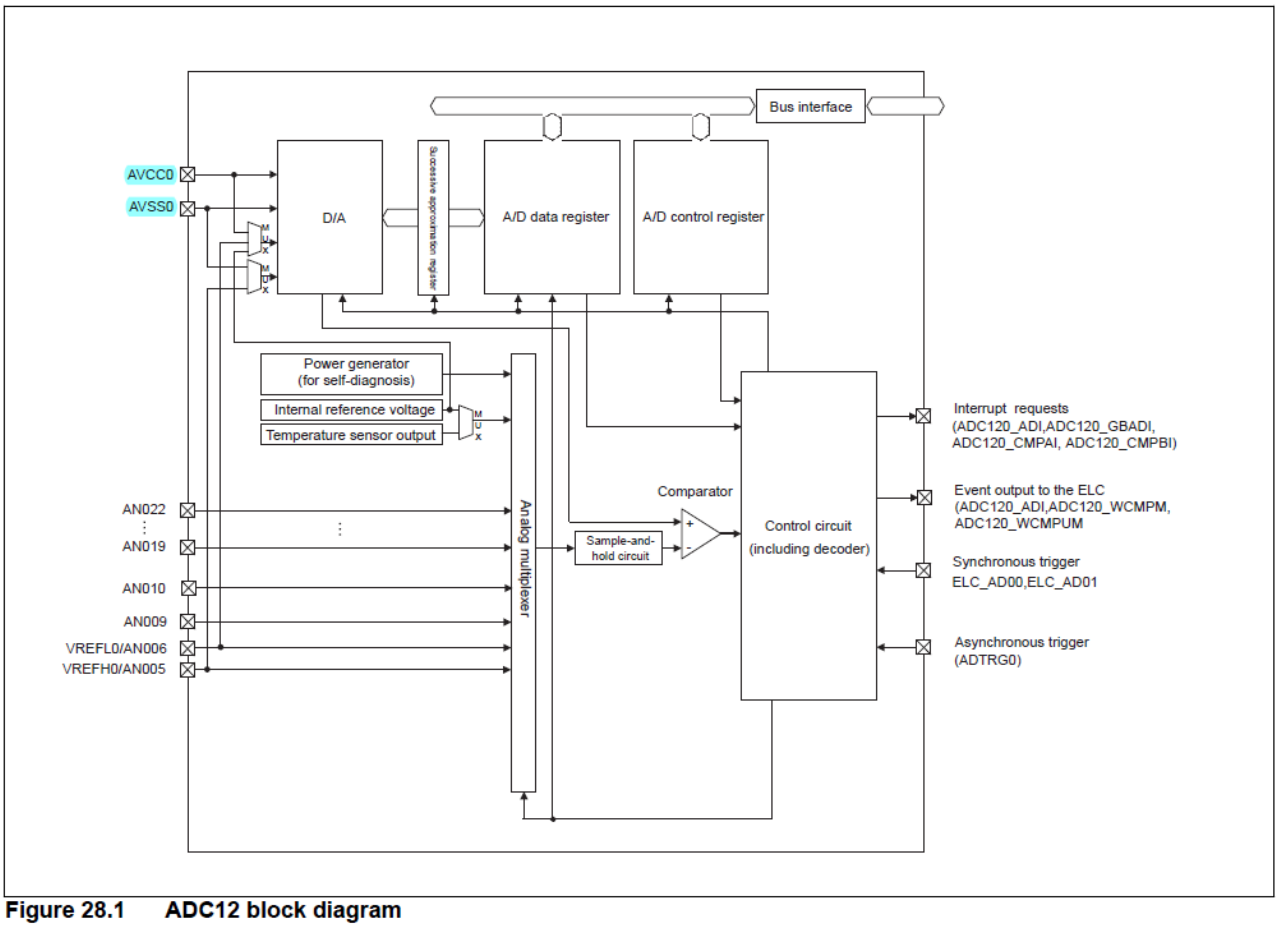

Figure 28.1 ADC12 block diagram

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Table 28.3 ADC12 I/O pins

Pin name	I/O	Function
AVCC0	Input	Analog block power supply pin
AVSS0	Input	Analog block power supply ground pin
VREFH0	Input	Analog reference voltage supply pin
VREFL0	Input	Analog reference ground pin
AN005, AN006, AN009, AN010, AN019 to AN022	Input	Analog input pins 5, 6, 9, 10, 19 to 22
ADTRG0	Input	External trigger input pin for starting A/D conversion

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28.2.37 ADHVREFCNT : A/D High-Potential/Low-Potential Reference Voltage Control Register

Base address: ADC120 = 0x4005_C000

Offset address: 0x08A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ADSLP	—	—	LVSEL	—	—	HVSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	HVSEL[1:0]	High-Potential Reference Voltage Select 0 0: AVCC0 is selected as the high-potential reference voltage 0 1: VREFH0 is selected as the high-potential reference voltage 1 0: Internal reference voltage is selected as the high-potential reference voltage 1 1: No reference voltage pin is selected (internal node discharge)	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	LVSEL	Low-Potential Reference Voltage Select 0: AVSS0 is selected as the low-potential reference voltage. 1: VREFL0 is selected as the low-potential reference voltage.	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	ADSLP	Sleep 0: Normal operation 1: Standby state	R/W

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LVSEL bit (Low-Potential Reference Voltage Select)

The LVSEL bit specifies the low-potential reference voltage as AVSS0 or VREFL0.

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28.7 A/D Conversion Procedure When Selecting Internal Reference Voltage as High-Potential Reference Voltage

The following sequence describes the A/D conversion procedure after selecting the internal reference voltage as the high-potential reference voltage. In this case, A/D conversion is possible for channels of analog input, however A/D conversion of the internal reference voltage and the temperature sensor output is prohibited.

1. Set ADHVREFCNT.HVSEL[1:0] to 11b to discharge the high-potential reference voltage path in the ADC12.
2. Wait for a 1 µs discharge period in the software.
3. Set ADHVREFCNT.HVSEL[1:0] to 10b to select internal reference voltage as the high-potential reference voltage.*1
4. Wait until the internal reference voltage is stabilized (for 5 µs) in the software, then perform A/D conversion.

Note 1. The ADC12 has a protection function that disables selection of internal reference voltage (ADHVREFCNT.HVSEL[1:0] = 10b) without discharge (ADHVREFCNT.HVSEL[1:0] = 11b) from the selection of VREFH0 (ADHVREFCNT.HVSEL[1:0] = 01b) or AVCC0 (ADHVREFCNT.HVSEL[1:0] = 00b). If the internal reference voltage is selected without discharge, discharge is forcibly set. Select the internal reference voltage again 1 µs later.

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28.8.11 Notes on Board Design

The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible. In addition, digital circuit signal lines and analog circuit signal lines should not intersect or be placed near each other. If these rules are not followed, noise can occur on analog signals and A/D conversion accuracy is affected. The analog input pins, reference power supply pin (VREFH0), reference ground pin (VREFL0) should be separated from digital circuits using the ground (AVSS0).

28.8.12 Constraints on Noise Prevention

To prevent the analog input pins from being destroyed by abnormal voltage such as excessive surge, insert a capacitor between AVCC0 and AVSS0 and between VREFH0 and VREFL0. Additionally, connect a protection circuit to protect the analog input pins as shown in Figure 28.33.

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36. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = 1.6 to 5.5 V, VREFH0 = 1.6 V to AVCC0

VSS = VREFL0 = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3 V.

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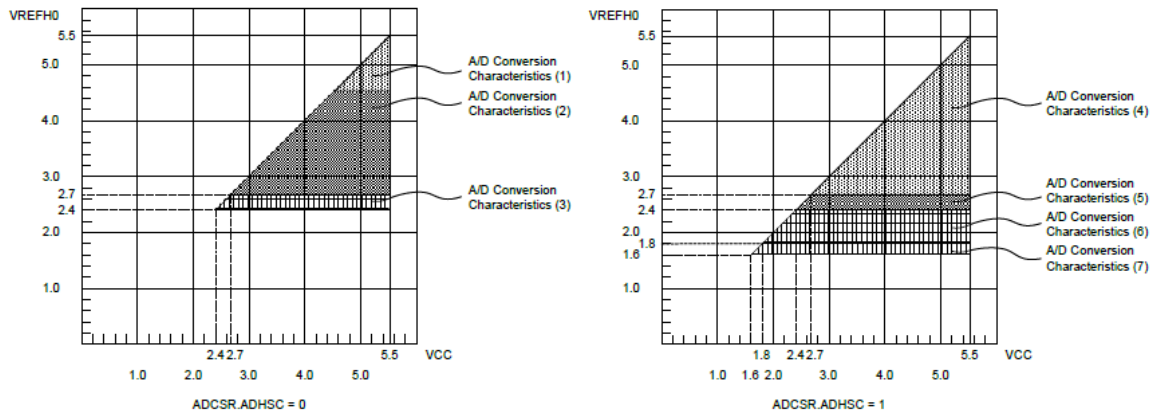

Figure 36.44 AVCC0 to VREFH0 voltage range

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Table 36.39 A/D conversion characteristics (1) in high-speed A/D conversion mode

Table 36.40 A/D conversion characteristics (2) in high-speed A/D conversion mode

Table 36.41 A/D conversion characteristics (3) in high-speed A/D conversion mode

Table 36.42 A/D conversion characteristics (4) in low-power A/D conversion mode

Table 36.43 A/D conversion characteristics (5) in low-power A/D conversion mode

Table 36.44 A/D conversion characteristics (6) in low-power A/D conversion mode

Table 36.45 A/D conversion characteristics (7) in low-power A/D conversion mode

Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

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Table 36.46 12-bit A/D converter channel classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN005, AN006, AN009, AN010	AVCC0 = 1.6 to 5.5 V	Pins AN005, AN006, AN009, AN010 cannot be used as general I/O, TS transmission, when the A/D converter is in use.
Normal-precision channel	AN019 to AN022		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 1.8 to 5.5 V	—
Temperature sensor input channel	Temperature sensor output	AVCC0 = 1.8 to 5.5 V	—

Table 36.47 A/D internal reference voltage characteristics

Conditions: VCC = VREFH0 = 1.8 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.42	1.48	1.54	V	—
PCLKD (ADCLK) frequency*3	1	—	2	MHz	—
Sampling time*4	5.0	—	—	µs	—

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 1.8 V.
Note 2. The 12-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 12-bit A/D converter.
Note 3. When the internal reference voltage is selected as the high-potential reference voltage.
Note 4. When the internal reference voltage is converted.