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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-V85-A001A/E	Rev	1.00
Title	Correction for Incorrect Description Notice V850ES/JG3-L Descriptions in the Hardware User's Manual Rev.7.00 Changed		Information Category	Technical Notification		
Applicable Product	V850ES/JG3-L μPD70F3841, μPD70F3842	Lot No. All Lot	Reference Document	V850ES/JG3-L User's Manual: Hardware R01UH0165EJ0700 (Rev.7.00)		

This document describes misstatements found in the V850ES/JG3-L hardware user's manual Rev.7.00 (R01UH0001EJ0700).

Cancelation line parts (ex. ~~capable of separate output~~) are deleted and gray parts (ex. 6 bits) are changed.

The above corrections will be made for the next revision of the hardware user's manual.

No. 1

Location: Table 1-1 on page 21

Incorrect:

Product Name		μPD70F3841	μPD70F3842	μPD70F3792	μPD70F3793	μPD70F3737	μPD70F3738
Internal memory	Flash memory	768 KB	1 MB	384 KB	512 KB	128 KB	256 KB
	RAM	80 KB Note1	80 KB Note1	32 KB	40 KB	8 KB	16 KB
Memory Space	Logical space	64 MB					
	External memory area	15 MB					
External bus interface		Address buses: 22bit Address data buses: 8/16 bits Multiplexed bus mode (capable of separate output)		Address buses: 22 bits Address data buses: 8/16 bits Separate bus/multiplexed bus mode selectable			

Correct:

Product Name		μPD70F3841	μPD70F3842	μPD70F3792	μPD70F3793	μPD70F3737	μPD70F3738
Internal memory	Flash memory	768 KB	1 MB	384 KB	512 KB	128 KB	256 KB
	RAM	80 KB Note1	80 KB Note1	32 KB	40 KB	8 KB	16 KB
Memory Space	Logical space	64 MB					
	External memory area	15 MB					
External bus interface		Address buses: 6 bits Address data buses: 8/16 bits Multiplexed bus mode ~~(capable of separate output)~~		Address buses: 22 bits Address data buses: 8/16 bits Separate bus/multiplexed bus mode selectable			

No. 2

Location: 1.2 on page 22

Incorrect:

O Memory space: 64 MB of linear address space (for programs and data)
External expansion: Up to 16 MB (including 1 MB used as internal ROM/RAM)

• Internal memory: RAM: 8/16/32/40 /80 KB (see **Table 1-1**)
Flash memory: 128 K/256 K/384 K/512 K/768 K/1 MB (see **Table 1-1**)

• External bus interface: • Separate bus/multiplexed bus output selectable
(μPD70F3737, 70F3738,70F3792, 70F3793)
• Multiplexed bus mode (capable of separate output)
(μPD70F3841, 70F3842)

Correct:

O Memory space: 64 MB of linear address space (for programs and data)
External expansion: Up to 16 MB (including 1 MB used as internal ROM/RAM)

• Internal memory: RAM: 8/16/32/40 /80 KB (see **Table 1-1**)
Flash memory: 128 K/256 K/384 K/512 K/768 K/1 MB (see **Table 1-1**)

• External bus interface: • Separate bus/multiplexed bus output selectable
(μPD70F3737, 70F3738, 70F3792, 70F3793)
• Multiplexed bus mode ~~(capable of separate output)~~
(μPD70F3841, 70F3842)

No. 3

Location: 5.1 on page 185

Incorrect:

O Output can be selected from a multiplexed bus with a minimum of 3 bus cycles and a separate bus with a minimum of 2 bus cycles (μPD70F3737, 70F3738, 70F3792, 70F3793) .

O A multiplexed bus with a minimum of 3 bus cycles and a separate bus output are available (μPD70F3841, 70F3842).

Correct:

O Output can be selected from a multiplexed bus with a minimum of 3 bus cycles and a separate bus with a minimum of 2 bus cycles (μPD70F3737, 70F3738, 70F3792, 70F3793) .

O A multiplexed bus with a minimum of 3 bus cycles ~~and a separate bus output~~ is available (μPD70F3841, 70F3842).

No. 4

Location: 5.2 on page 187

Incorrect:

The following signals can be used to control an external device in each bus mode.

When use a separate bus in μPD70F3841 and μPD70F3842, refer to **Table 5-1**.

Correct:

The following signals can be used to control an external device in each bus mode.

~~When use a separate bus in μPD70F3841 and μPD70F3842, refer to **Table 5-1.**~~

No. 5

Location: Table 5-1 on page 186

Incorrect:

Bus Control Signal	I/O	Function	Alternate Function	Register to Switch Between Port Mode/Alternate-Function Mode
AD0 to AD15	I/O	Address/data bus	PDL0 to PDL15	PMCDL register
A0 to A15 Note1	Output	Address bus (capable of separate output)	P90 to P915	PMC9 register

Note 1. μPD70F3841, 70F3842 only

Correct:

Bus Control Signal	I/O	Function	Alternate Function	Register to Switch Between Port Mode/Alternate-Function Mode
AD0 to AD15	I/O	Address/data bus	PDL0 to PDL15	PMCDL register
~~A0 to A15 Note1~~	~~Output~~	~~Address bus (capable of separate output)~~	~~P90 to P915~~	~~PMC9 register~~

~~Note 1. μPD70F3841, 70F3842 only~~

No. 6

Location: 5.2.1 on page 187

Incorrect:

When the internal ROM, internal RAM, on-chip peripheral I/O or expanded internal RAM is accessed, the status of each pin is as follows.

When use a separate bus in μPD70F3841 and μPD70F3842, refer to the case of multiplexed bus mode.

Correct:

When the internal ROM, internal RAM, on-chip peripheral I/O or expanded internal RAM is accessed, the status of each pin is as follows.

~~When use a separate bus in μPD70F3841 and μPD70F3842, refer to the case of multiplexed bus mode.~~

No. 7

Location: 5.4 on page 190

Incorrect:

The μPD70F3737, 70F3738, 70F3792, and 70F3793 include the following two external bus interface modes.

- Multiplexed bus mode
- Separate bus mode

These two modes can be selected by using the EXIMC register in μPD70F3737, 70F3738, 70F3792, and 70F3793.

In μPD70F3841 and μPD70F3842, the mode is fixed to multiplexed bus mode but separate bus is available with using address bus (A0 to A15). In this case, EXIMC register is not supported.

Correct:

The μPD70F3737, 70F3738, 70F3792, and 70F3793 include the following two external bus interface modes.

- Multiplexed bus mode
- Separate bus mode

These two modes can be selected by using the EXIMC register in μPD70F3737, 70F3738, 70F3792, and 70F3793.

In μPD70F3841 and μPD70F3842, the mode is fixed to multiplexed bus mode ~~but separate bus is available with using address bus (A0 to A15). In this case~~, EXIMC register is not supported.

No. 8

Location: 5.10 on page 208

Incorrect:

Typical bus timing diagrams are shown below.

When use a separate bus in μPD70F3841, 70F3842, refer to timing of multiplexed bus mode.

Correct:

Typical bus timing diagrams are shown below.

~~When use a separate bus in μPD70F3841, 70F3842, refer to timing of multiplexed bus mode.~~

No. 9

Location: Figure 5-5 on page 208

Incorrect:

Note μPD70F3841, 70F3842 have A21 to A0 (When using separate output)

Correct:

~~**Note** μPD70F3841, 70F3842 have A21 to A0 (When using separate output)~~

No. 10

Location: Figure 5-6 on page 208

Incorrect:

Note μPD70F3841, 70F3842 have A21 to A0 (When using separate output)

Correct:

~~**Note** μPD70F3841, 70F3842 have A21 to A0 (When using separate output)~~

No. 11

Location: Figure 5-7 on page 209

Incorrect:

Note μPD70F3841, 70F3842 have A21 to A0 (When using separate output)

Correct:

~~**Note** μPD70F3841, 70F3842 have A21 to A0 (When using separate output)~~

No. 12

Location: Figure 5-8 on page 209

Incorrect:

Note μPD70F3841, 70F3842 have A21 to A0 (When using separate output)

Correct:

~~**Note** μPD70F3841, 70F3842 have A21 to A0 (When using separate output)~~

No. 13

Location: Figure 5-9 on page 210

Incorrect:

Note1. This idle state (TI) does not depend on the BCC register settings.

2. μPD70F3841, 70F3842 have A21 to A0 (When using separate output)

Correct:

Note1. This idle state (TI) does not depend on the BCC register settings.

~~**2.** μPD70F3841, 70F3842 have A21 to A0 (When using separate output)~~

No. 14

Location: Figure 5-10 on page 210

Incorrect:

Note μPD70F3841, 70F3842 have A21 to A0

Correct:

~~**Note** μPD70F3841, 70F3842 have A21 to A0~~

No. 15

Location: 34.7.3 on page 1045

Incorrect:

The values for just the access method to be used (synchronous with or asynchronous to CLKOUT) must be satisfied. It is not necessary to satisfy the values for both methods. When using a separate bus, refer to the specification of multiplexed bus mode.

Correct:

The values for just the access method to be used (synchronous with or asynchronous to CLKOUT) must be satisfied. It is not necessary to satisfy the values for both methods. ~~When using a separate bus, refer to the specification of multiplexed bus mode.~~

No. 16

Location: 34.7.3 (1) (a) **Read Cycle (Asynchronous to CLKOUT): In Multiplexed Bus Mode** on page 1046

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~

No. 17

Location: 34.7.3 (1) (a) **Write Cycle (Asynchronous to CLKOUT): In Multiplexed Bus Mode** on page 1047

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~

No. 18

Location: 34.7.3 (1) (b) **Read Cycle (Synchronous with CLKOUT): In Multiplexed Bus Mode** on page 1048

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~

No. 19

Location: 34.7.3 (1) (b) **Write Cycle (Synchronous with CLKOUT): In Multiplexed Bus Mode** on page 1049

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~