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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A080A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/L1A Descriptions in the User's Manual: Hardware Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/L1A Group	Lot No. All lots	Reference Document	RL78/L1A User's Manual: Hardware Rev. 1.00 R01UH0636EJ0100 (Aug. 2016)		

This document describes misstatements found in the RL78/L1A User's Manual: Hardware Rev. 1.00 (R01UH0636EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
3.3.5 Extended special function registers (2nd SFRs: 2nd Special FunctionRegisters) Table 3 - 10 Extended SFR (2nd SFR) List (1/10)	Page 73	Incorrect descriptions revised
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4.3 Registers Controlling Port Function	Page 105	Incorrect descriptions revised
4.3.8 Global analog input disable register (GAIDIS)	Page 117	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0636EJ0100	
1	3.3.5 Extended special function registers (2nd SFRs: 2nd Special FunctionRegisters) Table 3 - 10 Extended SFR (2nd SFR) List (1/10)		Page 73	Page 3
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3	4.3 Registers Controlling Port Function		Page 105	Page 5
4	4.3.8 Global analog input disable register (GAIDIS)		Page 117	Page 6

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/L1A Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A080A/E	Jun. 15, 2017	First edition issued Corrections No.1 to No.4 revised (this document)

1. **3.3.5 Extended special function registers (2nd SFRs: 2nd Special FunctionRegisters)**
   Table 3 - 10 Extended SFR (2nd SFR) List (1/10) (p.73)

Incorrect:

Table 3 - 10 Extended SFR (2nd SFR) List (1/15)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F007CH	Global analog input disable register	GAIDIS	R/W	√	√	—	00H

Correct:

(Delete)

2. **4.2 Port Configuration**
   Table 4 - 1 Port Configuration (p.98)

Incorrect:

Table 4 - 1 Port Configuration

Item	Configuration
Control registers	Port mode registers (PM0 to PM8, PM10, PM12, PM14, PM15) Port registers (P0 to P8, P10, P12 to P15) Pull-up resistor option registers (PU0, PU1, PU3 to PU5, PU7, PU8, PU12) Port input mode registers (PIM0, PIM1, PIM3, PIM4, PIM8) Port output mode registers (POM0, POM1, POM3, POM4, POM8) Port mode control registers (PMC2, PMC4, PMC8, PMC10, PMC14, PMC15) Peripheral I/O redirection registers (PIOR) **Global analog input disable register (GAIDIS)** LCD port function register (PFSEG0 to PFSEG5) LCD input switch control register (ISCLCD)
Port	• 80-pin products Total: 59 (CMOS I/O: 52 (N-ch open drain I/O [VDD tolerance]: 12), CMOS input: 5, N-ch open-drain I/O [6 V tolerance]: 2) • 100-pin products Total: 79 (CMOS I/O: 71 (N-ch open drain I/O [VDD tolerance]: 15), CMOS input: 5, CMOS output: 1, N-ch open-drain I/O [6 V tolerance]: 2)

Correct:

Table 4 - 1 Port Configuration

Item	Configuration
Control registers	Port mode registers (PM0 to PM8, PM10, PM12, PM14, PM15) Port registers (P0 to P8, P10, P12 to P15) Pull-up resistor option registers (PU0, PU1, PU3 to PU5, PU7, PU8, PU12) Port input mode registers (PIM0, PIM1, PIM3, PIM4, PIM8) Port output mode registers (POM0, POM1, POM3, POM4, POM8) Port mode control registers (PMC2, PMC4, PMC8, PMC10, PMC14, PMC15) Peripheral I/O redirection registers (PIOR) (Delete) LCD port function register (PFSEG0 to PFSEG5) LCD input switch control register (ISCLCD)
Port	• 80-pin products Total: 59 (CMOS I/O: 52 (N-ch open drain I/O [VDD tolerance]: 12), CMOS input: 5, N-ch open-drain I/O [6 V tolerance]: 2) • 100-pin products Total: 79 (CMOS I/O: 71 (N-ch open drain I/O [VDD tolerance]: 15), CMOS input: 5, CMOS output: 1, N-ch open-drain I/O [6 V tolerance]: 2)

3. 4.3 Registers Controlling Port Function (p.105)

Incorrect:

4.3 Registers Controlling Port Function

Port functions are controlled by the following registers.

- Port mode registers (PMxx)
- Port registers (Pxx)
- Pull-up resistor option registers (PUxx)
- Port input mode registers (PIMxx)
- Port output mode registers (POMxx)
- Port mode control registers (PMCxx)
- Peripheral I/O redirection register (PIOR)
- **Global analog input disable register (GAIDIS)**
- LCD port function register (PFSEG0 to PFSEG5)
- LCD input switch control register (ISCLCD)

Caution Which registers and bits are included depends on the product. For registers and bits mounted on each product, see Tables 4 – 2 to 4 – 5. Be sure to set bits that are not mounted to their initial values.

Correct:

4.3 Registers Controlling Port Function

Port functions are controlled by the following registers.

- Port mode registers (PMxx)
- Port registers (Pxx)
- Pull-up resistor option registers (PUxx)
- Port input mode registers (PIMxx)
- Port output mode registers (POMxx)
- Port mode control registers (PMCxx)
- Peripheral I/O redirection register (PIOR)

(Delete)

- LCD port function register (PFSEG0 to PFSEG5)
- LCD input switch control register (ISCLCD)

Caution Which registers and bits are included depends on the product. For registers and bits mounted on each product, see Tables 4 - 2 to 4 - 5. Be sure to set bits that are not mounted to their initial values.

4 4.3.8 Global analog input disable register (GAIDIS) (p.117)

Incorrect:

4.3.8 Global analog input disable register (GAIDIS)

This register is used to prevent through-current flowing from the input buffers of input ports which use AV_{DD} as the power supply when the AV_{DD} power supply is turned off.

When not all of the I/O ports using AV_{DD} as the power supply are used, low power consumption can be achieved by setting the GAIDIS register (setting the GAIDIS0 bit to 1) to turn off the AV_{DD} power supply.

By setting the GAIDIS0 bit to 1, input to any input buffer using AV_{DD} as the power supply is prohibited, preventing through-current from flowing when the AV_{DD} power supply is turned off.

The GAIDIS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H

. Figure 4 - 8 Format of Global analog input disable register (GAIDIS)

Address: F007CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
GAIDIS	0	0	0	0	0	0	0	GAIDIS0

GAIDIS0	Setting of input buffers using AV_{DD} power supply
0	Input to input buffers permitted (default)
1	Input to input buffers prohibited. No through-current flows to the input buffers.

Turn off the AV_{DD} power supply with the following procedure.

1. Prohibit input to input buffers (set GAIDIS0 = 1).
2. Turn off the AV_{DD} power supply.

Turn on again the AV_{DD} power supply with the following procedure.

1. Turn on the AV_{DD} power supply.
2. Permit input to input buffers (set GAIDIS0 = 0).

Caution 1. Do not input an input voltage equal to or greater than AV_{DD} to an input port that uses AV_{DD} as the power supply.

Caution 2. When input to input buffers is prohibited (GDIDIS0 = 1), the value read from the port register (Pxx) of a port that uses EV_{DD} as the power supply is 1.

Remark Even when input to input buffers is prohibited (GAIDIS0 = 1), peripheral functions which do not use port functions having AV_{DD} as the power supply can be used.

Correct:

(Delete)