Date: Jul. 1, 2014

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A029A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/L13 Descriptions in the User's Manual: Hardware Rev. 2.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/L13 Group	Lot No. All lots	Reference Document	RL78/L13 User's Manual: Hardware Rev. 2.00 R01UH0382EJ0200 (Dec. 2013)		

This document describes misstatements found in the RL78/L13 User's Manual: Hardware Rev. 2.00 (R01UH0382EJ0200).

Corrections

Applicable Item	Applicable Page	Contents
5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)	Page 164	Incorrect descriptions revised
14.5.7 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 14-71. and Figure 14-73.)	Pages 592 and 594	Incorrect descriptions revised
14.6.3 SNOOZE mode function	Page 618	Incorrect descriptions revised
14.6.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 14-90., Figure 14-91. and Figure 14-93.)	Pages 620, 621 and 623	Incorrect descriptions revised
19.4.3 Multiple interrupt servicing Table 19-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing	Page 864	Incorrect descriptions revised
23.2 Configuration of Power-on-reset Circuit Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1)	Page 900	Incorrect descriptions revised
32.1 Absolute Maximum Ratings	Page 1001	Specifications changed
32.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	Page 1056	Content change
33.1 Absolute Maximum Ratings	Page 1065	Specifications changed
33.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	Page 1114	Content change

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0382EJ0200	
1	5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)		Page 164	Page 3
2	14.5.7 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 14-71. and Figure 14-73.)		Pages 592 and 594	Page 4 and 5
3	14.6.3 SNOOZE mode function		Page 618	Page 6
4	14.6.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 14-90., Figure 14-91. and Figure 14-93.)		Pages 620, 621 and 623	Page 7 to 9
5	19.4.3 Multiple interrupt servicing Table 19-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing		Page 864	Page 10
6	23.2 Configuration of Power-on-reset Circuit Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1)		Page 900	Page 11
7	32.1 Absolute Maximum Ratings		Page 1001	Page 12
8	32.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics		Page 1056	Page 13
9	33.1 Absolute Maximum Ratings		Page 1065	Page 14
10	33.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics		Page 1114	Page 15

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/L13 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A029A/E	Jul. 01, 2014	First edition issued Corrections No.1 to No.10 revised (this document)

1. 5.3.9 High-speed on-chip oscillator trimming register (HIOTRM) (Page 243)

Incorrect:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined [Note] R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
•	•	•	•	•	•	
•	•	•	•	•	•	
•	•	•	•	•	•	
1	1	1	1	1	0	
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remarks 1. The HIOTRM register can be used to adjust the high-speed on-chip oscillator clock to an accuracy within about 0.05%.

2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

Correct:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined [Note] R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
•	•	•	•	•	•	
•	•	•	•	•	•	
•	•	•	•	•	•	
1	1	1	1	1	0	
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remarks 1. The HIOTRM register holds a six-bit value used to adjust the high-speed on-chip oscillator with an increment of 1 corresponding to an increase of frequency by about 0.05%.

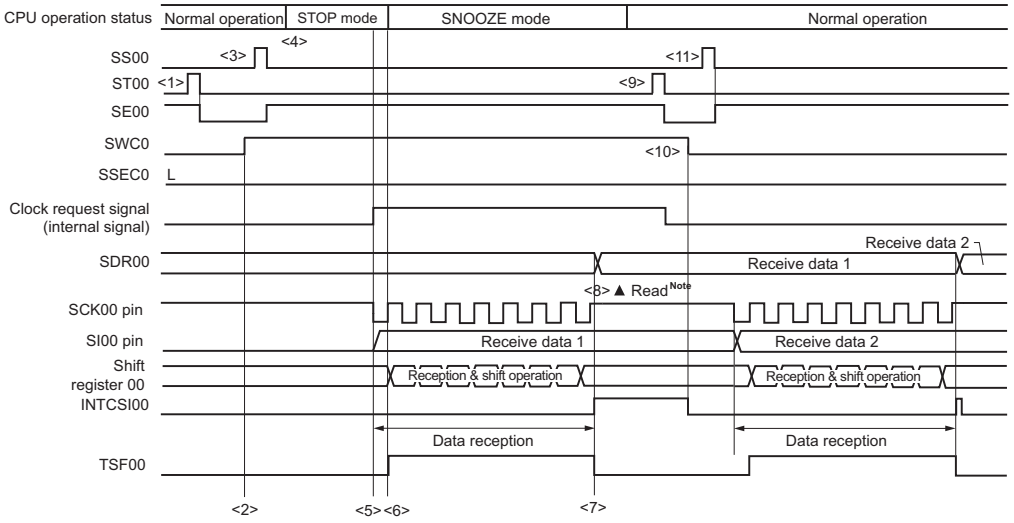
2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

2. 14.5.7 SNOOZE mode function

Timing Chart of SNOOZE Mode Operation (Figure 14-71. and Figure 14-73.) (Pages 592 and 594)

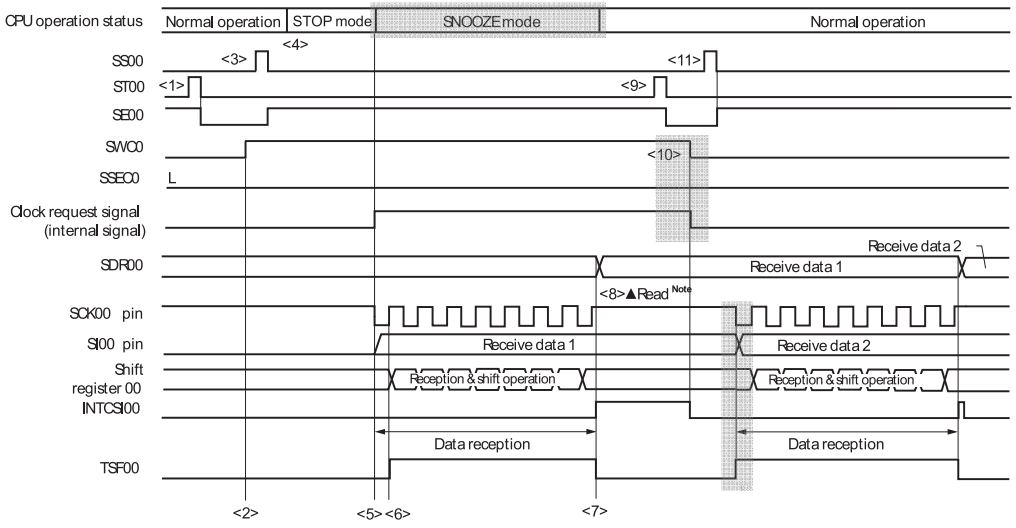
It is correction of "CPU operation status", "Clock request signal (internal signal)" and "TSF00" in this Figure.

Incorrect:
Figure 14-71. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

Correct:
Figure 14-71. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)

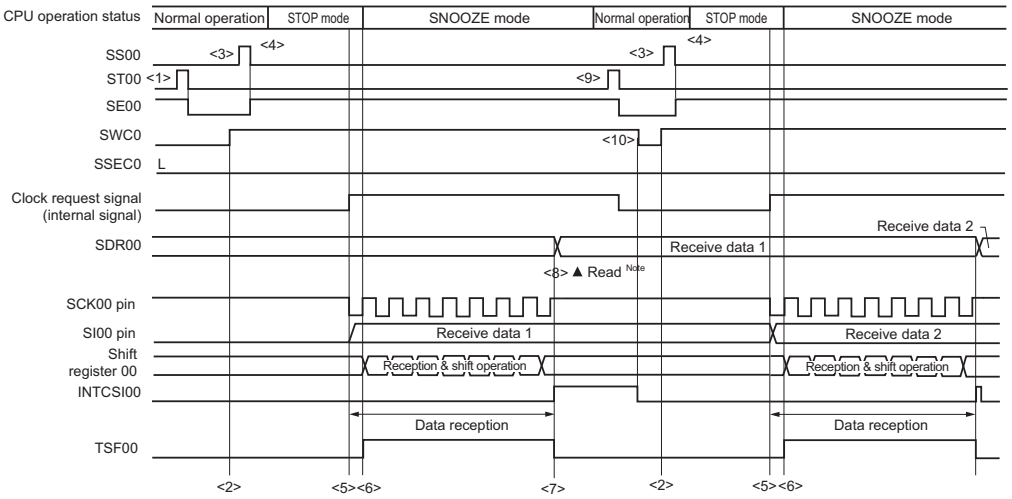


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)” and “INTCSI00” in this Figure.

Incorrect:

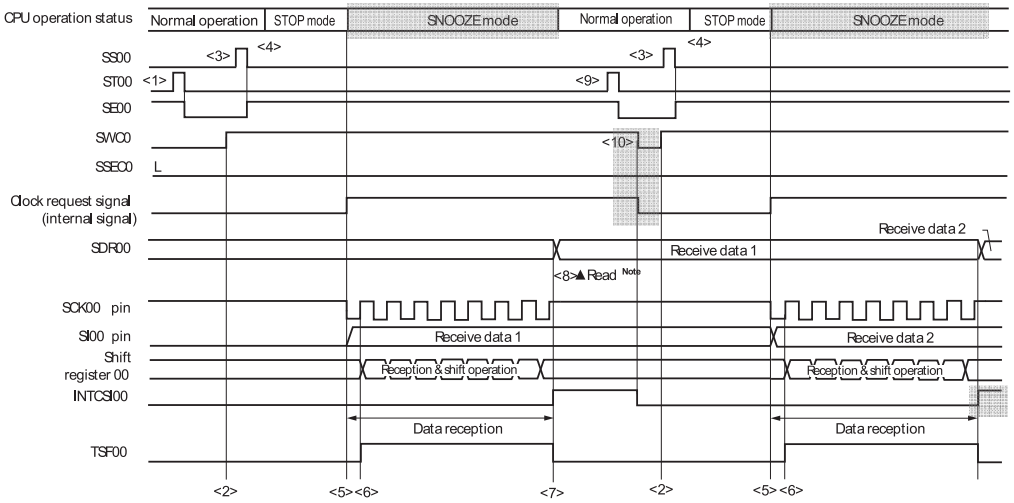
Figure 14-73. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

Correct:

Figure 14-73. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

3. 14.6.3 SNOOZE mode function (Page 618)

Incorrect:

14.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

Correct:

14.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

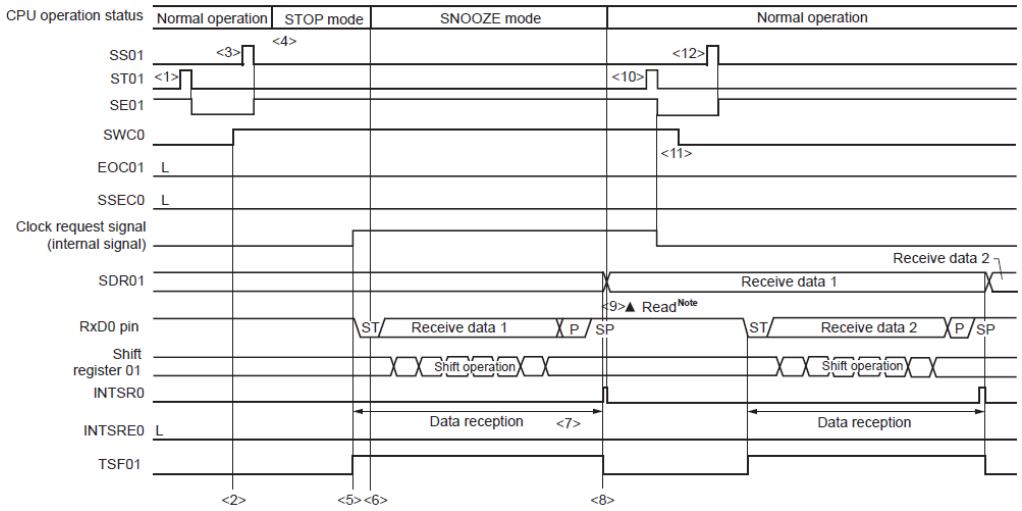
5. The CPU shifts from the STOP mode to the SNOOZE mode on detecting the valid edge of the RxDq signal. Note, however, that transfer through the UART channel may not start and the CPU may remain in the SNOOZE mode if an input pulse on the RxDq pin is too short to be detected as a start bit. In such cases, data may not be received correctly, and this may lead to a framing error or parity error in the next UART transfer.

4. 14.6.3 SNOOZE mode function
Timing Chart of SNOOZE Mode Operation (Figure 14-90., Figure 14-91. and Figure 14-93.) (Pages 620, 621 and 623)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

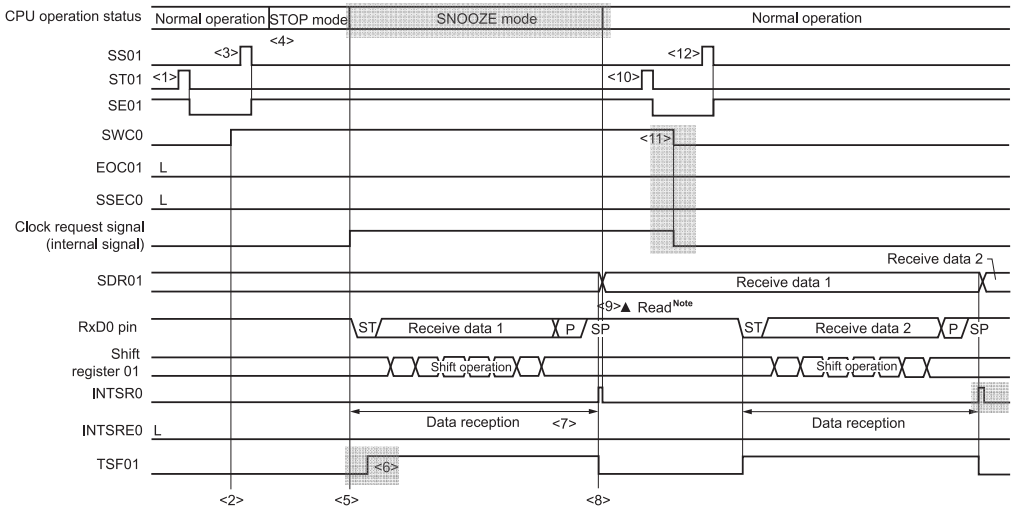
Figure 14-90. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)



(omitted)

Correct:

Figure 14-90. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)

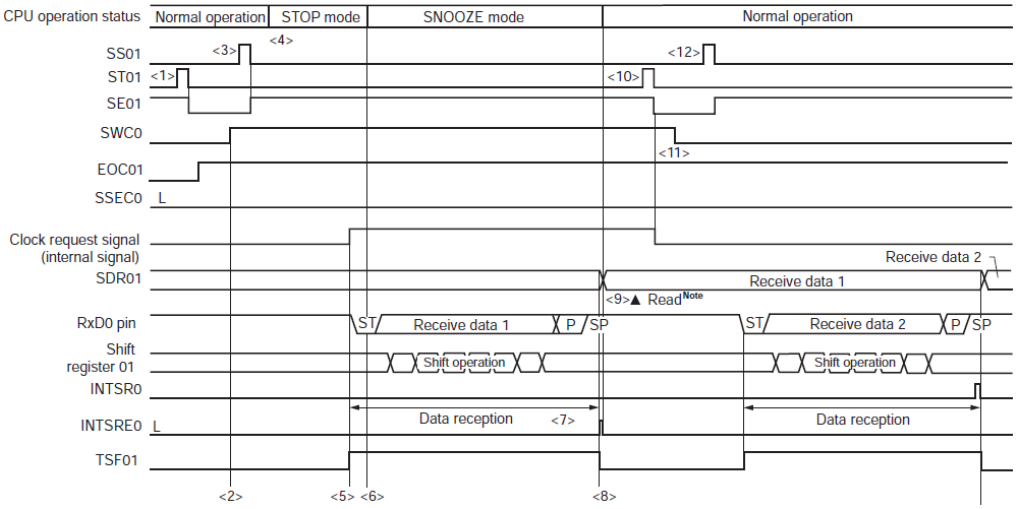


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

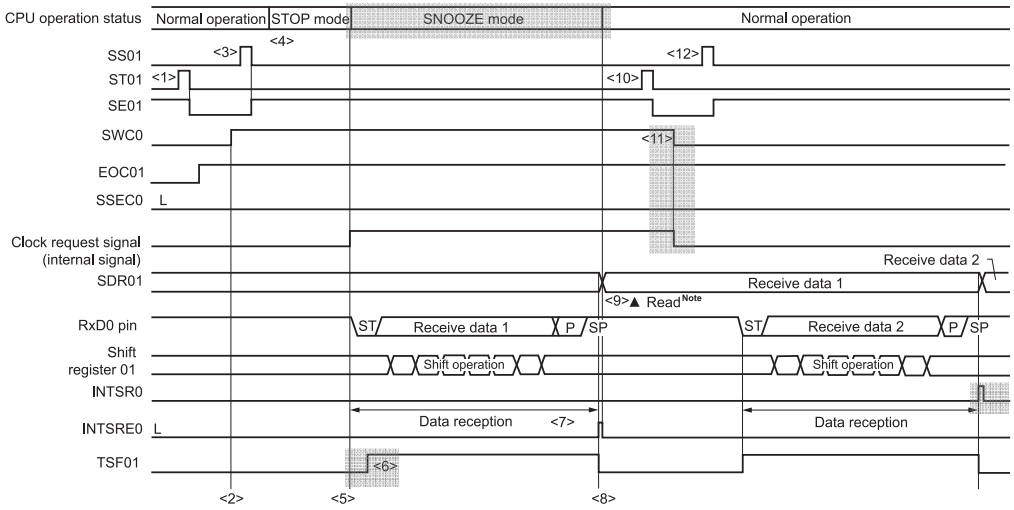
Figure 14-91. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)



(omitted)

Correct:

Figure 14-91. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)

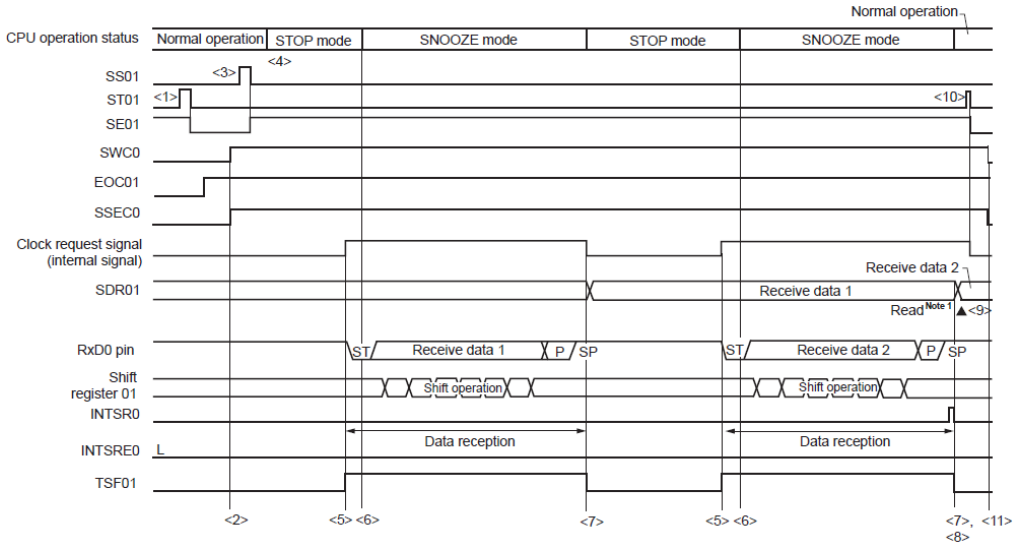


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

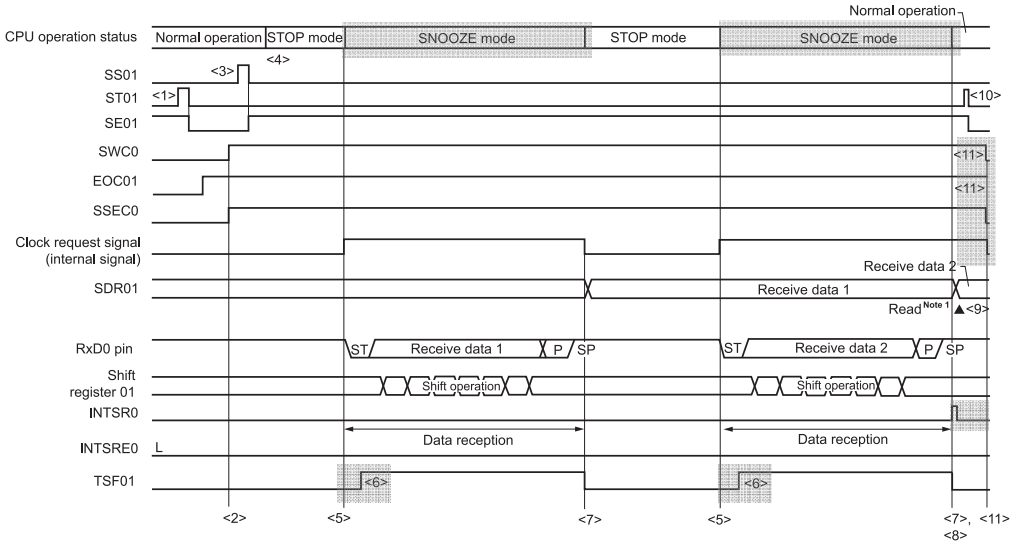
Figure 14-93. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

Correct:

Figure 14-93. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

5. 19.4.3 Multiple interrupt servicing

Table 19-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing (Page 864)

Incorrect:

Table 19-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request / Interrupt Being Serviced		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0 ISP0 = 0	○	×	×	×	×	×	×	×	○
	ISP1 = 0 ISP0 = 1	○	×	○	×	×	×	×	×	○
	ISP1 = 1 ISP0 = 0	○	×	○	×	○	×	×	×	○
	ISP1 = 1 ISP0 = 1	○	○	○	○	○	○	○	○	○
Software interrupt		○	×	○	×	○	×	○	×	○

(omitted)

Correct:

Table 19-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request / Interrupt Being Serviced		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0 ISP0 = 0	○	×	×	×	×	×	×	×	○
	ISP1 = 0 ISP0 = 1	○	×	○	×	×	×	×	×	○
	ISP1 = 1 ISP0 = 0	○	×	○	×	○	×	×	×	○
	ISP1 = 1 ISP0 = 1	○	×	○	×	○	×	○	×	○
Software interrupt		○	×	○	×	○	×	○	×	○

(omitted)

6. 23.2 Configuration of Power-on-reset Circuit
Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1) (Page 900)

Incorrect:

Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the externally input reset signal on the $\overline{\text{RESET}}$ pin is used

(omitted)

Notes 3. The time until normal operation starts includes the following reset processing time when the external reset is released (after the first release of POR) after the $\overline{\text{RESET}}$ signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.51 V, typ.) is reached.
Reset processing time when the external reset is released is shown below.
After the first release of POR:

0.672 ms (typ.), 0.832 ms (max.) (when the LVD is in use)
0.399 ms (typ.), 0.519 ms (max.) (when the LVD is off)

4. Reset processing time when the external reset is released after the second release of POR is shown below.
After the second release of POR:

0.531 ms (typ.), 0.675 ms (max.) (when the LVD is in use)
0.259 ms (typ.), 0.362 ms (max.) (when the LVD is off)

(omitted)

Correct:

Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the externally input reset signal on the $\overline{\text{RESET}}$ pin is used

(omitted)

Notes 3. The time until normal operation starts includes the following reset processing time when the external reset is released (release from the first external reset following release from the POR state) after the $\overline{\text{RESET}}$ signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.51 V, typ.) is reached.
Reset processing time when the external reset is released is shown below.
Release from the first external reset following release from the POR state:

0.672 ms (typ.), 0.832 ms (max.) (when the LVD is in use)
0.399 ms (typ.), 0.519 ms (max.) (when the LVD is off)

4. Reset times in cases of release from an external reset other than the above are listed below.
Release from the reset state for external resets other than the above case:

0.531 ms (typ.), 0.675 ms (max.) (when the LVD is in use)
0.259 ms (typ.), 0.362 ms (max.) (when the LVD is off)

(omitted)

7. 32.1 Absolute Maximum Ratings (Page 1001)

Incorrect:

Absolute Maximum Ratings (3/3)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P07, **P14 to P17**, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−40	mA
		Total of all pins −170 mA	P00 to P07, **P14 to P17**, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−170	mA
	I_{OH2}	Per pin	**P10 to P13, P20 to P27**	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00 to P07, **P14 to P17**, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
		Total of all pins 170 mA	P40 to P47, P130	70	mA
			P00 to P07, **P14 to P17**, P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
	I_{OL2}	Per pin	**P10 to P13, P20 to P27**	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Correct:

Absolute Maximum Ratings (3/3)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−40	mA
		Total of all pins −170 mA	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−170	mA
	I_{OH2}	Per pin	P20, P21	−0.5	mA
		Total of all pins		−1	mA
Output current, low	I_{OL1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
		Total of all pins 170 mA	P40 to P47, P130	70	mA
			P00 to P07, P10 to P17, P22 to P27,P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
	I_{OL2}	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

8. 32.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 1056)

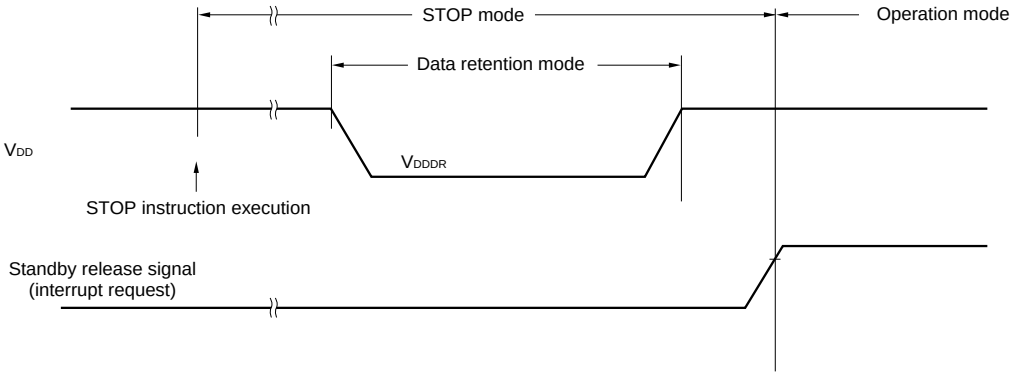
Old:

32.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



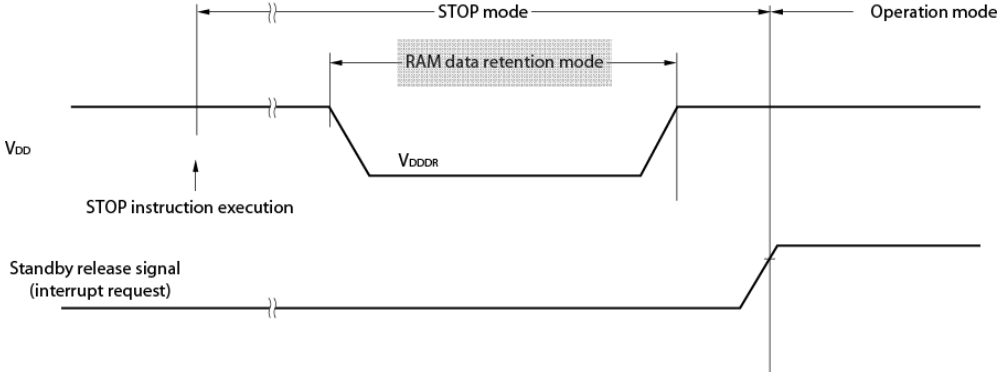
New:

32.8 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



9. 33.1 Absolute Maximum Ratings (Page 1065)

Incorrect:

Absolute Maximum Ratings (3/3)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P07, **P14 to P17**, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−40	mA
		Total of all pins −170 mA	P00 to P07, **P14 to P17**, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−170	mA
	I_{OH2}	Per pin	**P10 to P13, P20 to P27**	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00 to P07, **P14 to P17**, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
		Total of all pins 170 mA	P40 to P47, P130	70	mA
			P00 to P07, **P14 to P17**, P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
	I_{OL2}	Per pin	**P10 to P13, P20 to P27**	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Correct:

Absolute Maximum Ratings (3/3)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−40	mA
		Total of all pins −170 mA	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−170	mA
	I_{OH2}	Per pin	P20, P21	−0.5	mA
		Total of all pins		−1	mA
Output current, low	I_{OL1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
		Total of all pins 170 mA	P40 to P47, P130	70	mA
			P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
	I_{OL2}	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

10. 33.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 1114)

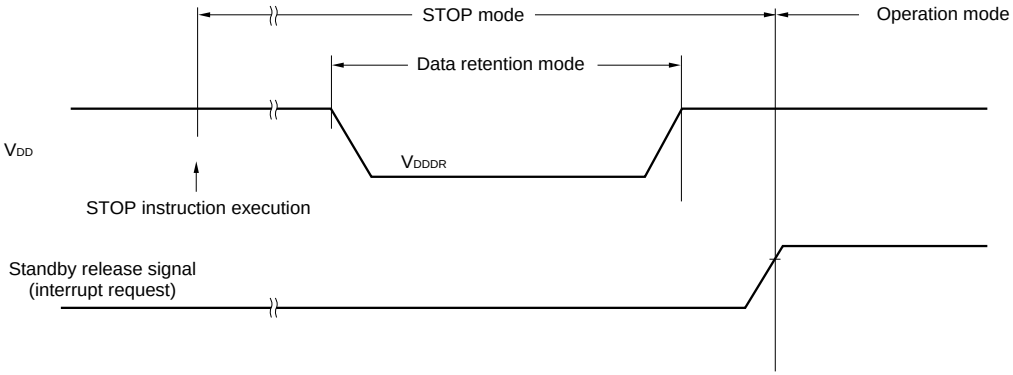
Old:

33.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



New:

33.8 RAM Data Retention Characteristics

(T_A = –40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.