Date: Oct 29, 2014

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A032A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/L12 Descriptions in the User's Manual: Hardware Rev. 2.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/L12 Group	Lot No. All lots	Reference Document	RL78/L12 User's Manual: Hardware Rev. 2.00 R01UH0330EJ0200 (Dec. 2013)		

This document describes misstatements found in the RL78/L12 User's Manual: Hardware Rev. 2.00 (R01UH0330EJ0200).

Corrections

Applicable Item	Applicable Page	Contents
5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)	Page 147	Incorrect descriptions revised
12.5.7 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 12-69. and Figure 12-71)	Pages 468 and 470	Incorrect descriptions revised
12.6.3 SNOOZE mode function	Page 494	Incorrect descriptions revised
12.6.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 12-88., Figure 12-89. and Figure 12-91.)	Pages 496, 497 and 499	Incorrect descriptions revised
17.3.1 Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L)	Page.708	Incorrect descriptions revised
17.3.2 Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L)	Page.710	Incorrect descriptions revised
17.4.3 Multiple interrupt servicing Table 17-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing	Page 720	Incorrect descriptions revised
21.2 Configuration of Power-on-reset Circuit Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)	Page 756	Incorrect descriptions revised
30.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	Page 910	Content change
31.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	Page 959	Content change

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0330EJ0200	
1	5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)		Page 147	Page 3
2	12.5.7 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 12-69. and Figure 12-71)		Pages 468 and 470	Page 4 and 5
3	12.6.3 SNOOZE mode function		Page 494	Page 6
4	12.6.3 SNOOZE mode function Timing Chart of SNOOZE Mode Operation (Figure 12-88., Figure 12-89. and Figure 12-91.)		Pages 496, 497 and 499	Page 7 to 9
5	17.3.1 Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L)		Page.708	Page 10
6	17.3.2 Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L)		Page.710	Page 11
7	17.4.3 Multiple interrupt servicing Table 17-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing		Page 720	Page 12
8	21.2 Configuration of Power-on-reset Circuit Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)		Page 756	Page 13
9	30.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics		Page 910	Page 14
10	31.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics		Page 959	Page 15

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/L12 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A032A/E	Oct. 29, 2014	First edition issued Corrections No.1 to No.10 revised (this document)

1. 5.3.9 High-speed on-chip oscillator trimming register (HIOTRM) (Page 147)

Incorrect:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined [Note] R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
•	•	•	•	•	•	
•	•	•	•	•	•	
•	•	•	•	•	•	
1	1	1	1	1	0	
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remarks 1. The HIOTRM register can be used to adjust the high-speed on-chip oscillator clock to an accuracy within about 0.05%.

2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

Correct:

5.3.9 High-speed on-chip oscillator trimming register (HIOTRM)

(omitted)

Figure 5-10. Format of High-Speed On-Chip Oscillator Trimming Register (HIOTRM)

Address: F00A0H After reset: undefined [Note] R/W

Symbol	7	6	5	4	3	2	1	0
HIOTRM	0	0	HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0

HIOTRM5	HIOTRM4	HIOTRM3	HIOTRM2	HIOTRM1	HIOTRM0	High-speed on-chip oscillator
0	0	0	0	0	0	Minimum speed
0	0	0	0	0	1	
0	0	0	0	1	0	
0	0	0	0	1	1	
0	0	0	1	0	0	
•	•	•	•	•	•	
•	•	•	•	•	•	
•	•	•	•	•	•	
1	1	1	1	1	0	
1	1	1	1	1	1	Maximum speed

Note The value after reset is the value adjusted at shipment.

Remarks 1. The HIOTRM register holds a six-bit value used to adjust the high-speed on-chip oscillator with an increment of 1 corresponding to an increase of frequency by about 0.05%.

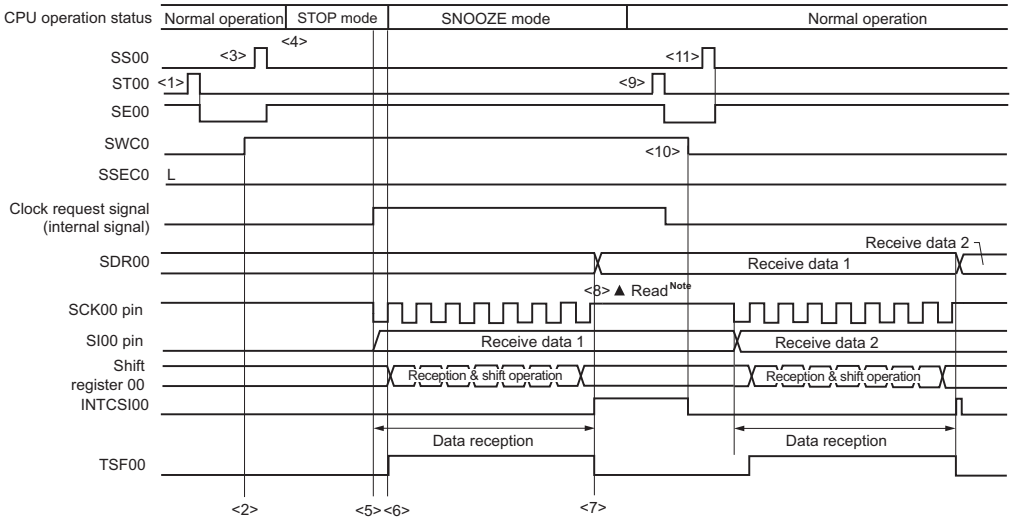
2. For the usage example of the HIOTRM register, see the application note for RL78 MCU series High-speed On-chip Oscillator (HOCO) Clock Frequency Correction (R01AN0464).

2. 14.5.7 SNOOZE mode function

Timing Chart of SNOOZE Mode Operation (Figure 12-69. and Figure 12-71.) (Pages 468 and 470)

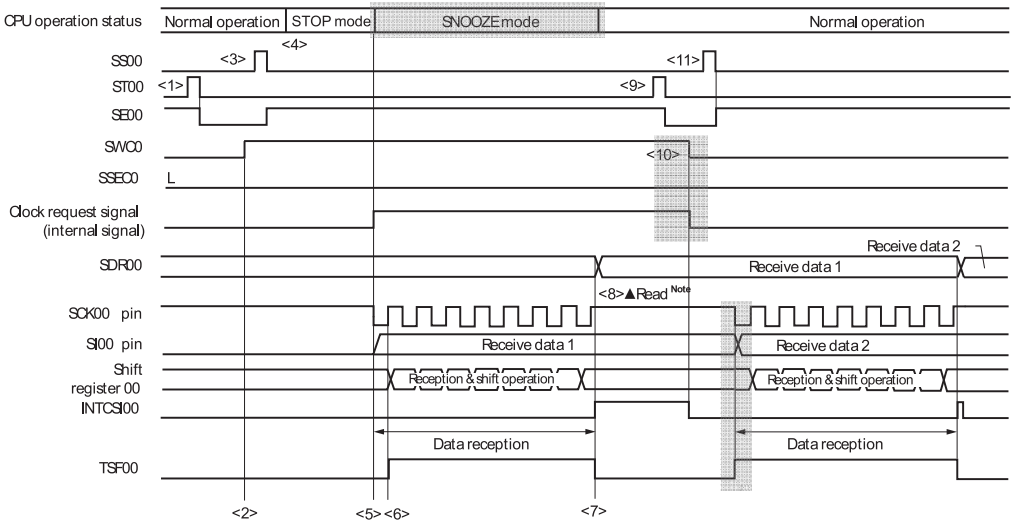
It is correction of “CPU operation status”, “Clock request signal (internal signal)” and “TSF00” in this Figure.

Incorrect:
Figure 12-69. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

Correct:
Figure 12-69. Timing Chart of SNOOZE Mode Operation (once startup)
(Type 1: DAPmn = 0, CKPmn = 0)

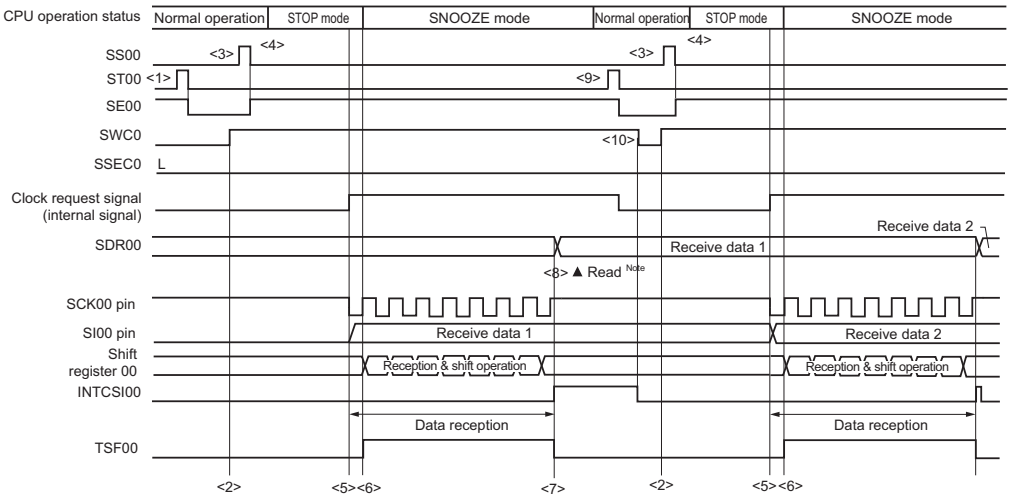


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)” and “INTCSI00” in this Figure.

Incorrect:

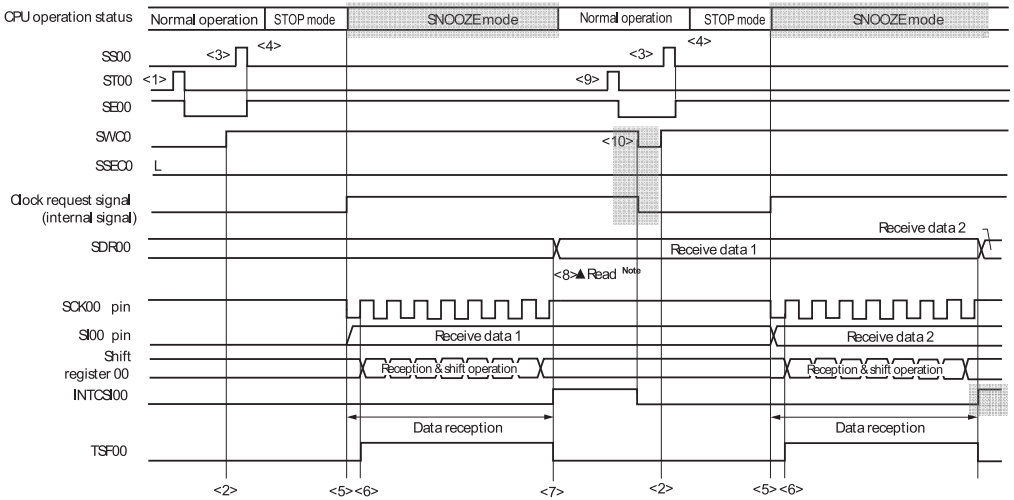
Figure 12-71. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

Correct:

Figure 12-71. Timing Chart of SNOOZE Mode Operation (continuous startup)
(Type 1: DAPmn = 0, CKPmn = 0)



(omitted)

3. 12.6.3 SNOOZE mode function (Page 494)

Incorrect:

12.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

Correct:

12.6.3 SNOOZE mode function

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

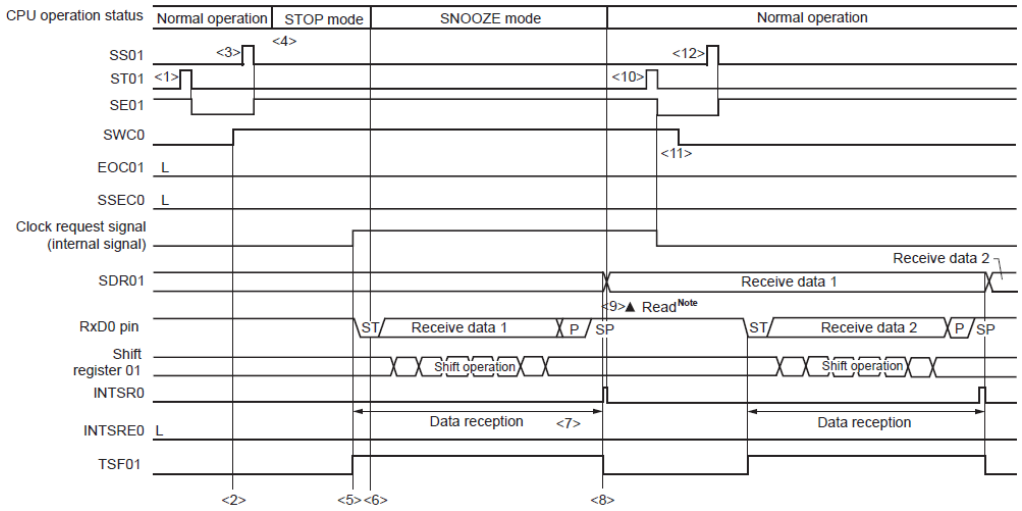
5. The CPU shifts from the STOP mode to the SNOOZE mode on detecting the valid edge of the RxDq signal. Note, however, that transfer through the UART channel may not start and the CPU may remain in the SNOOZE mode if an input pulse on the RxDq pin is too short to be detected as a start bit. In such cases, data may not be received correctly, and this may lead to a framing error or parity error in the next UART transfer.

4. 12.6.3 SNOOZE mode function
Timing Chart of SNOOZE Mode Operation (Figure 12-88., Figure 12-89. and Figure 12-91.) (Pages 496, 497 and 499)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

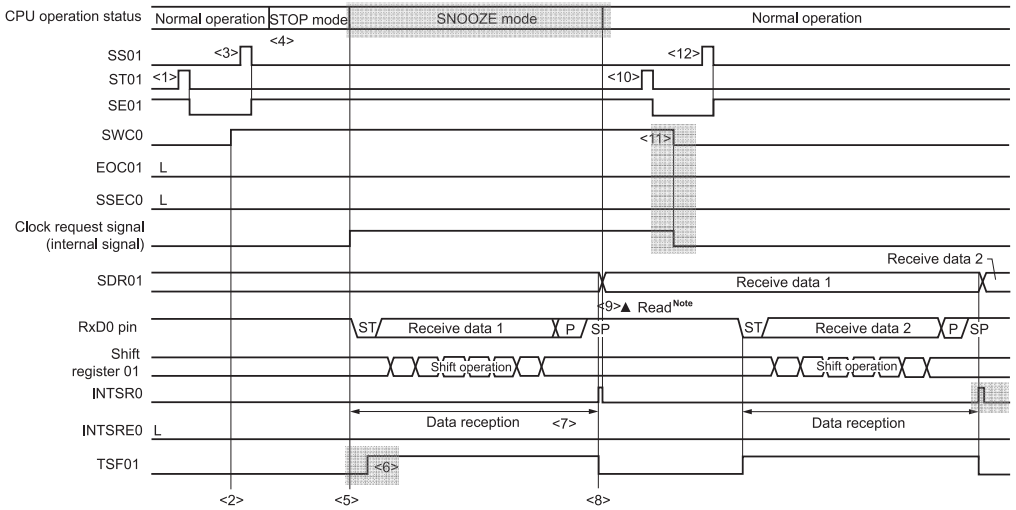
Figure 12-88. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)



(omitted)

Correct:

Figure 12-88. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)

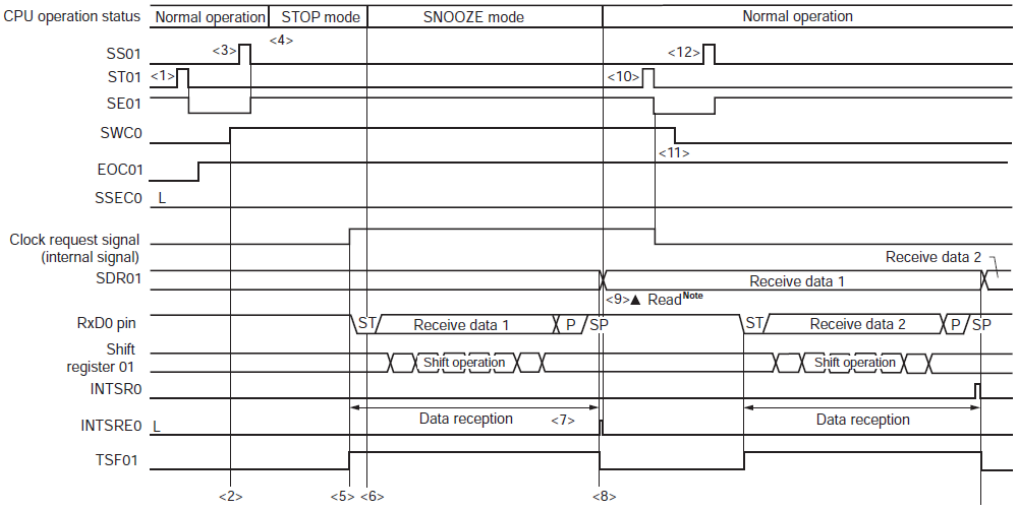


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

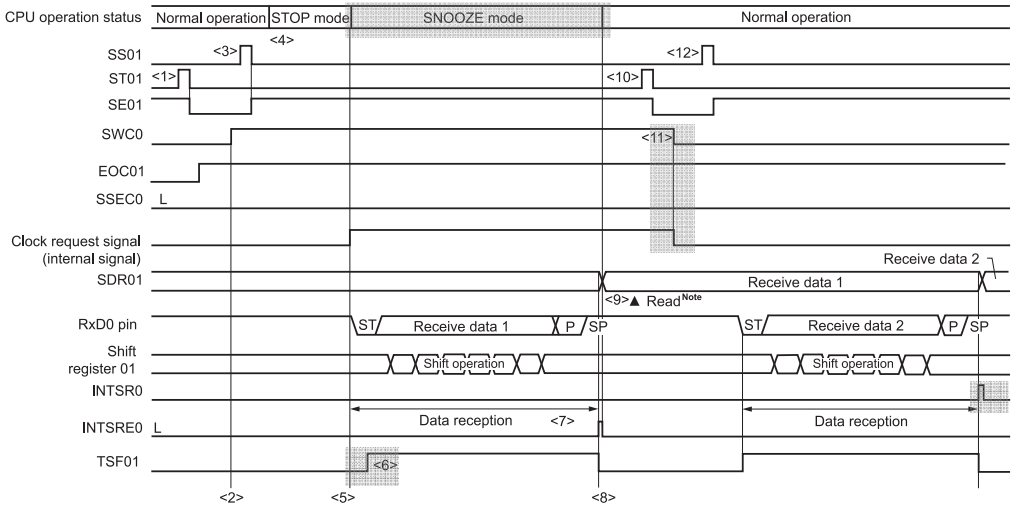
Figure 12-89. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)



(omitted)

Correct:

Figure 12-89. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)

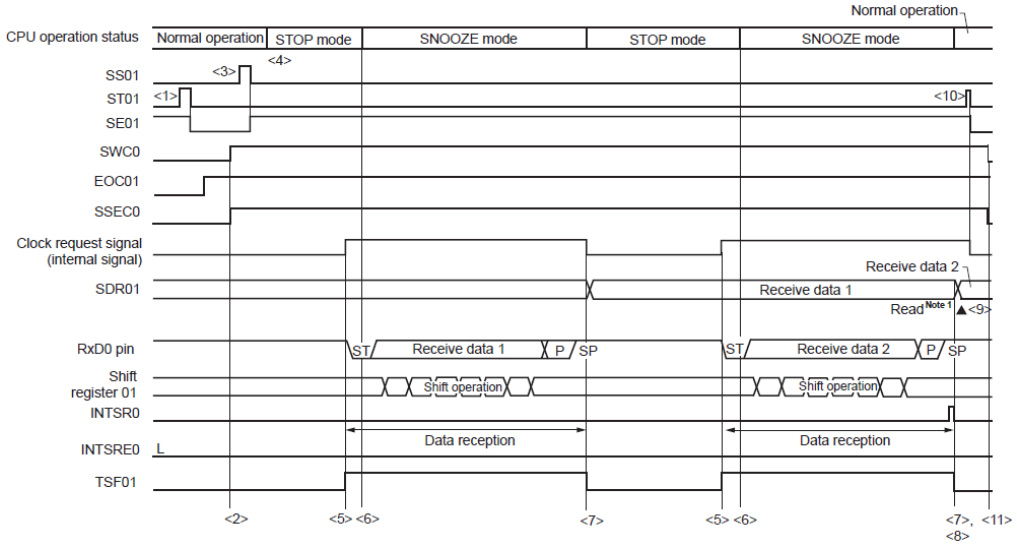


(omitted)

It is correction of “CPU operation status”, “Clock request signal (internal signal)”, “INTSR0” and “TSF01” in this Figure.

Incorrect:

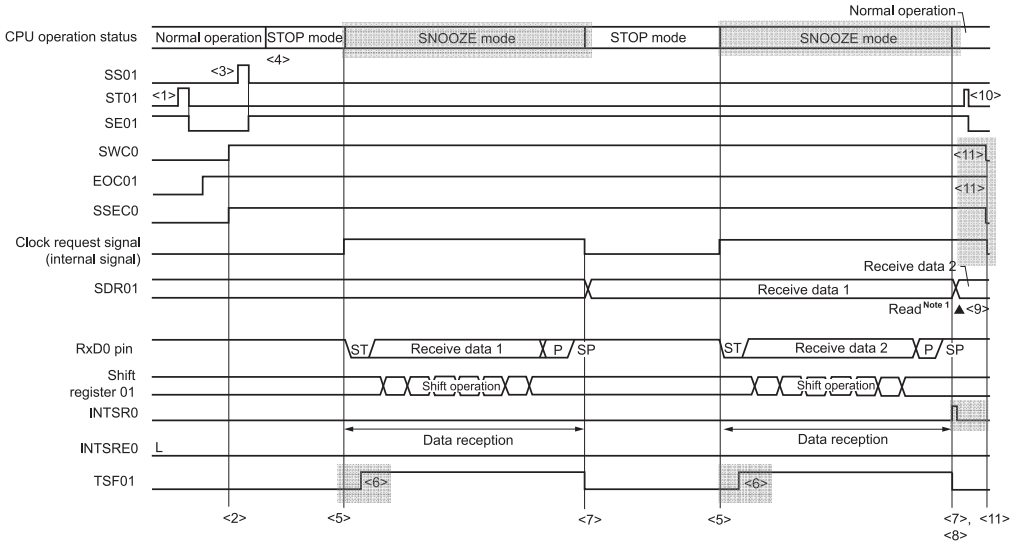
Figure 12-91. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

Correct:

Figure 12-91. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



(omitted)

5. 17.3.1 Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L)

Figure 17-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L) (64-pin products)(p.708)

Incorrect:

Figure 17-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L) (64-pin products)

Address: FFFD0H After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
IF2L	0	0	0	FLIF	MDIF	PIF7	PIF6	0

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Correct:

Figure 17-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L) (64-pin products)

Address: FFFD0H After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	0
IF2L	0	0	0	FLIF	MDIF	PIF7	PIF6	0

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

6. 17.3.2 Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L) Figure 17-3. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L)(64-pin products)(p.710)

Incorrect:

Figure 17-3. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L)(64-pin products)

Address: FFFD4H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
MK2L	1	1	1	FLMK	MDMK	PMK7	PMK6	0

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Correct:

Figure 17-3. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L)(64-pin products)

Address: FFFD4H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	0
MK2L	1	1	1	FLMK	MDMK	PMK7	PMK6	1

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

7. 17.4.3 Multiple interrupt servicing
Table 17-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing (Page 720)

Incorrect:

Table 17-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request / Interrupt Being Serviced		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0 ISP0 = 0	○	×	×	×	×	×	×	×	○
	ISP1 = 0 ISP0 = 1	○	×	○	×	×	×	×	×	○
	ISP1 = 1 ISP0 = 0	○	×	○	×	○	×	×	×	○
	ISP1 = 1 ISP0 = 1	○	○	○	○	○	○	○	○	○
Software interrupt		○	×	○	×	○	×	○	×	○

(omitted)

Correct:

Table 17-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request / Interrupt Being Serviced		Maskable Interrupt Request								Software Interrupt Request
		Priority Level 0 (PR = 00)		Priority Level 1 (PR = 01)		Priority Level 2 (PR = 10)		Priority Level 3 (PR = 11)		
		IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP1 = 0 ISP0 = 0	○	×	×	×	×	×	×	×	○
	ISP1 = 0 ISP0 = 1	○	×	○	×	×	×	×	×	○
	ISP1 = 1 ISP0 = 0	○	×	○	×	○	×	×	×	○
	ISP1 = 1 ISP0 = 1	○	×	○	×	○	×	○	×	○
Software interrupt		○	×	○	×	○	×	○	×	○

(omitted)

8. 21.2 Configuration of Power-on-reset Circuit
Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3) (Page 756)

Incorrect:

Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the externally input reset signal on the $\overline{\text{RESET}}$ pin is used

(omitted)

Notes 3. **The time until normal operation starts includes the following reset processing time when the external reset is released (after the first release of POR) after the $\overline{\text{RESET}}$ signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.51 V, typ.) is reached.**
Reset processing time when the external reset is released is shown below.
After the first release of POR:
0.672 ms (typ.), 0.832 ms (max.) (when the LVD is in use)
0.399 ms (typ.), 0.519 ms (max.) (when the LVD is off)

4. **Reset processing time when the external reset is released after the second release of POR is shown below.**
After the second release of POR:
0.531 ms (typ.), 0.675 ms (max.) (when the LVD is in use)
0.259 ms (typ.), 0.362 ms (max.) (when the LVD is off)
(omitted)

Correct:

Figure 21-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the externally input reset signal on the $\overline{\text{RESET}}$ pin is used

(omitted)

Notes 3. The time until normal operation starts includes the following reset processing time when the external reset is released (release from the first external reset following release from the POR state) after the $\overline{\text{RESET}}$ signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.51 V, typ.) is reached.
Reset processing time when the external reset is released is shown below.
Release from the first external reset following release from the POR state:
0.672 ms (typ.), 0.832 ms (max.) (when the LVD is in use)
0.399 ms (typ.), 0.519 ms (max.) (when the LVD is off)

4. Reset times in cases of release from an external reset other than the above are listed below.
Release from the reset state for external resets other than the above case:
0.531 ms (typ.), 0.675 ms (max.) (when the LVD is in use)
0.259 ms (typ.), 0.362 ms (max.) (when the LVD is off)
(omitted)

9. 30.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 910)

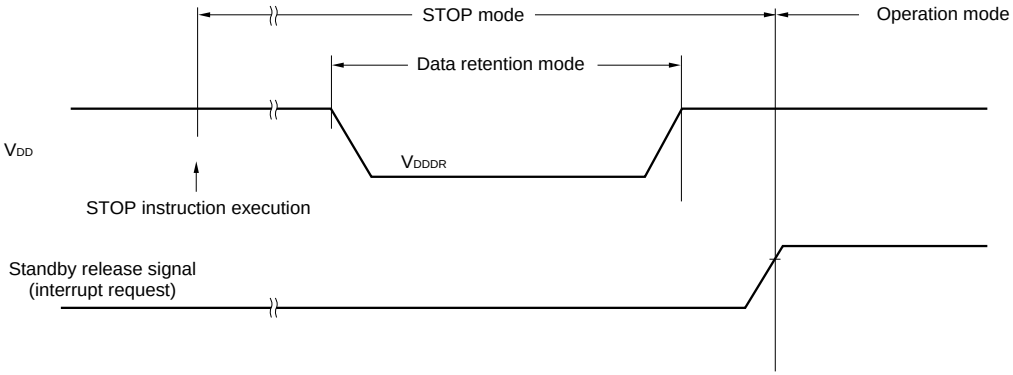
Old:

30.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



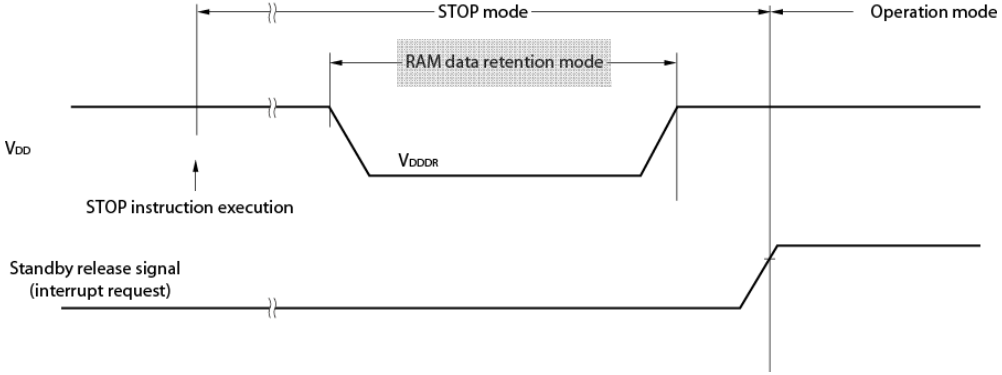
New:

30.8 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



10. 31.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (Page 959)

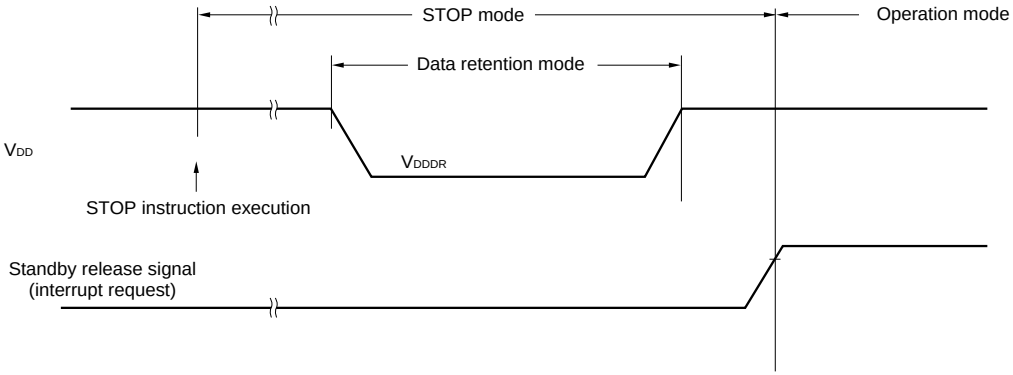
Old:

31.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



New:

31.8 RAM Data Retention Characteristics

(T_A = –40 to +105°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.