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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0129A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/I1C (512KB) Descriptions in the User's Manual: Hardware Rev. 1.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/I1C (512KB) Group	Lot No. All lots	Reference Document	RL78/I1C (512KB) User's Manual: Hardware Rev. 1.10 R01UH0889EJ0110 (Jul. 2023)		

This document describes misstatements found in the RL78/I1C (512KB) User's Manual: Hardware Rev. 1.00 (R01UH0889EJ0110).

Corrections

Applicable Item	Applicable Page	Contents
1.3.1 80-pin product	Page 5	Added description
1.3.2 100-pin product	Page 6	Added description
2.3 Connection of Unused Pins	Page 27	Incorrect descriptions revised
Figure 2-17. Pin Block Diagram for Pin Type 12-1-6	Page 44	Added description
4.2.13 Port 15	Page 107	Incorrect descriptions revised
Table 4-8. Setting Examples of Registers and Output Latches When Using Alternate Function (12/12)	Page 143	Incorrect descriptions revised
4.6.3 Point to Note on the P150 to P152 Pins	New addition	Added description
43.3.1 Pin characteristics	Page 1224	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

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Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
		Document No.	English	R01UH0889EJ0110
1	1.3.1 80-pin product			Page 5	Page 3
2	1.3.2 100-pin product			Page 6	Page 4
3	2.3 Connection of Unused Pins			Page 27	Page 5
4	Figure 2-17. Pin Block Diagram for Pin Type 12-1-6			Page 44	Page 6
5	4.2.13 Port 15			Page 107	Page 7
6	Table 4-8. Setting Examples of Registers and Output Latches When Using Alternate Function (12/12)			Page 143	Page 7
7	4.6.3 Point to Note on the P150 to P152 Pins			New addition	Page 8 to Page 9
8	43.3.1 Pin characteristics			Page 1224	Page 10

Incorrect: Bold with underline; Correct: Gray hatched

Revision History No,

RL78/G16 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0129A/E	Nov. 29, 2023	First edition issued Corrections No.1 to No.8 revised (this document)

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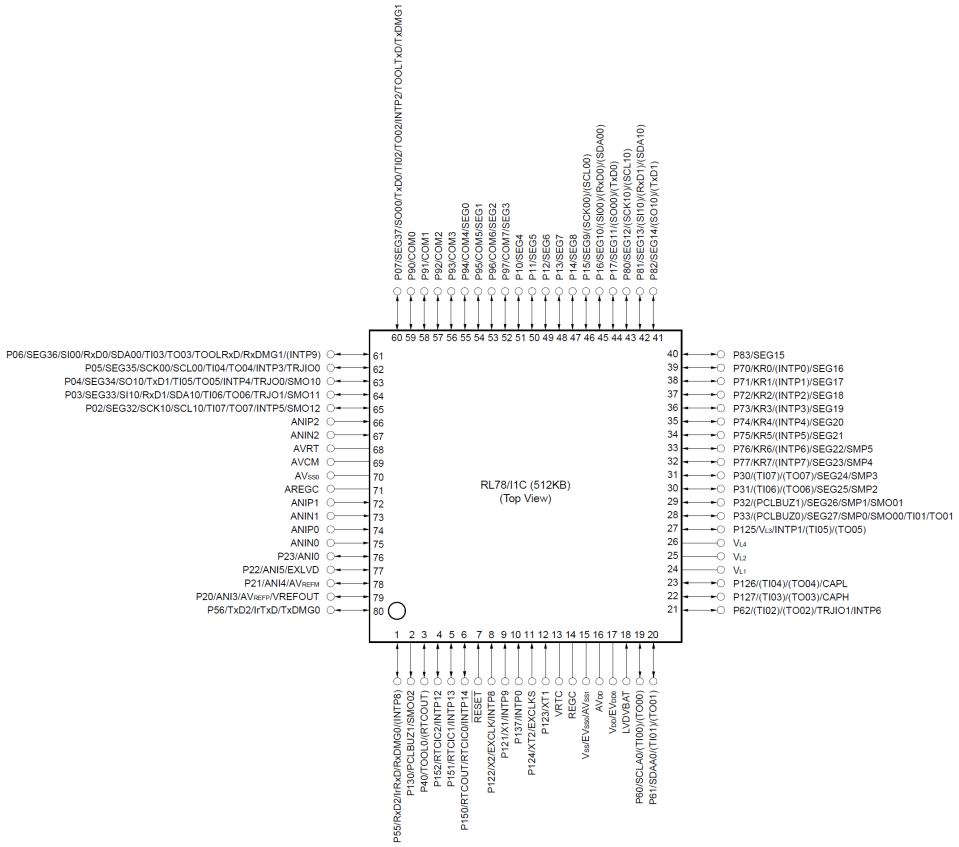
1. 1.3.1 80-pin product (page 5)

Incorrect:

・80-pin plastic LFQFP (12 × 12 mm, 0.5-mm pitch)



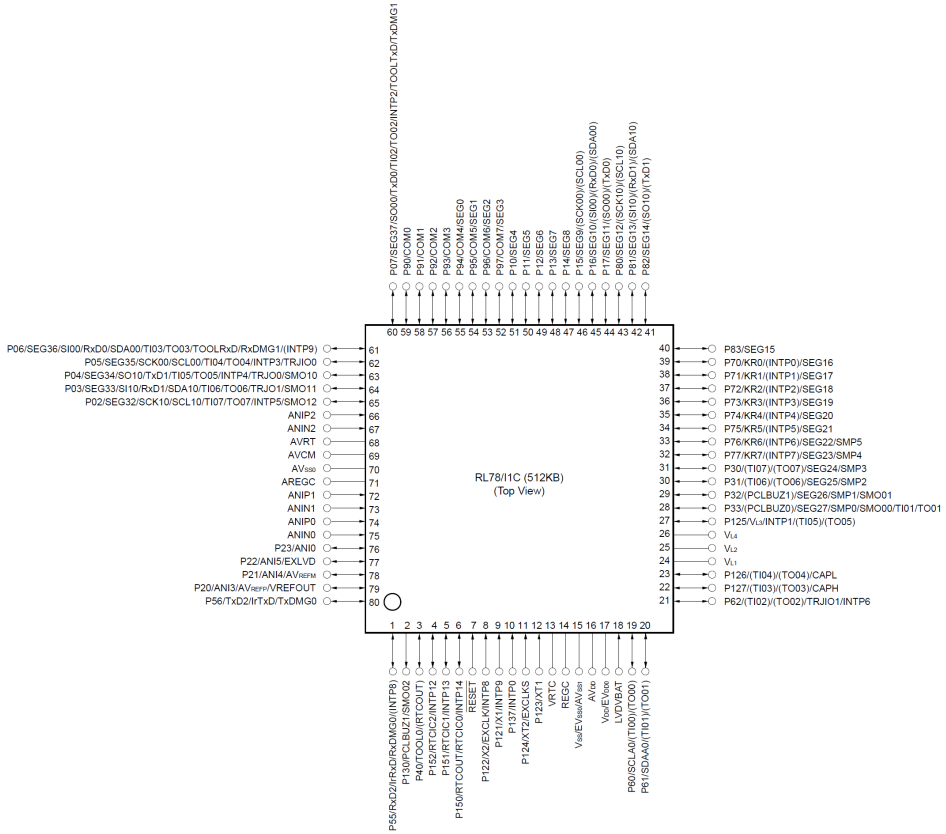
Caution 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1μF).

2. Make the voltage on the AV_{DD} pin the same as that on the V_{DD} and EV_{DD0} pins.

(omitted)

Correct:

・80-pin plastic LFQFP (12 × 12 mm, 0.5-mm pitch)



Caution 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

2. Make the voltage on the AV_{DD} pin the same as that on the V_{DD} and EV_{DD0} pins.

3. When a high-level signal is to be input to any pin among pins P150 to P152 (including if the pin is in use for a multiplexed pin function rather than for GPIO), the pin should always be individually connected via a resistor to V_{DD} or VRTC, whichever of the voltages is higher at the time, or to a voltage higher than both but no higher than 6V.

(omitted)

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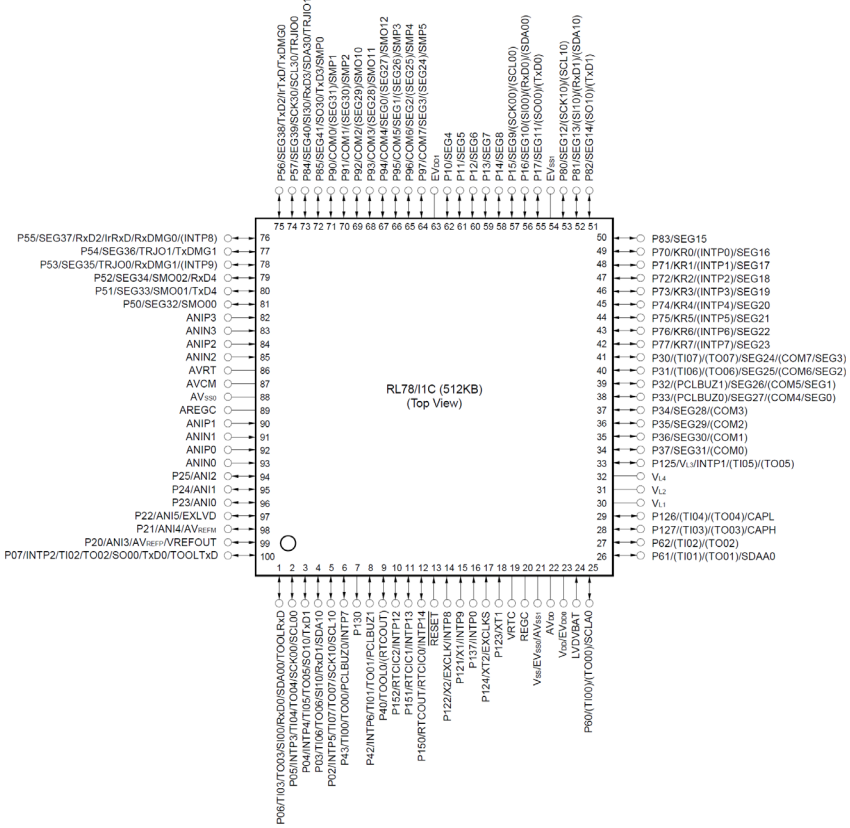
2. 1.3.2 100-pin product (page 6)

Incorrect:

·100-pin plastic LFQFP (14 × 14 mm, 0.5-mm pitch)



Cautions 1. Make the voltage on the EV_{SS1} pin the same as that on the VSS, EV_{SS0}, and AV_{SS1} pins.

2. Make the voltage on the EV_{DD1} pin the same as that on the V_{DD} and EV_{DD0} pins.

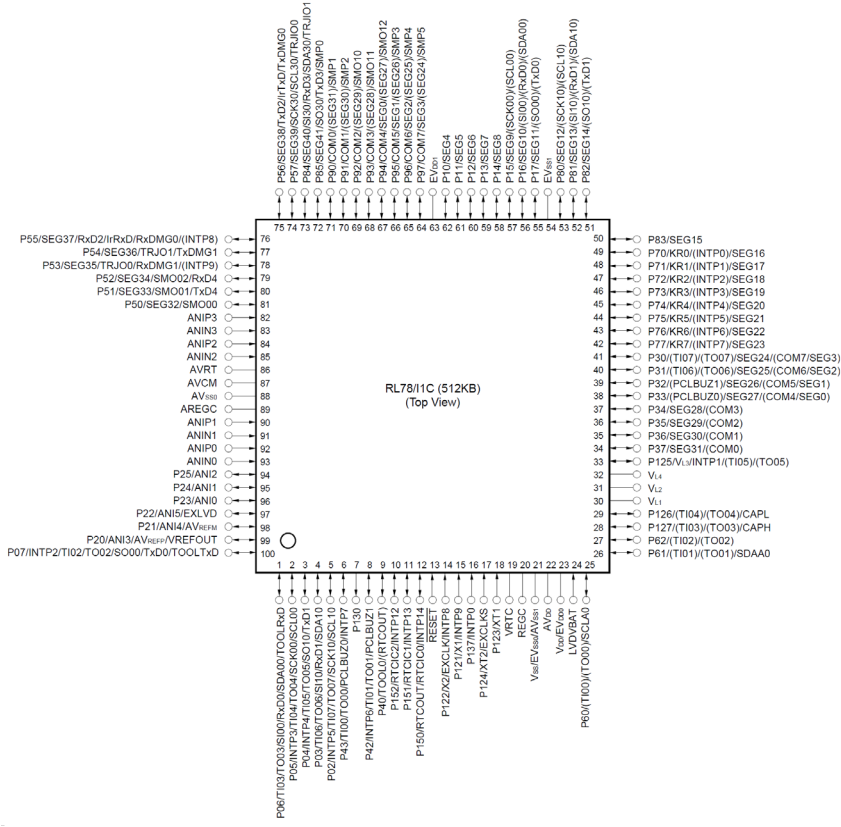
3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

4. Make the voltage on the AV_{DD} pin the same as that on the V_{DD} and EV_{DD0} pins.

(omitted)

Correct:

·100-pin plastic LFQFP (14 × 14 mm, 0.5-mm pitch)



Cautions 1. Make the voltage on the EV_{SS1} pin the same as that on the V_{SS}, EV_{SS0}, and AV_{SS1} pin .

2. Make the voltage on the EV_{DD1} pin the same as that on the V_{DD} and EV_{DD0} pins.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

4. Make the voltage on the AV_{DD} pin the same as that on the V_{DD} and EV_{DD0} pins.

5. When a high-level signal is to be input to any pin among pins P150 to P152 (including if the pin is in use for a multiplexed pin function rather than for GPIO), the pin should always be individually connected via a resistor to V_{DD} or VRTC, whichever of the voltages is higher at the time, or to a voltage higher than both but no higher than 6V.

(omitted)

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3. 2.3 Connection of Unused Pins (page 27)

Incorrect:

Pin Name	I/O	Recommended Connection of Unused Pins
P70 to P77 P80 to P85 P90 to P97	I/O	<When setting to port I/O> Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open. <When setting to segment output> Leave open.
P121, P122	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P123, P124	Input	Independently connect to V_{SS} via a resistor.
P125 to P127	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P130	Output	Leave open.
P137	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P150 to P152	I/O	**Input: Independently connect to V_{SS} via a resistor.** **Output: Set the port's output latch to 0 and leave the pins open, or set the port's output latch to 1 and independently connect the pins to V_{SS} via a resistor.**

Correct:

Pin Name	I/O	Recommended Connection of Unused Pins
P70 to P77 P80 to P85 P90 to P97	I/O	<When setting to port I/O> Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open. <When setting to segment output> Leave open.
P121, P122	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P123, P124	Input	Independently connect to V_{SS} via a resistor.
P125 to P127	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P130	Output	Leave open.
P137	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P150 to P152	I/O	Set these pins to the input mode, and individually connect each of them via a resistor to Vss.

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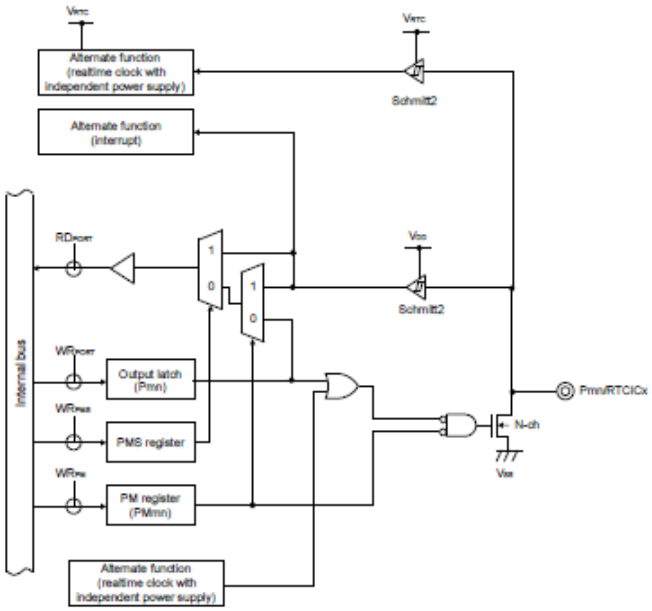
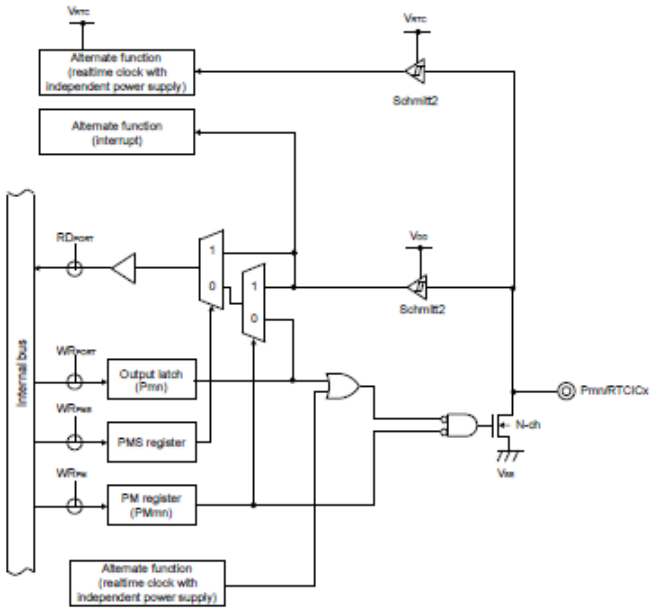
4. Figure 2-17. Pin Block Diagram for Pin Type 12-1-6 (page 44)

Incorrect:



Correct:



Caution 1 When a high-level signal is to be input to any pin among pins P150 to P152 (including if the pin is in use for a multiplexed pin function rather than for GPIO), the pin should always be individually connected via a resistor to V_{DD} or VRTC, whichever of the voltages is higher at the time, or to a voltage higher than both but no higher than 6V.

Caution 2 A through current may flow through if the pin is in the intermediate potential, because the Input buffer is turned on when the pin is in output mode.

Remarks 1. For alternate functions, see 2.1 Port Function.

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5. 4.2.13 Port 15 (page 107)

Incorrect:

P150 to P152 are I/O port pins with output latches. Port 15 can be set to the input mode or output mode in 1-bit unitsusing port mode register 15 (PM15).

Outputs from the P150 to P152 pins are N-ch open-drain (**V_{DD} tolerant**).

This port can also be used for RTC time capture input, real-time clock correction clock output, and external interrupt request input.

Reset signal generation sets port 15 to the digital input invalid mode.

Note “Digital input invalid” refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

Correct:

P150 to P152 are I/O port pins with output latches. Port 15 can be set to the input mode or output mode in 1-bit unitsusing port mode register 15 (PM15).

Outputs from the P150 to P152 pins are N-ch open-drain (6-V tolerant).

This port can also be used for RTC time capture input, real-time clock correction clock output, and external interrupt request input.

Reset signal generation sets port 15 to input mode.

6. Table 4-8. Setting Examples of Registers and Output Latches When Using Alternate Function (12/12) (page 143)

Incorrect:

Pin Name	Used Function		PIOR0	POM××	PM××	P××	PFSEG×× (ISCVL3, ISCCAP)Note	Alternate Function Output		80-pin	100-pin
	Function Name	I/O						SAU and UARTMG	Other than SAU and UARTMG		
P150	P150	Input	–	×	1	×	–	–	–	√	√
		N-ch open drain output (6 V tolerance)	×	–	0	0/1	–	–	–		
	RTCOUT	Output	PIOR03 = 0	–	0	0	–	–	–		
	RTCIC0	Input	×	–	1	×	–	–	–		
	INTP14	Input	–	–	×	×	–	–	–		
P151	P151	Input	–	×	1	×	–	–	–	√	√
		N-ch open drain output (6 V tolerance)	–	–	0	0/1	–	–	–		
	RTCIC1	Input	–	–	1	×	–	–	–		
	INTP13	Input	–	–	×	×	–	–	–		
P152	P152	Input	–	–	1	×	–	–	–	√	√
		N-ch open drain output (6 V tolerance)	–	–	0	0/1	–	–	–		
	RTCIC2	Input	–	–	1	×	–	–	–		
	INTP12	Input	–	–	×	×	–	–	–		

Correct:

Pin Name	Used Function		PIOR0	POM××	PM××	P××	PFSEG×× (ISCVL3, ISCCAP)Note	TCEN bit	Alternate Function Output		80-pin	100-pin
	Function Name	I/O							SAU and UARTMG	Other than SAU and UARTMG		
P150	P150	Input	–	–	1	×	–	–	–	–	√	√
		N-ch open drain output (6 V tolerance)	–	–	0	0/1	–	0	–	–		
	RTCOUT	Output	PIOR03 = 0	–	0	0	–	0	–	–		
	RTCIC0	Input	–	–	1	×	–	1	–	–		
	INTP14	Input	–	–	1	×	–	–	–	–		
P151	P151	Input	–	–	1	×	–	–	–	–	√	√
		N-ch open drain output (6 V tolerance)	–	–	0	0/1	–	0	–	–		
	RTCIC1	Input	–	–	1	×	–	1	–	–		
	INTP13	Input	–	–	1	×	–	–	–	–		
P152	P152	Input	–	–	1	×	–	–	–	–	√	√
		N-ch open drain output (6 V tolerance)	–	–	0	0/1	–	0	–	–		
	RTCIC2	Input	–	–	1	×	–	1	–	–		
	INTP12	Input	–	–	1	×	–	–	–	–		

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7. 4.6.3 Point to Note on the P150 to P152 (new addition)

Incorrect:

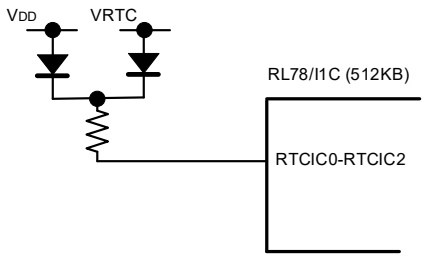
Correct:

4.6.3 Point to Note on the P150 to P152

Note the following points when using a P150/RTCIC0- P152/RTCIC2 pin under any of conditions (1) to (4) stated below.

(1) A pin is in use as a time-capture event input RTCICn (n = 0 to 2).

Setting a TCEN bit in the RTCCRy (y = 0 to 2) register enables operation of the pin as a time-capture input pin (RTCICn). Each of the P150/RTCIC0 to P152/RTCIC2 pins has two input buffers powered by V_{DD} and VRTC. Since the input buffers are always on, a through-current might flow when an intermediate potential is input to the input buffers. Accordingly, configure the circuit as follows such that each pin selected for time-capture input is always individually connected to either V_{DD} or VRTC, whichever of the voltages is higher at the time, or to a voltage higher than both but no higher than 6V. This is to prevent the input of an intermediate potential to the given pin even in cases where, for example, the V_{DD} voltage fluctuates from being greater than or equal to VRTC to being less than VRTC.



Continued on next page

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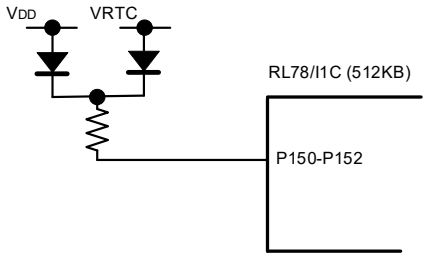
(2) A P150 to P152 pin is in use as an input port pin.

Each of the P150 to P152 pins has two input buffers powered by V_{DD} and VRTC. Since the input buffers are always on, a through-current might flow when an intermediate potential is input to the input buffers. Accordingly, when a high-level signal is to be input to any pin among P150 to P152, configure the circuit as follows so that the pin is always individually connected to either V_{DD} or VRTC, whichever of the voltages is higher at the time, or to a voltage higher than both but no higher than 6V. This is to prevent the input of an intermediate potential to the given pin even in cases where, for example, the V_{DD} voltage fluctuates from being greater than or equal to VRTC to being less than VRTC.



(3) A P150 to P152 pin is in use as an output port (N-ch open-drain output) pin.

When a P150 to P152 pin is in use in the output mode, set the corresponding TCEN bit in the RTCCRy (y = 0 to 2) register to 0. When a high-level signal is to be output from any pin among P150 to P152, handling of the pin is the same as in the input mode. Configure the circuit so that the pin is always individually connected to V_{DD} or VRTC, whichever of the voltages is higher at the time, or to a voltage higher than both but no higher than 6V. When a reset occurs due to the V_{DD} power dropping or being cut off while the output from any of these pins is a low-level signal, they are all set for the input mode.

(4) A P150/RTCIC0 to P152/RTCIC2 pin is not in use.

Set the P150 to P152 pins to the input mode, and individually connect them via a resistor to Vss, in accord with the recommended connection of unused pins.

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8. 43.3.1 Pin characteristics (page 1224)

Incorrect:

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127	Normal input buffer	0.8EV_{DD}		EV_{DD}	V
	V_{IH2}	P02, P03, P05, P06, P15, P16, P42, P43, P52, P53, P55, P57, P80, P81, P84	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	2.2		EV_{DD}	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	2.0		EV_{DD}	V
			TTL input buffer 1.6 V ≤ EV_{DD} < 3.3 V	1.5		EV_{DD}	V
	V_{IH3}	P20 to P25		0.7AV_{DD}		AV_{DD}	V
	V_{IH4}	P60 to P62		0.7EV_{DD}		6.0	V
	V_{IH5}	P121, P122, P137, P150 to P152, EXCLK		0.8V_{DD}		V_{DD}	V
	V_{IH6}	$\overline{\text{RESET}}$		0.8V_{DD}		6.0	V
	V_{IH7}	P123, P124, EXCLKS		0.8V_{RTC}		V_{RTC}	V
Input voltage, low	V_{IL1}	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127	Normal input buffer	0		0.2EV_{DD}	V
	V_{IL2}	P02, P03, P05, P06, P15, P16, P42, P43, P52, P53, P55, P57, P80, P81, P84	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P25		0		0.3AV_{DD}	V
	V_{IL4}	P60 to P62		0		0.3EV_{DD}	V
	V_{IL5}	P121, P122, P137, P150 to P152, EXCLK, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL6}	P123, P124, EXCLKS		0		0.2V_{RTC}	V

(omitted)

Correct:

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127	Normal input buffer	0.8EV_{DD}		EV_{DD}	V
	V_{IH2}	P02, P03, P05, P06, P15, P16, P42, P43, P52, P53, P55, P57, P80, P81, P84	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	2.2		EV_{DD}	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	2.0		EV_{DD}	V
			TTL input buffer 1.6 V ≤ EV_{DD} < 3.3 V	1.5		EV_{DD}	V
	V_{IH3}	P20 to P25		0.7AV_{DD}		AV_{DD}	V
	V_{IH4}	P60 to P62		0.7EV_{DD}		6.0	V
	V_{IH5}	P121, P122, P137, P150 to P152, EXCLK		0.8V_{DD}		V_{DD}	V
	V_{IH6}	$\overline{\text{RESET}}$		0.8V_{DD}		6.0	V
	V_{IH7}	P123, P124, EXCLKS		0.8V_{RTC}		V_{RTC}	V
	V_{IH8}	P150 to P152[Note]		0.8V_{DD}		6.0	V
	V_{IH9}	RTCIC0 to RTCIC2[Note]		0.8V_{RTC}		6.0	V
Input voltage, low	V_{IL1}	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127	Normal input buffer	0		0.2EV_{DD}	V
	V_{IL2}	P02, P03, P05, P06, P15, P16, P42, P43, P52, P53, P55, P57, P80, P81, P84	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P25		0		0.3AV_{DD}	V
	V_{IL4}	P60 to P62		0		0.3EV_{DD}	V
	V_{IL5}	P121, P122, P137, P150 to P152, EXCLK, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL6}	P123, P124, EXCLKS		0		0.2V_{RTC}	V
	V_{IL7}	P150 to P152[Note]		0		0.2V_{DD}	V
	V_{IL8}	RTCIC0 to RTCIC2[Note]		0		0.2V_{RTC}	V

Note When a high-level signal is to be input to any pin among pins P150 to P152 (including if the pin is in use for a multiplexed pin function rather than for GPIO), the pin should always be individually connected via a resistor to V_{DD} or VRTC, whichever of the voltages is higher at the time, or to a voltage higher than both but no higher than 6V.

(omitted)

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