Date: Sep. 21, 2016

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A024D/E	Rev.	4.00
Title	Correction for Incorrect Description Notice RL78/I1A Descriptions in the Hardware User's Manual Rev. 2.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/I1A Group : R5F107xxx	Lot No. All lots	Reference Document	RL78/I1A User's Manual: Hardware Rev.2.10 R01UH0169EJ0210 (Jul. 2013)		

This document describes misstatements found in the RL78/I1A User's Manual: Hardware Rev.2.10 (R01UH0169EJ0210).

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Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/I1A User's Manual: Hardware Rev.2.10 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A024C/E	Apr.24,2015	Third edition issued No.1 to No.21 incorrect descriptions revised
TN-RL*-A046A/E	Jul.06,2015	First edition issued No.22 incorrect descriptions revised
TN-RL*-A024D/E	Sep.21,2016	First edition issued No.23 to No.80 in corrections(This notice)

1. Figure 7-19. Format of Peripheral Function Switch Register 0 (PFSEL0)(p.303)

Incorrect descriptions of the TMRSTEN1 and TMRSTEN0 bits of Peripheral Function Switch Register 0 (PFSEL0) are revised, and Note is added.

Old)

Figure 7-19. Format of Peripheral Function Switch Register 0 (PFSEL0)

Address: F05C6H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0

CMP2STEN	CMP0STEN	Comparator interrupt selection
See **CHAPTER 14 COMPARATOR**.		

PNFEN	Use/Do not use external interrupt INTP20 noise filter
0	Use noise filter
1	Do not use noise filter

ADTRG11	ADTRG10	Timer trigger selection for A/D conversion
0	0	Timer KB0 trigger source
0	1	Timer KB1 trigger source
1	0	Timer KB2 trigger source
1	1	Setting prohibited

TMRSTEN1	Function selection for external interrupt INTP21
0	External interrupt function (external interrupt generation enabled, timer restart disabled)
1	Timer restart function (external interrupt generation disabled, standby release disabled)

TMRSTEN0	Function selection for external interrupt INTP20
0	External interrupt function (external interrupt generation enabled, timer restart disabled)
1	Timer restart function (external interrupt generation disabled, standby release disabled)

Remark See **Figure 14-1 Block Diagram of Comparator**.

New)

Figure 7-19. Format of Peripheral Function Switch Register 0 (PFSEL0)

Address: F05C6H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0

CMP2STEN	CMP0STEN	Comparator interrupt selection
See **CHAPTER 14 COMPARATOR**.		

PNFEN	Use/Do not use external interrupt INTP20 noise filter
0	Use noise filter
1	Do not use noise filter

ADTRG11	ADTRG10	Timer trigger selection for A/D conversion
0	0	Timer KB0 trigger source
0	1	Timer KB1 trigger source
1	0	Timer KB2 trigger source
1	1	Setting prohibited

TMRSTEN1	Switch of external interrupt INTP21 **Note**
0	External interrupt function is selected (stop mode release enabled, timer restart disabled).
1	Timer restart function is selected (stop mode release disabled, timer restart enabled).

TMRSTEN0	Switch of external interrupt INTP20 **Note**
0	External interrupt function is selected (stop mode release enabled, timer restart disabled).
1	Timer restart function/forced output stop function 2 is selected (stop mode release disabled, timer restart enabled).

Note When INTP20 or INTP21 is used as a trigger of the timer KB forced output stop function 2 or timer restart function, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

Remark See **Figure 14-1 Block Diagram of Comparator**.

2. Figure7-73.Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p)(p.380~p.381)

Incorrect descriptions of forced output stop function control register 0p (TKBPACTL0p) are revised, and Note is added.

Old)

Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (1/2)

Address: F0630H (TKBPACTL00), F0632H (TKBPACTL01) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL0p	TKBPAFXS0p3	TKBPAFXS0p2	TKBPAFXS0p1	TKBPAFXS0p0	0	0	0	TKBPAFCM0p

7	6	5	4	3	2	1	0
0	TKBPAHZS0p2	TKBPAHZS0p1	TKBPAHZS0p0	TKBPAHCM0p1	TKBPAHCM0p0	TKBPAMD0p1	TKBPAMD0p0

TKBPAFXS0p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	**INTP20 can be used as a trigger.**

TKBPAFXS0p2	Comparator trigger selection for forced output stop function 2
0	Comparator 2 can not be used as a trigger.
1	**Comparator 2 can be used as a trigger.**

TKBPAFXS0p1	Comparator trigger selection for forced output stop function 2
0	Comparator 1 can not be used as a trigger.
1	**Comparator 1 can be used as a trigger.**

TKBPAFXS0p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAFCM0p	Operation mode selection for forced output stop function 2
0	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period.**
1	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.**

Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (2/2)

TKBPAHZS0p2	Comparator trigger selection for forced output stop function 1
0	Comparator 2 can not be used as a trigger.
1	**Comparator 2 can be used as a trigger.**

TKBPAHZS0p1	Comparator trigger selection for forced output stop function 1
0	Comparator 1 can not be used as a trigger.
1	**Comparator 1 can be used as a trigger.**

TKBPAHZS0p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAHCM0p1	TKBPAHCM0p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT0)** = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT0)** = 1" is invalid. Forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT0)** = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT0)** = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT0)** = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT0)** = 1 is written when the trigger signal is in its inactive period.

TKBPAMD0p1	TKBPAMD0p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Cautions 1. During timer operation, setting the other bits of the TKBPACTL0p register is prohibited. However, the TKBPACTL0p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (1/2)

Address: F0630H (TKBPACTL00), F0632H (TKBPACTL01) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL0p	TKBPAFXS0p3	TKBPAFXS0p2	TKBPAFXS0p1	TKBPAFXS0p0	0	0	0	TKBPAFCM0p
	7	6	5	4	3	2	1	0
	0	TKBPAHZS0p2	TKBPAHZS0p1	TKBPAHZS0p0	TKBPAHCM0p1	TKBPAHCM0p0	TKBPAMD0p1	TKBPAMD0p0

TKBPAFXS0p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	INTP20 can be used as a trigger. Note 1

TKBPAFXS0p2	Comparator trigger selection for forced output stop function 2
0	Comparator 2 can not be used as a trigger.
1	Comparator 2 can be used as a trigger. Note 2

TKBPAFXS0p1	Comparator trigger selection for forced output stop function 2
0	Comparator 1 can not be used as a trigger.
1	Comparator 1 can be used as a trigger. Note 3

TKBPAFXS0p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. Note 2

TKBPAFCM0p	Operation mode selection for forced output stop function 2
0	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period. Note 4
1	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger. Note 4

TKBPAHZS0p2	Comparator trigger selection for forced output stop function 1
0	Comparator 2 can not be used as a trigger.
1	Comparator 2 can be used as a trigger. Note 2

TKBPAHZS0p1	Comparator trigger selection for forced output stop function 1
0	Comparator 1 can not be used as a trigger.
1	Comparator 1 can be used as a trigger. Note 3

TKBPAHZS0p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. Note 2

Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (2/2)

TKBPAHCM0p1	TKBPAHCM0p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT0p) = 1" is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level. **Note 4**
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT0p) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written when the trigger signal is in its inactive period. **Note 4**

TKBPAMD0p1	TKBPAMD0p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Notes 1. When INTP20 is used as the forced output stop function 2, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

2. When CMP0 or CMP2 is used as the timer KB forced output stop function, set CMPnSTEN = 1. See **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

3. When CMP1 is used as the timer KB forced output stop function, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

4. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).

Cautions 1. During timer operation, setting the other bits of the TKBPACTL0p register is prohibited. However, the TKBPACTL0p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

3. Figure7-74.Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p)(p.382~p.383)

Incorrect descriptions of forced output stop function control register 1p (TKBPACTL1p) are revised, and Note is added.

Old)

Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) (1/2)

Address: F0670H (TKBPACTL10), F0672H (TKBPACTL11) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL1p	TKBPAFXS1p3	TKBPAFXS1p2	TKBPAFXS1p1	TKBPAFXS1p0	0	0	0	TKBPAFCM1p
	7	6	5	4	3	2	1	0
	0	TKBPAHZS1p2	TKBPAHZS1p1	TKBPAHZS1p0	TKBPAHCM1p1	TKBPAHCM1p0	TKBPAMD1p1	TKBPAMD1p0

TKBPAFXS1p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	**INTP20 can be used as a trigger.**

TKBPAFXS1p2	Comparator trigger selection for forced output stop function 2
0	Comparator 3 can not be used as a trigger.
1	**Comparator 3 can be used as a trigger.**

TKBPAFXS1p1	Comparator trigger selection for forced output stop function 2
0	Comparator 2 can not be used as a trigger.
1	**Comparator 2 can be used as a trigger.**

TKBPAFXS1p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAFCM1p	Operation mode selection for forced output stop function 2
0	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period.**
1	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.**

Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) (2/2)

TKBPAHZS1p2	Comparator trigger selection for forced output stop function 1
0	Comparator 3 can not be used as a trigger.
1	**Comparator 3 can be used as a trigger.**

TKBPAHZS1p1	Comparator trigger selection for forced output stop function 1
0	Comparator 2 can not be used as a trigger.
1	**Comparator 2 can be used as a trigger.**

TKBPAHZS1p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAHCM1p1	TKBPAHCM1p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT1)** = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT1)** = 1" is invalid. Forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT1)** = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT1)** = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT1)** = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT1)** = 1 is written when the trigger signal is in its inactive period.

TKBPAMD1p1	TKBPAMD1p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Cautions 1. During timer operation, setting the other bits of the TKBPACTL1p register is prohibited. However, the TKBPACTL1p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) (1/2)

Address: F0670H (TKBPACTL10), F0672H (TKBPACTL11) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL1p	TKBPAFXS1p3	TKBPAFXS1p2	TKBPAFXS1p1	TKBPAFXS1p0	0	0	0	TKBPAFCM1p
	7	6	5	4	3	2	1	0
	0	TKBPAHZS1p2	TKBPAHZS1p1	TKBPAHZS1p0	TKBPAHCM1p1	TKBPAHCM1p0	TKBPAMD1p1	TKBPAMD1p0

TKBPAFXS1p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	INTP20 can be used as a trigger. Note 1

TKBPAFXS1p2	Comparator trigger selection for forced output stop function 2
0	Comparator 3 can not be used as a trigger.
1	Comparator 3 can be used as a trigger. Note 2

TKBPAFXS1p1	Comparator trigger selection for forced output stop function 2
0	Comparator 2 can not be used as a trigger.
1	Comparator 2 can be used as a trigger. Note 3

TKBPAFXS1p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. Note 3

TKBPAFCM1p	Operation mode selection for forced output stop function 2
0	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period. Note 4
1	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger. Note 4

TKBPAHZS1p2	Comparator trigger selection for forced output stop function 1
0	Comparator 3 can not be used as a trigger.
1	Comparator 3 can be used as a trigger. Note 2

TKBPAHZS1p1	Comparator trigger selection for forced output stop function 1
0	Comparator 2 can not be used as a trigger.
1	Comparator 2 can be used as a trigger. Note 3

TKBPAHZS1p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. Note 3

Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) (2/2)

TKBPAHCM1p1	TKBPAHCM1p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT1p) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT1p) = 1" is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT1p) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT1p) = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT1p) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT1p) = 1 is written when the trigger signal is in its inactive period.

TKBPAMD1p1	TKBPAMD1p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Notes 1. When INTP20 is used as the forced output stop function 2, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

2. When CMP3 is used as the timer KB forced output stop function, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

3. When CMP0 or CMP2 is used as the timer KB forced output stop function, set CMPnSTEN = 1. For details, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

4. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).

Cautions 1. During timer operation, setting the other bits of the TKBPACTL1p register is prohibited. However, the TKBPACTL1p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

4. Figure7-75.Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p)(p.384~p.385)

Incorrect descriptions of forced output stop function control register 2p (TKBPACTL2p) are revised, and Note is added.

Old)

Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) (1/2)

Address: F06B0H (TKBPACTL20) , F06B2H (TKBPACTL21) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL2p	TKBPAFXS2p3	TKBPAFXS2p2	TKBPAFXS2p1	TKBPAFXS2p0	0	0	0	TKBPAFCM2p

7	6	5	4	3	2	1	0
0	TKBPAHZS2p2	TKBPAHZS2p1	TKBPAHZS2p0	TKBPAHCM2p1	TKBPAHCM2p0	TKBPAMD2p1	TKBPAMD2p0

TKBPAFXS2p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	**INTP20 can be used as a trigger.**

TKBPAFXS2p2	Comparator trigger selection for forced output stop function 2
0	Comparator 5 can not be used as a trigger.
1	**Comparator 5 can be used as a trigger.**

TKBPAFXS2p1	Comparator trigger selection for forced output stop function 2
0	Comparator 3 can not be used as a trigger.
1	**Comparator 3 can be used as a trigger.**

TKBPAFXS2p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAFCM2p	Operation mode selection for forced output stop function 2
0	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period.**
1	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.**

Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) (2/2)

TKBPAHZS2p2	Comparator trigger selection for forced output stop function 1
0	Comparator 5 can not be used as a trigger.
1	**Comparator 5 can be used as a trigger.**

TKBPAHZS2p1	Comparator trigger selection for forced output stop function 1
0	Comparator 4 can not be used as a trigger.
1	**Comparator 4 can be used as a trigger.**

TKBPAHZS2p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAHCM2p1	TKBPAHCM2p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT2)** = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT2)** = 1" is invalid. Forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT2)** = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT2)** = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT2)** = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT2)** = 1 is written when the trigger signal is in its inactive period.

TKBPAMD2p1	TKBPAMD2p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Cautions 1. During timer operation, setting the other bits of the TKBPACTL2p register is prohibited. However, the TKBPACTL2p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) (1/2)

Address: F06B0H (TKBPACTL20) , F06B2H (TKBPACTL21) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL2p	TKBPAFXS2p3	TKBPAFXS2p2	TKBPAFXS2p1	TKBPAFXS2p0	0	0	0	TKBPAFCM2p
	7	6	5	4	3	2	1	0
	0	TKBPAHZS2p2	TKBPAHZS2p1	TKBPAHZS2p0	TKBPAHCM2p1	TKBPAHCM2p0	TKBPAMD2p1	TKBPAMD2p0

TKBPAFXS2p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	INTP20 can be used as a trigger. Note 1

TKBPAFXS2p2	Comparator trigger selection for forced output stop function 2
0	Comparator 5 can not be used as a trigger.
1	Comparator 5 can be used as a trigger. Note 2

TKBPAFXS2p1	Comparator trigger selection for forced output stop function 2
0	Comparator 3 can not be used as a trigger.
1	Comparator 3 can be used as a trigger. Note 2

TKBPAFXS2p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. Note 3

TKBPAFCM2p	Operation mode selection for forced output stop function 2
0	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period. Note 4
1	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger. Note 4

TKBPAHZS2p2	Comparator trigger selection for forced output stop function 1
0	Comparator 5 can not be used as a trigger.
1	Comparator 5 can be used as a trigger. Note 2

TKBPAHZS2p1	Comparator trigger selection for forced output stop function 1
0	Comparator 4 can not be used as a trigger.
1	Comparator 4 can be used as a trigger. Note 2

TKBPAHZS2p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. Note 3

Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) (2/2)

TKBPAHCM2p1	TKBPAHCM2p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT2p) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT2p) = 1" is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT2p) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT2p) = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT2p) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT2p) = 1 is written when the trigger signal is in its inactive period.

TKBPAMD2p1	TKBPAMD2p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Notes 1. When INTP20 is used as the forced output stop function 2, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

2. When CMP4 or CMP5 is used as the timer KB forced output stop function, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

3. When CMP0 is used as the timer KB forced output stop function, set CMP0STEN = 1. For details, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

4. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).

Cautions 1. During timer operation, setting the other bits of the TKBPACTL2p register is prohibited. However, the TKBPACTL2p register can be refreshed (the same value is written).

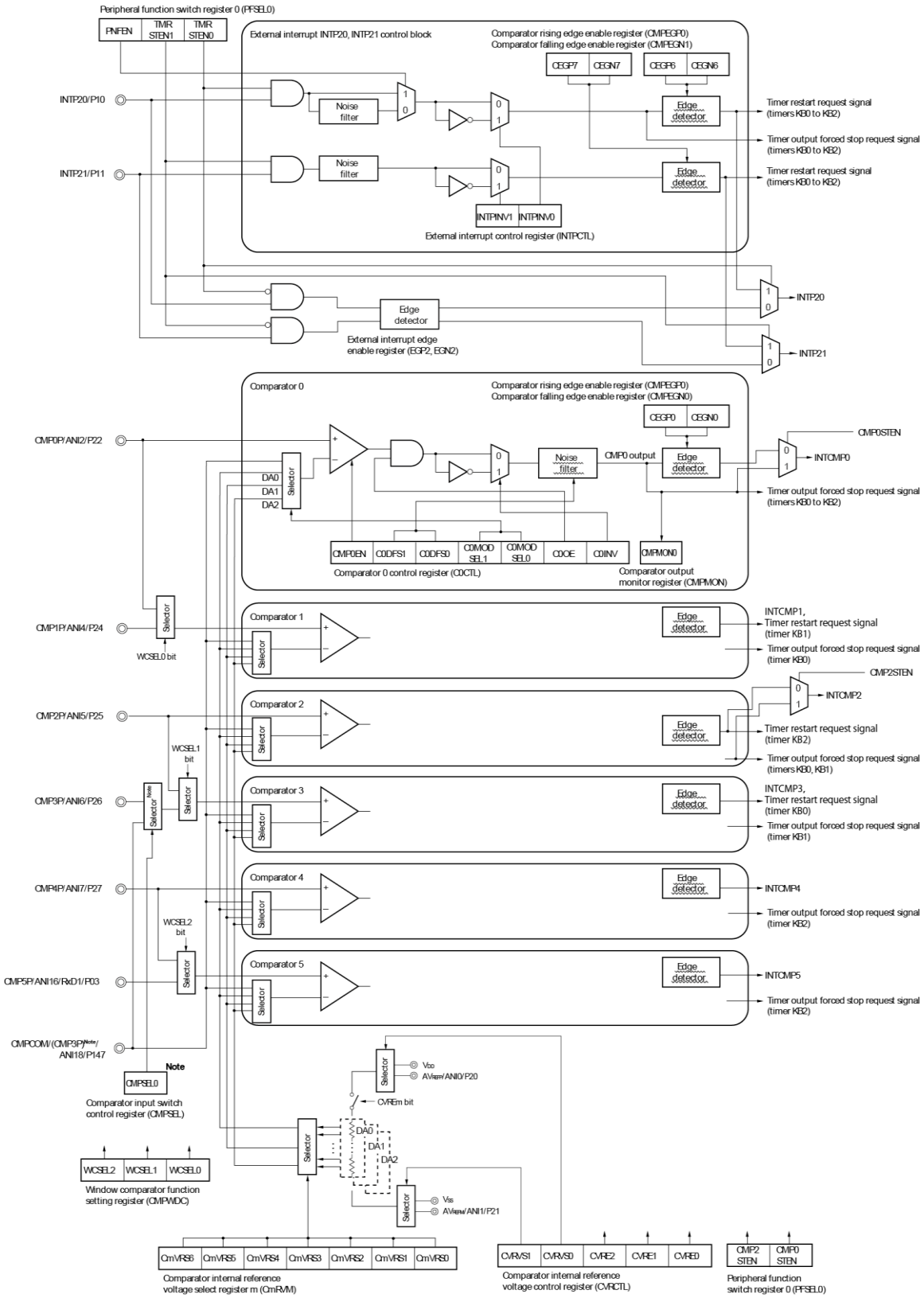
2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

5. Figure 14-1. Block Diagram of Comparator(p.527)

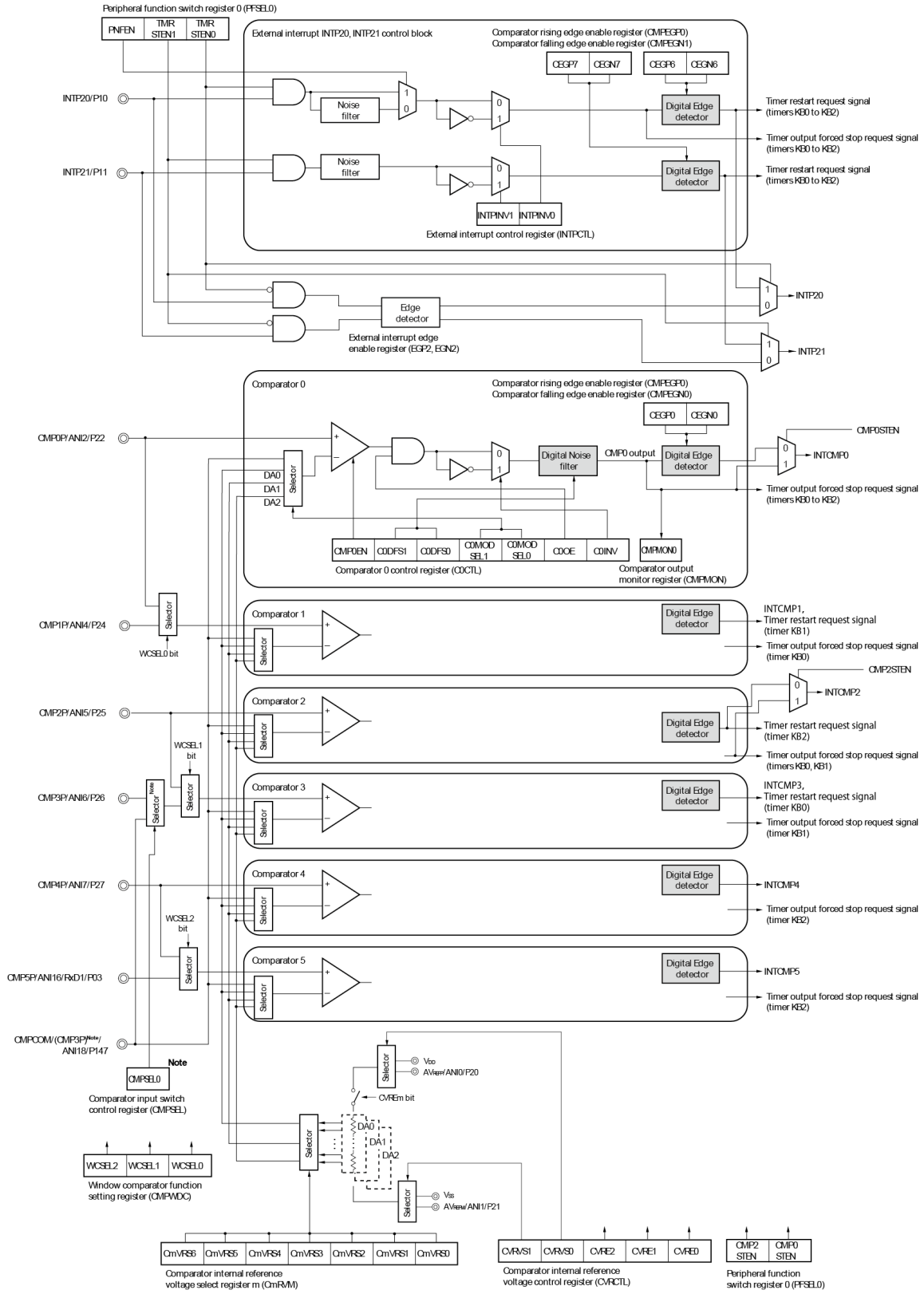
Incorrect names of the noise filter and the edge detection circuit in the block diagram are revised, and Note is added.

Old)



Note 20-pin products only. ANI16/CMP3P/P26 is selected by default for 30- and 38-pin products.

Remark m = 0 to 2



Note 20-pin products only. ANI16/CMP3P/P26 is selected by default for 30- and 38-pin products.

Caution When INTP20, INTP21, and comparator are used as the timer KB forced output stop function 2 or timer KB restart function, see 14. 5 Caution for Using Timer KB Simultaneous Operation Function.

Remark m = 0 to 2

6. Figure 14-12. Format of Peripheral Function Switch Register 0 (PFSEL0)(p.538)

Incorrect descriptions of the comparator and external interrupts are revised, and Notes are added.

Old)

Figure 14-12. Format of Peripheral Function Switch Register 0 (PFSEL0)

Address: F05C6H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0

CMP2STEN	Comparator 2 detection interrupt (INTCMP2) switching
0	STOP mode clear disabled
1	STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register)

CMP0STEN	Comparator 0 detection interrupt (INTCMP0) switching
0	STOP mode clear disabled
1	STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register)

PNFEN	Use/Do not use external interrupt INTP20 noise filter
0	Use noise filter
1	Do not use noise filter

TMRSTEN1	External interrupt INTP21 function select
0	External interrupt function (can be generated external interrupt, but cannot be used for timer restart function)
1	Timer restart function (cannot be generated external interrupt, and cannot release standby mode)

TMRSTEN0	External interrupt INTP20 function select
0	External interrupt function (can be generated external interrupt, but cannot be used for timer restart function)
1	Timer restart function (cannot be generated external interrupt, and cannot release standby mode)

Caution Comparator detection interrupt other than CMP0 and CMP2 cannot be used to clear the STOP mode.

Figure 14-12. Format of Peripheral Function Switch Register 0 (PFSEL0)

Address: F05C6H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0

CMP2STEN	Comparator 2 detection interrupt (INTCMP2) switching Note 1
0	Signal via digital edge detect circuit is selected. STOP mode release is disabled.
1	Forced output stop request signal is selected. STOP mode release is enabled, but only when not using noise filter. (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register)

CMP0STEN	Comparator 0 detection interrupt (INTCMP0) switching Note 1
0	Signal via digital edge detect circuit is selected. STOP mode release is disabled.
1	Forced output stop request signal is selected. STOP mode release is enabled, but only when not using noise filter. (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register)

PNFEN	Use/Do not use external interrupt INTP20 noise filter
0	Use noise filter
1	Do not use noise filter

TMRSTEN1	External interrupt INTP21 function switching Note 2
0	External interrupt function is selected. (STOP mode release is enabled, but cannot be used for timer restart function)
1	Timer restart function is selected. (STOP mode release is disabled, but can be used for timer restart function)

TMRSTEN0	External interrupt INTP20 function switching Note 2
0	External interrupt function is selected. (STOP mode release is enabled, but cannot be used for timer restart function)
1	Timer restart function/forced output stop function 2 is selected. (STOP mode release is disabled, but can be used for timer restart function)

Notes 1. When the interrupt for CMP0 and CMP2 is used, adopt a function used with the interrupt input signal.
When the CMP0 and CMP2 are used as a trigger of the timer KB forced output stop function, set CMPnSTEN = 1.
When the CMP2 is used as a trigger of the timer restart function for timer KB, set CMP2STEN = 0.
For details, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

2. When INTP20 and INTP21 are used as a trigger of the timer KB forced output stop function 2 or timer restart function, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

Caution Comparator detection interrupt other than CMP0 and CMP2 cannot be used to clear the STOP mode.

Remark n = 0, 2

7. 14. 5 Caution for Using Timer KB Simultaneous Operation Function

As respects of INTP2m and comparator, Caution for Using Timer KB Simultaneous Operation Function is added.

Old)

No applicable item

New)

14. 5 Caution for Using Timer KB Simultaneous Operation Function

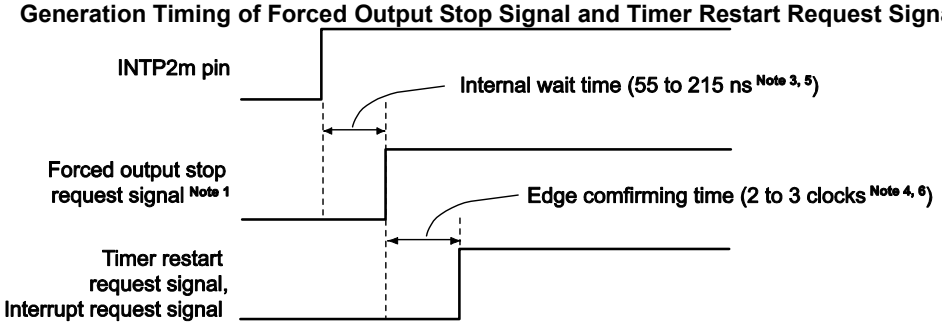
In addition to their use as an external interrupt input, the INTP2m pin output and the comparator output signal can be used as a trigger for functions that operate simultaneously with timer KB, such as the forced output stop function and timer restart function. The settings in peripheral function switch register 0 (PFSEL0) and the edge selection registers must be specified according to the function used. The width of the active signal required until each function starts operating differs.

When using INTP2m or the comparator output signal, refer to Tables 14-4 to 14-6 to specify the necessary register settings, and configure external circuits so that the required active signal width is assured.

Table 14-4. Relationship of INTP2m function, register settings, and active signal width

Function	Peripheral enable register setting	Edge setting registers	Necessary active signal width to operate each function		
			Interrupt	Forced output stop	Timer restart
External interrupt (STOP release is enabled)	TMRSTENm = 0	EGPn, EGNn	To 1 μs	-	-
Forced output stop Note 1	TMRSTENm = 1	CEGPp, CEGNp Note 2	55 to 215 ns Note 3 + 2 to 3 clocks Note 4	55 to 215 ns Note 3, 5	-
Timer restart	TMRSTENm = 1	CEGPp, CEGNp	55 to 215 ns Note 3 + 2 to 3 clocks Note 4	-	55 to 215 ns Note 3 + 2 to 3 clocks Note 4, 6

Figure 14-18. Generation Timing of Forced Output Stop Signal and Timer Restart Request Signal by INTP2m



Notes 1. Only INTP20 can be used as a trigger for forced output stop function 2.

2. The active level of INTP20 (used for forced output stop function 2) is high. Edge selection is only applied to detection of an interrupt signal.

3. 5 to 15 ns when noise filtering on INTP20 is disabled (PNFEN = 1)

4. For f_{CLK} or f_{PLL} (when PLLON = 1)

5. An additional output delay time (10 to 40 ns) is required from when forced output stop function 2 starts operating to when the level of the timer KB output changes.

Notes 6. Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.

Remark m = 0, 1 n = 20, 21 p = 7, 6

Table 14-5. Relationship of comparator 0 and 2 functions, register settings, and active signal width

Function	Peripheral enable register setting	Edge setting registers	Necessary active signal width to operate each function		
			Interrupt	Forced output stop	Timer restart
External interrupt (STOP release is enabled Note 1)	CMPnSTEN = 1	Rising edge only Note 2	To 150 ns Note 3	-	-
External interrupt (STOP release is disabled)	CMPnSTEN = 0	CEGPn, CEGNn	To 150 ns Note 3 + 2 to 3 clocks Note 4, 5	-	-
Forced output stop	CMPnSTEN = 1	**Note 6**	To 150 ns Note 3	To 150 ns Note 3, 7	-
Timer restart	CMPnSTEN = 0	CEGPn, CEGNn	To 150 ns Note 3 + 2 to 3 clocks Note 4, 5	-	To 150 ns Note 3 + 2 to 3 clocks Note 4, 5

Figure 14-19. Generation Timing of Forced Output Stop Request Signal by Comparator 0 and 2 (CMPnSTEN = 1)

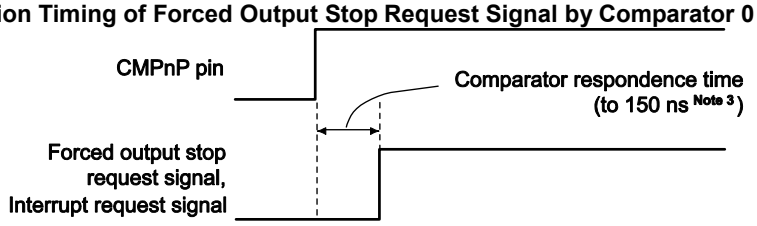
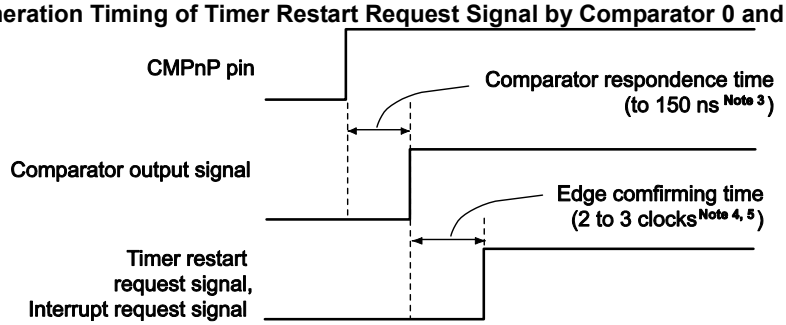


Figure 14-20. Generation Timing of Timer Restart Request Signal by Comparator 0 and 2 (CMPnSTEN = 0)



Notes 1. When noise filtering is set to "0, 0" by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL)

2. To change the level of the edge direction, invert the comparator output signal by using the CnINV bit in the comparator n control register (CnCTL).

3. This is the time required when noise filtering is set to "0, 0" by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL).
If a setting other than "0, 0" is specified, the specified noise elimination width is added.

4. For f_{CLK} or f_{PLL} (when PLLON = 1)

Notes 5. Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.

6. The active level of INTP20 (used for forced output stop function 2) is high.

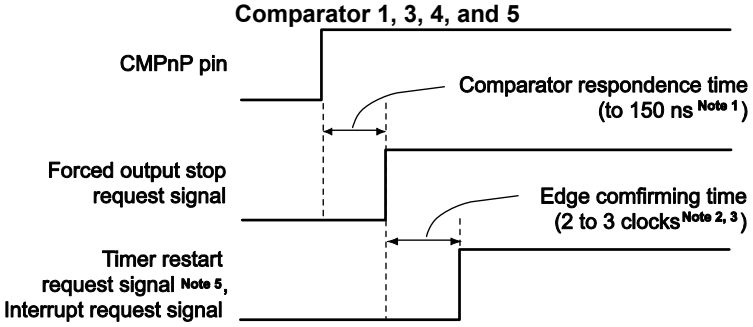
7. An additional output delay time (10 to 40 ns) is required from when forced output stop function 2 starts operating to when the level of the timer KB output changes.

Remark n = 0, 2

Table 14-6. Relationship of comparator 1, 3, 4, and 5 functions, register settings, and active signal width

Function	Peripheral enable register setting	Edge setting registers	Necessary active signal width to operate each function		
			Interrupt	Forced output stop	Timer restart
External interrupt (STOP release is disabled)	-	CEGPn, CEGNn	To 150 ns Note 1 + 2 to 3 clocks Note 2, 3	-	-
Forced output stop	-	**Note 4**	To 150 ns Note 2 + 2 to 3 clocks Note 3, 4	To 150 ns Note 2, 5	-
Timer restart Note 6	-	CEGPn, CEGNn	To 150 ns Note 2 + 2 to 3 clocks Note 3, 4	-	To 150 ns Note 2 + 2 to 3 clocks Note 3, 4

Figure 14-21. Generation Timing of Forced Output Stop Request Signal and Timer Restart Request Signal by Comparator 1, 3, 4, and 5



Notes 1. When noise filtering is set to "0, 0" by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL). If a setting other than "0, 0" is specified, the specified noise elimination width is added.

2. For f_{CLK} or f_{PLL} (when PLLON = 1)

3. Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.

4. The active level of INTP20 (used for forced output stop function 2) is high.

5. An additional output delay time (10 to 40 ns) is required from when forced output stop function 2 starts operating to when the level of the timer KB output changes.

6. The timer restart function can be used for comparator 1 and 3 only .

Remark n = 1, 3 to 5

8. Timing Chart of SNOOZE Mode Operation (p.666, 667, 669)

The content of No.8 will be corrected at No.69, 70 and 71. Please see the renewed content.

9. Table 20-1. Interrupt Source List (2/3)(p.898)

Note for the interrupt source list is added.

Old):

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 40 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 20-1.

3. INTCMP1, INTCMP3, INTCMP4, and INTCMP5 cannot be used to clear the STOP mode.

New):

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 40 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 20-1.

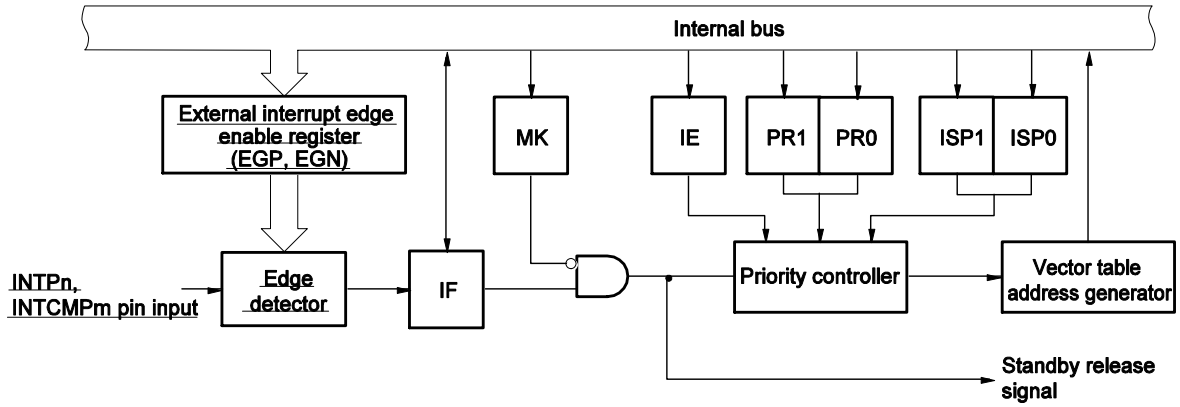
3. INTCMP1, INTCMP3, INTCMP4, and INTCMP5 cannot be used to clear the STOP mode.
About interrupt generation timing, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

10. Figure 20-1. Basic Configuration of Interrupt Function(p.900)

Incorrect the basic configuration of interrupt function is revised.

Old)

(B) External maskable interrupt (INTPn, INTCMPm)

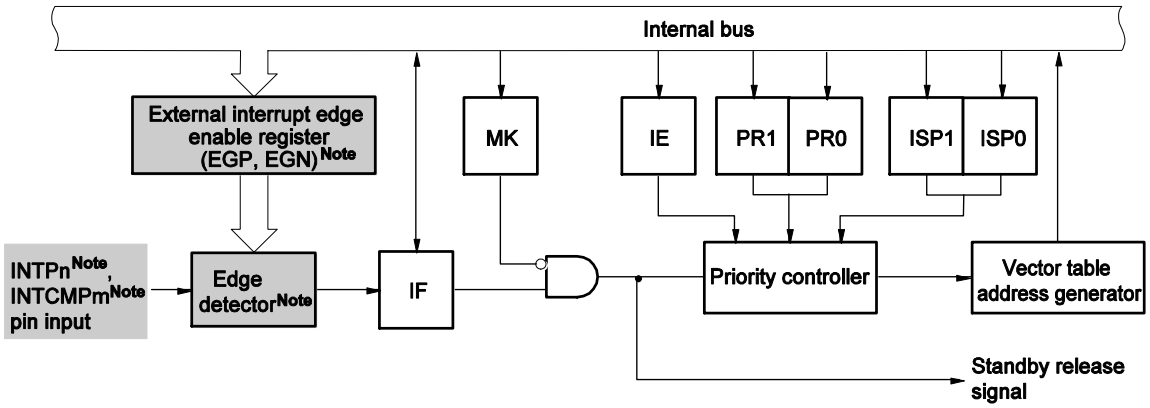


IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

Remark 20-pin: n = 0, 20, 21, 22, m = 0 to 3
30-pin: n = 0, 4, 11, 20 to 23, m = 0 to 5
38-pin: n = 0, 3, 4, 9 to 11, 20 to 23, m = 0 to 5

New)

(B) External maskable interrupt (INTPn[Note], INTCMPm[Note])



Note According to setting for using of the timer KB simultaneous function (the timer KB forced output stop function and timer restart function), the interrupt signal pass and the interrupt generation timing and the edge enable register for INTP20 and INTP21 and INTCMPm vary. For details, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

Remark 20-pin: n = 0, 20, 21, 22, m = 0 to 3
30-pin: n = 0, 4, 11, 20 to 23, m = 0 to 5
38-pin: n = 0, 3, 4, 9 to 11, 20 to 23, m = 0 to 5

11. Table 21-1. Operating Statuses in HALT Mode (2/2)(p.931)

Incorrect description about the comparator operation in HALT mode is revised.

Old)

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock	
			When CPU Is Operating on XT1 Clock (f_{XT})	When CPU Is Operating on External Subsystem Clock (f_{EXS})
System clock			Clock supply to the CPU is stopped	
	Main system clock	f_{IH}	Operation disabled	
		f_X		
		f_{EX}		
	Subsystem clock	f_{XT}	Operation continues (cannot be stopped)	Cannot operate
		f_{EXS}	Cannot operate	Operation continues (cannot be stopped)
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops	
CPU			Operation stopped	
Code flash memory				
Data flash memory				
RAM				
Port (latch)			Status before HALT mode was set is retained	
Timer array unit			Operable when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).	
Timer KB0 to KB2				
Timer KC0				
Real-time clock (RTC)			Operable	
12-bit interval timer				
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**	
A/D converter			Operation disabled	
Programmable gain amplifier			Operable (However, this is not used, since the operation has been disabled for the A/D converter that is the destination for input of the PGA output signal)	
Comparator			Operable (When in the low-consumption RTC mode (RTCLPC = 1 in the OSMC register), this can be used only when the STOP mode cancel is set (CMPnSTEN = 1 in the PFSEL0 register) by the comparator interrupt detection and the noise filter is not used (n = 0, 2))	

(Omitted)

New)

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock	
			When CPU Is Operating on XT1 Clock (f_{XT})	When CPU Is Operating on External Subsystem Clock (f_{EXS})
System clock			Clock supply to the CPU is stopped	
	Main system clock	f_{IH}	Operation disabled	
		f_X		
		f_{EX}		
	Subsystem clock	f_{XT}	Operation continues (cannot be stopped)	Cannot operate
		f_{EXS}	Cannot operate	Operation continues (cannot be stopped)
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops	
CPU			Operation stopped	
Code flash memory				
Data flash memory				
RAM				
Port (latch)			Status before HALT mode was set is retained	
Timer array unit			Operable when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).	
Timer KB0 to KB2				
Timer KC0				
Real-time clock (RTC)			Operable	
12-bit interval timer				
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**	
A/D converter			Operation disabled	
Programmable gain amplifier			Operable (However, this is not used, since the operation has been disabled for the A/D converter that is the destination for input of the PGA output signal)	
Comparator			Only CMP0 and CMP2 are operable. (When in the low-consumption RTC mode (RTCLPC = 1 in the OSMC register), CMPn can be used only when the STOP mode cancel is set (CMPnSTEN = 1 in the PFSEL0 register) by the comparator interrupt detection and the noise filter is not used. (n = 0, 2))	

(Omitted)

12. Table 21-2. Operating Statuses in STOP Mode(p.936)

Incorrect description about the comparator operation in STOP mode is revised.

Old)

STOP Mode Setting / Item			When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{IH}	Stopped		
		f_X			
		f_{EX}			
	Subsystem clock	f_{XT}	Status before STOP mode was set is retained		
		f_{EXS}			
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops		
CPU			Operation stopped		
Code flash memory					
Data flash memory					
RAM					
Port (latch)			Status before STOP mode was set is retained		
Timer array unit			Operation disabled		
Timer KB0 to KB2					
Timer KC0					
Real-time clock (RTC)			Operable		
12-bit interval timer					
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**		
A/D converter			Wakeup operation is enabled (switching to the SNOOZE mode)		
Programmable gain amplifier			Operable		
Comparator			Operable (Only for channels set to enable cancellation of STOP mode and when digital filter is not used)		

(Omitted)

New)

STOP Mode Setting / Item			When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{IH}	Stopped		
		f_X			
		f_{EX}			
	Subsystem clock	f_{XT}	Status before STOP mode was set is retained		
		f_{EXS}			
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops		
CPU			Operation stopped		
Code flash memory					
Data flash memory					
RAM					
Port (latch)			Status before STOP mode was set is retained		
Timer array unit			Operation disabled		
Timer KB0 to KB2					
Timer KC0					
Real-time clock (RTC)			Operable		
12-bit interval timer					
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**		
A/D converter			Wakeup operation is enabled (switching to the SNOOZE mode)		
Programmable gain amplifier			Operable		
Comparator			Only CMP0 and CMP2 are operable when the STOP mode cancel is set (CMPnSTEN = 1 in the PFSEL0 register) by the comparator interrupt detection and the noise filter is not used. (n = 0, 2)		

(Omitted)

13. Table 21-3. Operating Statuses in SNOOZE Mode(p.942)

Incorrect description about the comparator operation in SNOOZE mode is revised.

Old)

Item \ STOP Mode Setting			When Inputting CSI00/UART0 Data Reception Signal or A/D Converter Timer Trigger Signal While in STOP Mode
			When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})
System clock			Clock supply to the CPU is stopped
	Main system clock	f_{IH}	Operation started
		f_X	Stopped
		f_{EX}	
	Subsystem clock	f_{XT}	Use of the status while in the STOP mode continues
		f_{EXS}	
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops
CPU			Operation stopped
Code flash memory			
Data flash memory			
RAM			
Port (latch)			Use of the status while in the STOP mode continues
Timer array unit			Operation disabled
Timer KB0 to KB2			
Timer KC0			
Real-time clock (RTC)			Operable
12-bit interval timer			
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**
A/D converter			Operable
Programmable gain amplifier			Operable
Comparator			Operable (Only for channels set to enable cancellation of STOP mode and when digital filter is not used)

(Omitted)

New)

Item \ STOP Mode Setting			When Inputting CSI00/UART0 Data Reception Signal or A/D Converter Timer Trigger Signal While in STOP Mode
			When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})
System clock			Clock supply to the CPU is stopped
	Main system clock	f_{IH}	Operation started
		f_X	Stopped
		f_{EX}	
	Subsystem clock	f_{XT}	Use of the status while in the STOP mode continues
		f_{EXS}	
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops
CPU			Operation stopped
Code flash memory			
Data flash memory			
RAM			
Port (latch)			Use of the status while in the STOP mode continues
Timer array unit			Operation disabled
Timer KB0 to KB2			
Timer KC0			
Real-time clock (RTC)			Operable
12-bit interval timer			
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**
A/D converter			Operable
Programmable gain amplifier			Operable
Comparator			Only CMP0 and CMP2 are operable when the STOP mode cancel is set (CMPnSTEN = 1 in the PFSEL0 register) by the comparator interrupt detection and the noise filter is not used. (n = 0, 2)

(Omitted)

14. 32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics(p.1100)

Descriptions of the data memory STOP mode low supply voltage data retention characteristics are added.

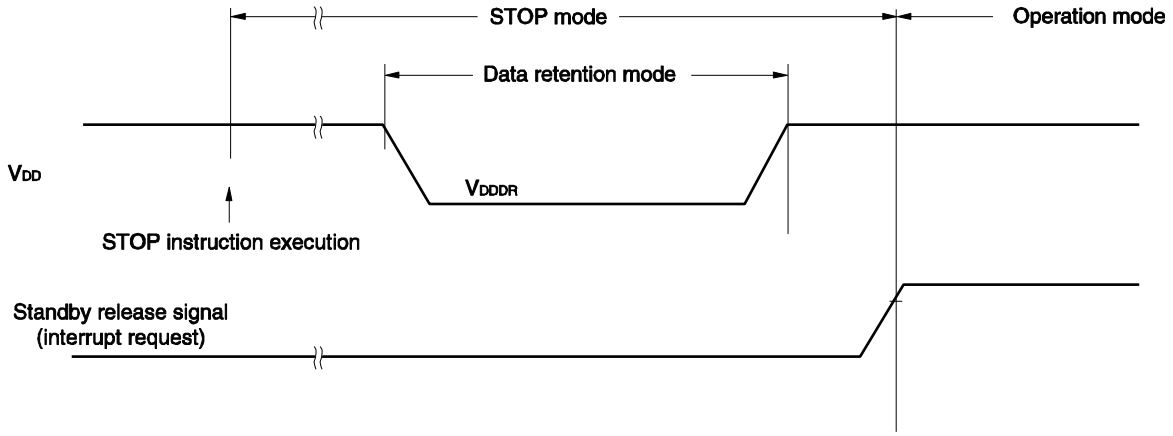
Old)

32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



New)

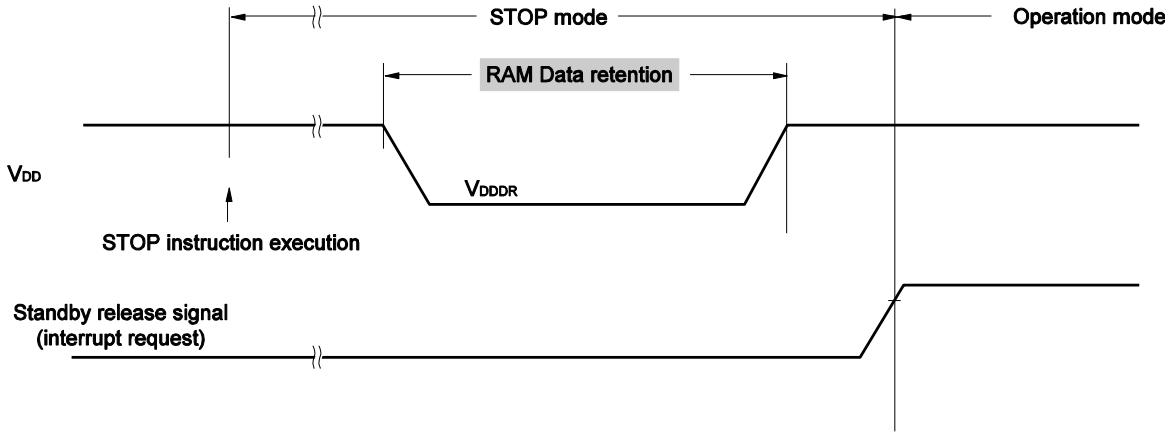
32.7 RAM Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Caution When CPU is operated at the voltage of out of the operation voltage range, RAM data is not retained. Therefore, set STOP mode before the supplied voltage is below the operation voltage range.



15. 33.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics(p.1142)

Descriptions of the data memory STOP mode low supply voltage data retention characteristics are added.

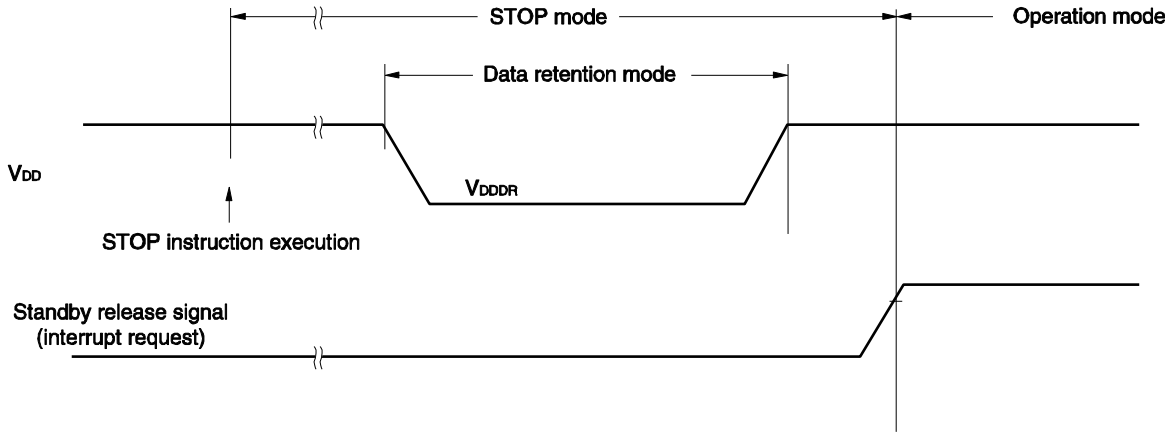
Old)

33.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +125°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



New)

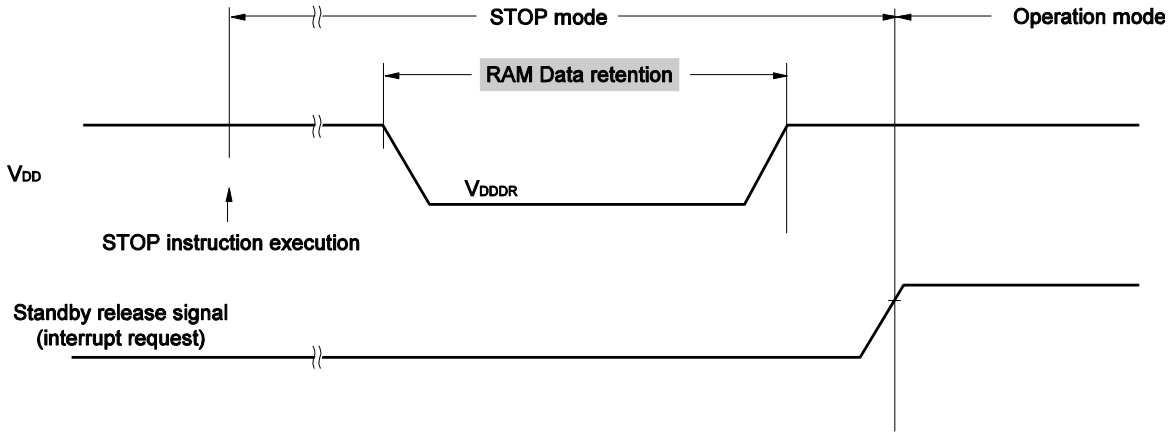
33.7 RAM Data Retention Characteristics

(T_A = –40 to +125°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Caution When CPU is operated at the voltage of out of the operation voltage range, RAM data is not retained. Therefore, set STOP mode before the supplied voltage is below the operation voltage range.

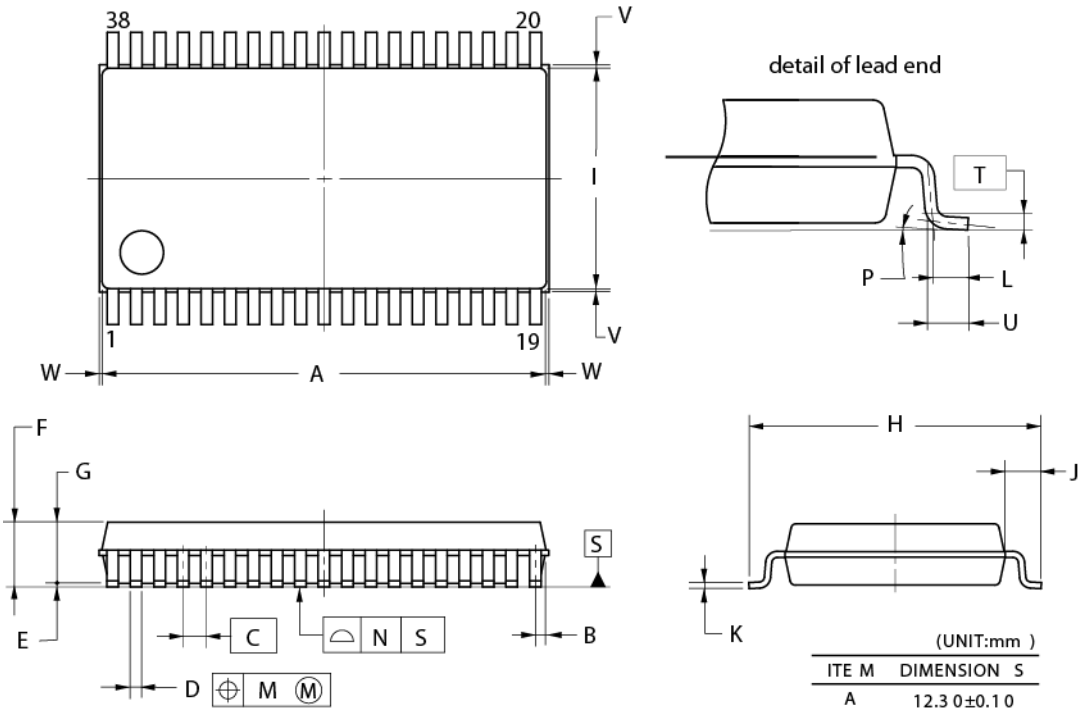


16. 34.3 38-pin Products(p.1147)

Incorrect descriptions of the package code and dimensions are revised.

Old)

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-SSOP38-6.1x12.3-0.65	PRSP0038JA-B	P38MC-65-GAA-2	0.3



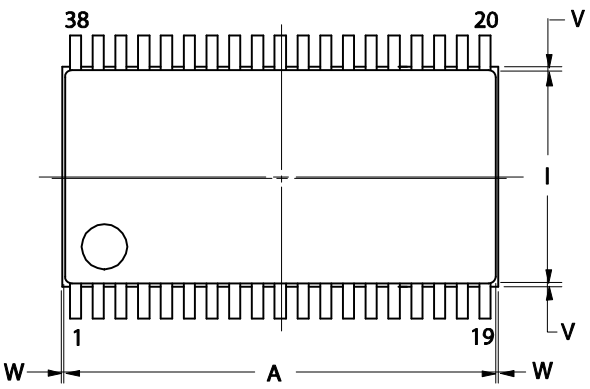
NOT E

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition .

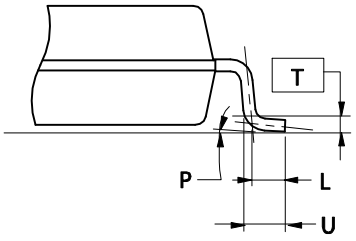
(UNIT:mm)

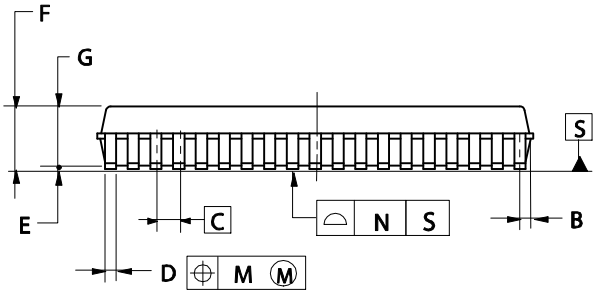
ITE M	DIMENSION S
A	12.30±0.10
B	0.30
C	0.65 (T.P.)
D	$0.30^{+0.10}_{-0.05}$
E	0.125±0.075
F	2.00 MAX .
G	1.70±0.10
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.10}_{-0.05}$
L	0.50
M	0.10
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX .
W	0.15 MAX .

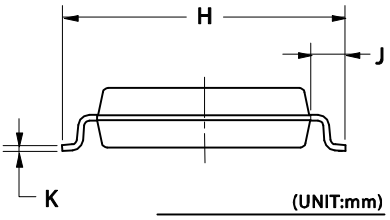
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-SSOP38-0300-0.65	PRSP0038JA-A	P38MC-65-2A4-2	0.3



detail of lead end







NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

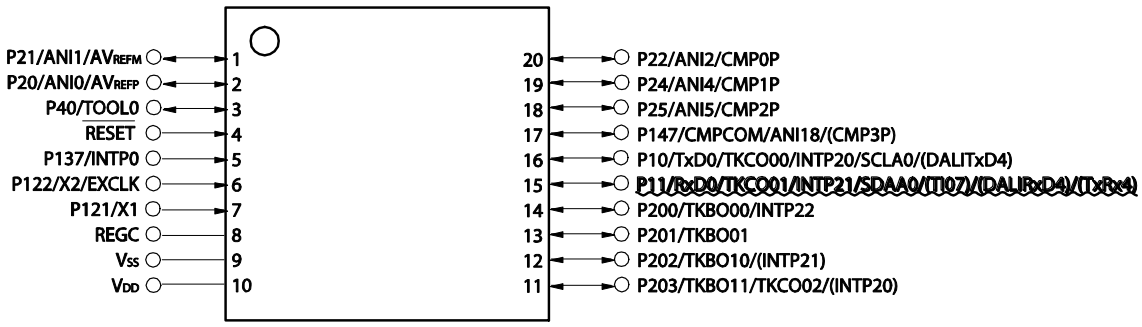
(UNIT:mm)

ITEM	DIMENSIONS
A	12.30±0.10
B	0.30
C	0.65 (T.P.)
D	0.32 +0.08 -0.07
E	0.125±0.075
F	2.00 MAX.
G	1.70±0.10
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	0.17 +0.08 -0.07
L	0.50
M	0.10
N	0.10
P	3° +7° -3°
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

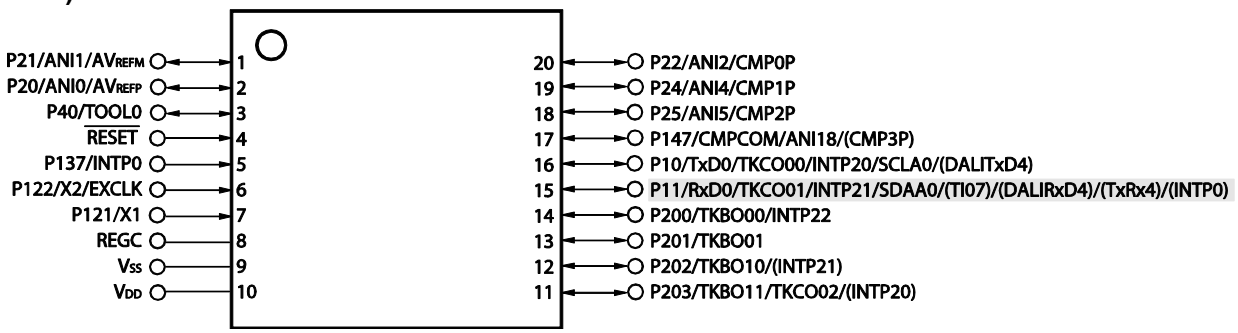
17. 1.3.1 20-pin products(p.4)

Incorrect alternate-function pin is revised.

Old)



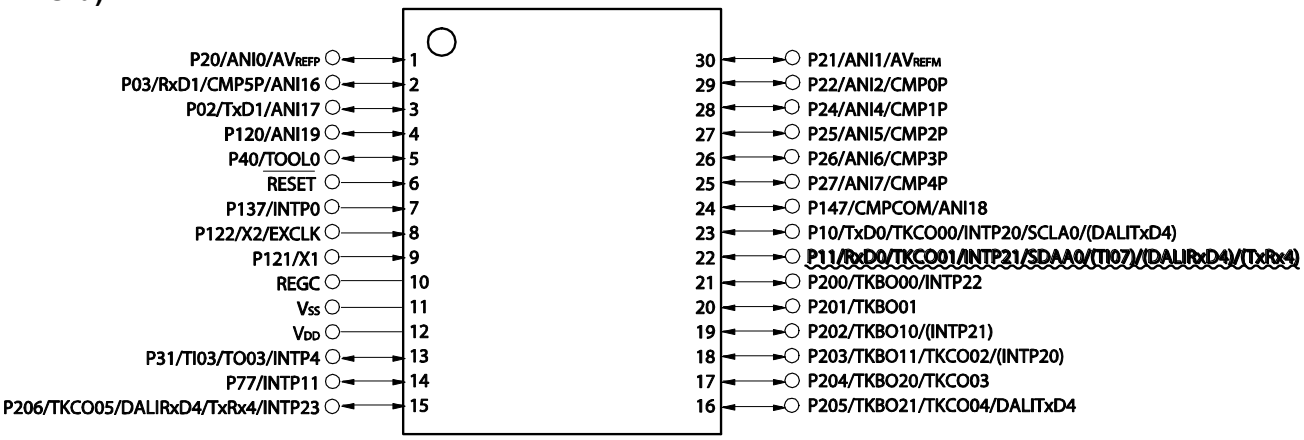
New)



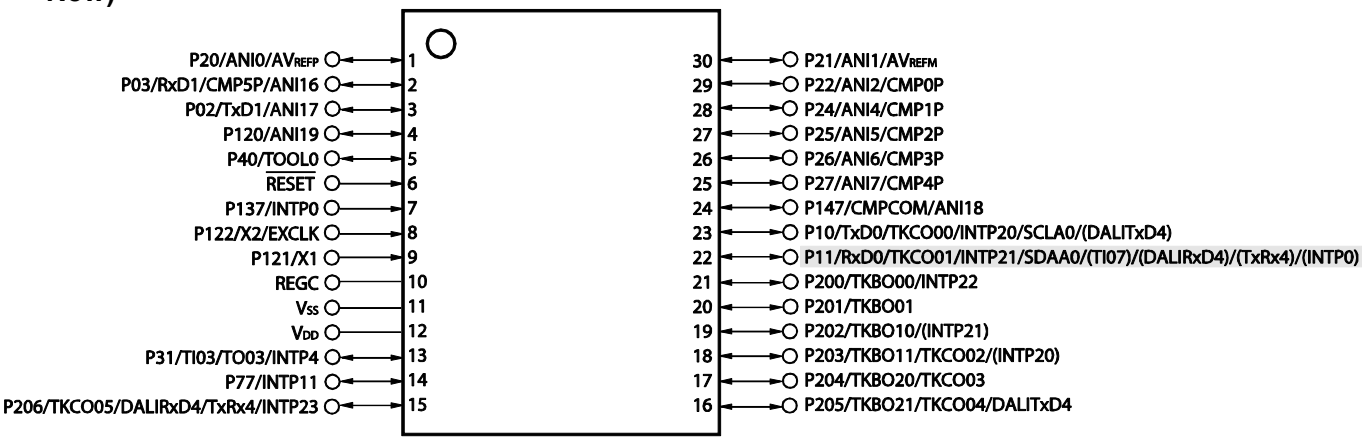
18. 1.3.2 30-pin products(p.5)

Incorrect alternate-function pin is revised.

Old)



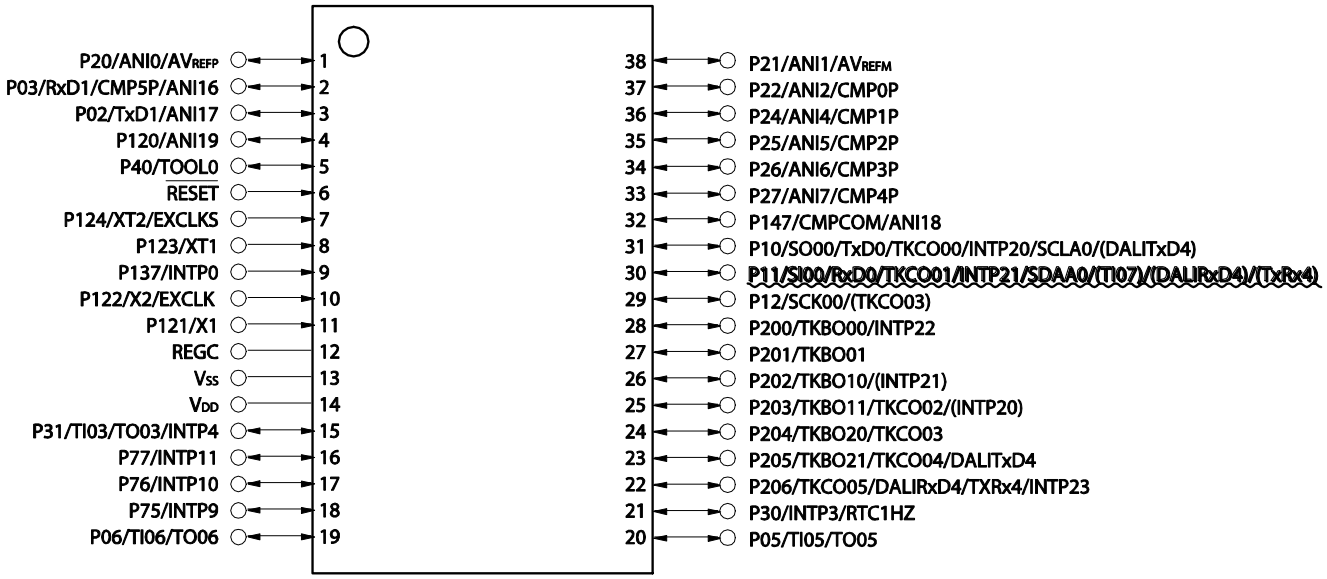
New)



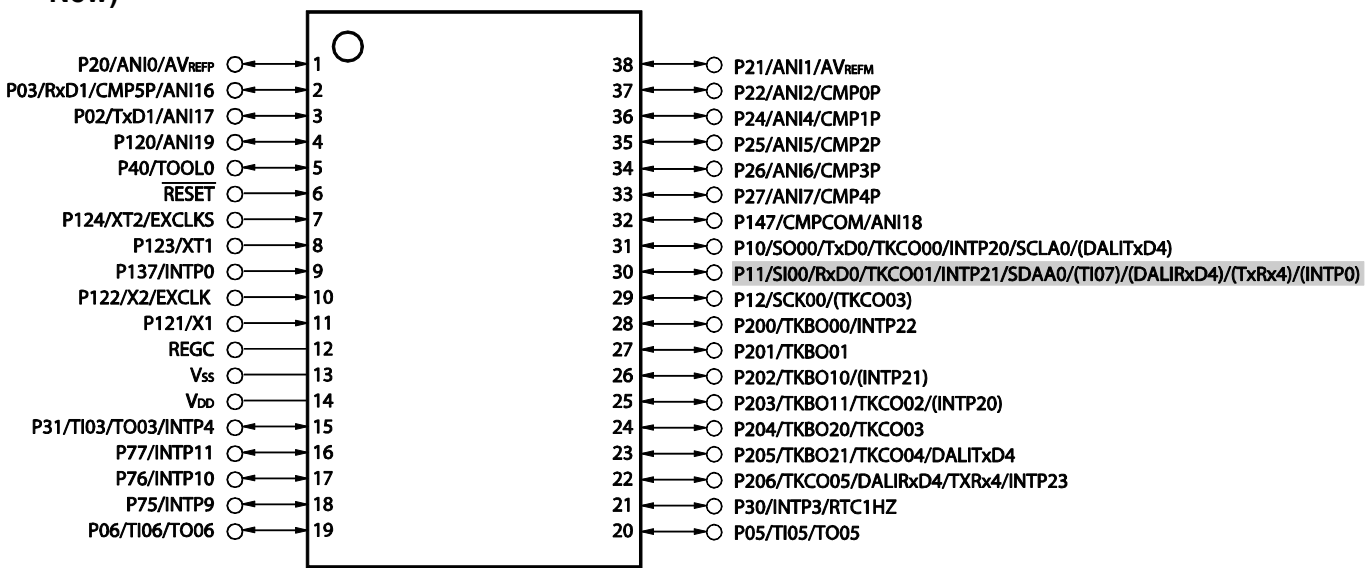
19. 1.3.3 38-pin products(p.6)

Incorrect alternate-function pin is revised.

Old)



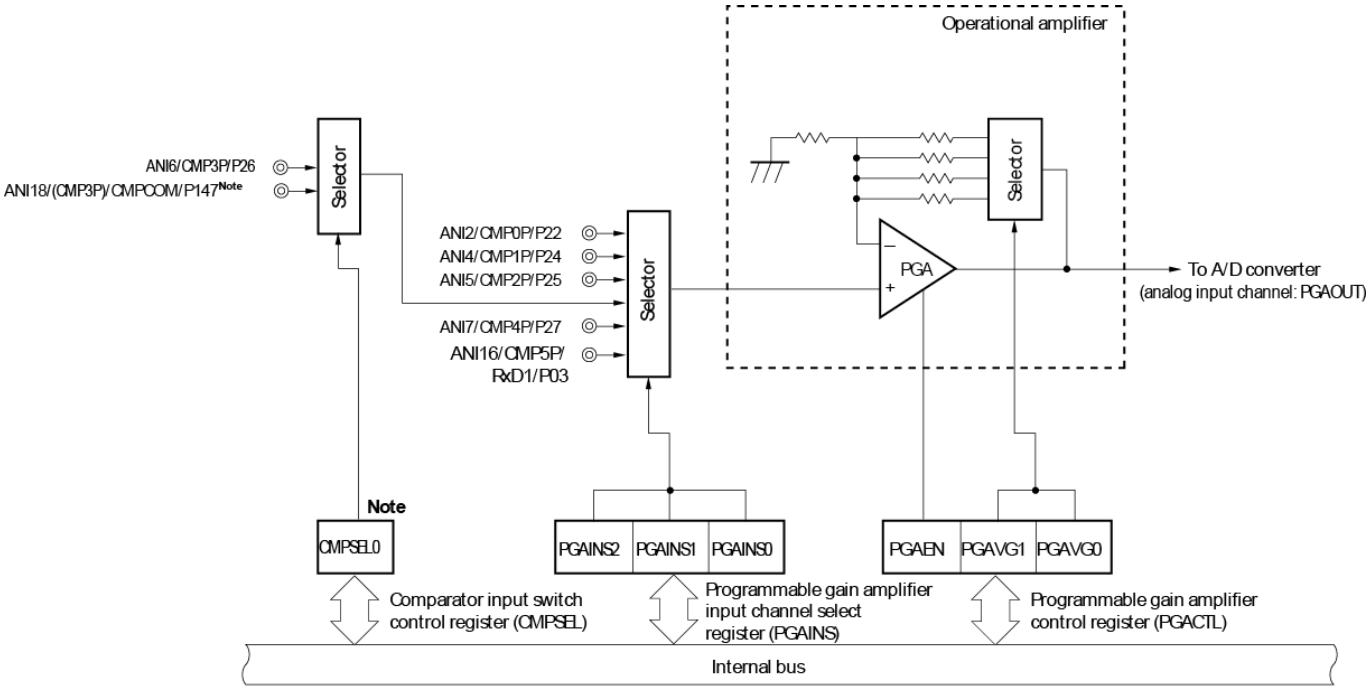
New)



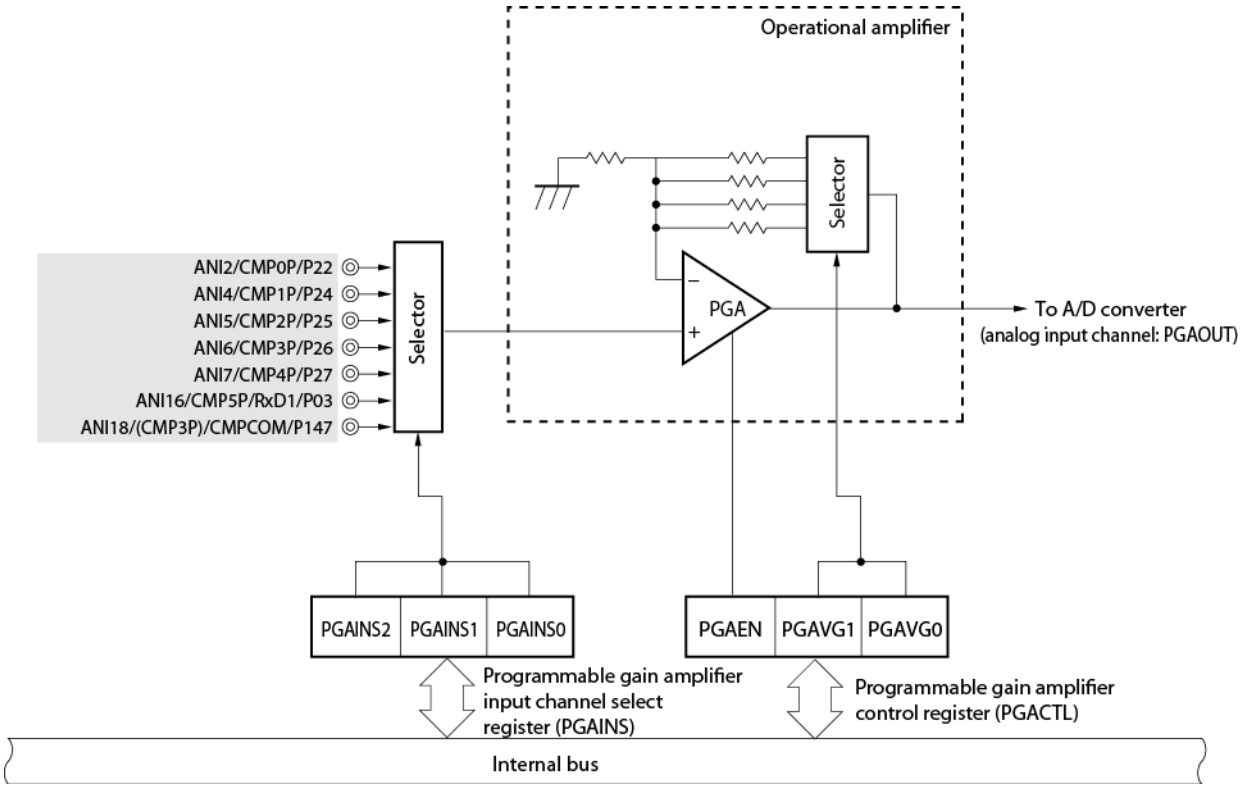
20. Figure 13-1. Block Diagram of Operational Amplifier(p.516)

Incorrect block diagram is revised.

Old)



New)



21. 13.3.3 Programmable gain amplifier input channel select register (PGAINS)(p.519)

Incorrect description of programmable gain amplifier input channel select register (PGAINS) is revised.

Old)

Figure 13-4. Format of Programmable Gain Amplifier Input Channel Select Register (PGAINS)

Address: F0551H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PGAINS	0	0	0	0	0	PGAINS2	PGAINS1	PGAINS0

PGAINS2	PGAINS1	PGAINS0	Analog input channel for input to programmable gain amplifier
0	0	0	ANI2/CMP0P
0	0	1	ANI4/CMP1P
0	1	0	ANI5/CMP2P
0	1	1	ANI6/CMP3P **or ANI18/(CMP3P)**Note
1	0	0	ANI7/CMP4P
1	0	1	ANI16/CMP5P
Other than above			Setting prohibited

Note Selected by the comparator input switch control register (CMPSEL) (20-pin products only)

Caution Set the PGAINS register during stop operation of the programmable gain amplifier (PGAEN = 0).

New)

Figure 13-4. Format of Programmable Gain Amplifier Input Channel Select Register (PGAINS)

Address: F0551H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PGAINS	0	0	0	0	0	PGAINS2	PGAINS1	PGAINS0

PGAINS2	PGAINS1	PGAINS0	Analog input channel for input to programmable gain amplifier
0	0	0	ANI2/CMP0P
0	0	1	ANI4/CMP1P
0	1	0	ANI5/CMP2P
0	1	1	ANI6/CMP3P
1	0	0	ANI7/CMP4P
1	0	1	ANI16/CMP5P
1	1	0	ANI18/CMPCOM/(CMP3P Note)
Other than above			Setting prohibited

Note Selected by the comparator input switch control register (CMPSEL) (20-pin products only)

Caution Set the PGAINS register during stop operation of the programmable gain amplifier (PGAEN = 0).

22. Precaution regarding the use of REAL-TIME CLOCK(p.427)

RWAIT bit is bit 0 of Real-time Clock Control Register 1 (RTCC1).
For the description of RWAIT bit, it'll add the following Note1 and Note2, because after setting to RWAIT = 1, the time required to until RWST = 1 might be longer than one clock time of the operation clock (f_{RTC}).

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
This bit controls the operation of the counter. Be sure to write "1" to it to read or write the counter value. As the internal counter (16 bits) is continuing to run, complete reading or writing within one second and turn back to 0. When RWAIT = 1, it takes up to 1 operating clock (f_{RTC}) until the counter value can be read or written (RWST = 1). Notes1,2 When the internal counter (16 bits) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up. However, when it wrote a value to second count register, it will not keep the overflow event.	

Note1. When setting RWAIT=1 during 1 operating clock (f_{RTC}), after setting RTCE=1, it may take two clock time of the operation clock (f_{RTC}), until RWST bit is set to "1".

Note2. When setting RWAIT=1 during 1 operating clock (f_{RTC}), after returning from a stand-by (HALT mode, STOP mode and SNOOZE mode), it may take two clock time of the operation clock (f_{RTC}), until RWST bit is set to "1".

23. 2.4 Block Diagrams of Pins

NEW)

2.4 Block Diagrams of Pins

Figures 2-1 to 2-12 show the block diagrams of the pins described in **2.1.1 20-pin products** to **2.1.3 38-pin products**.

Figure 2-1. Pin Block Diagram for Pin Type 2-1-1

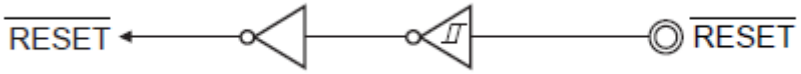
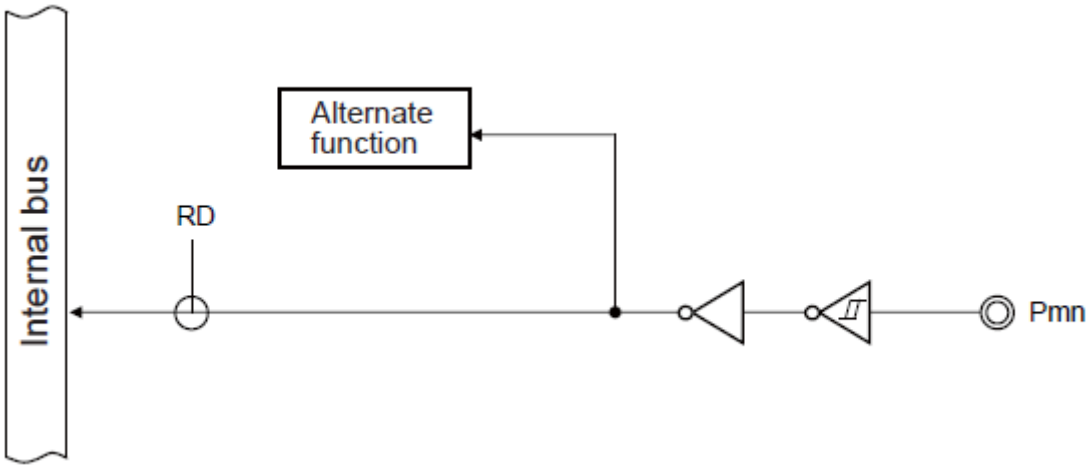
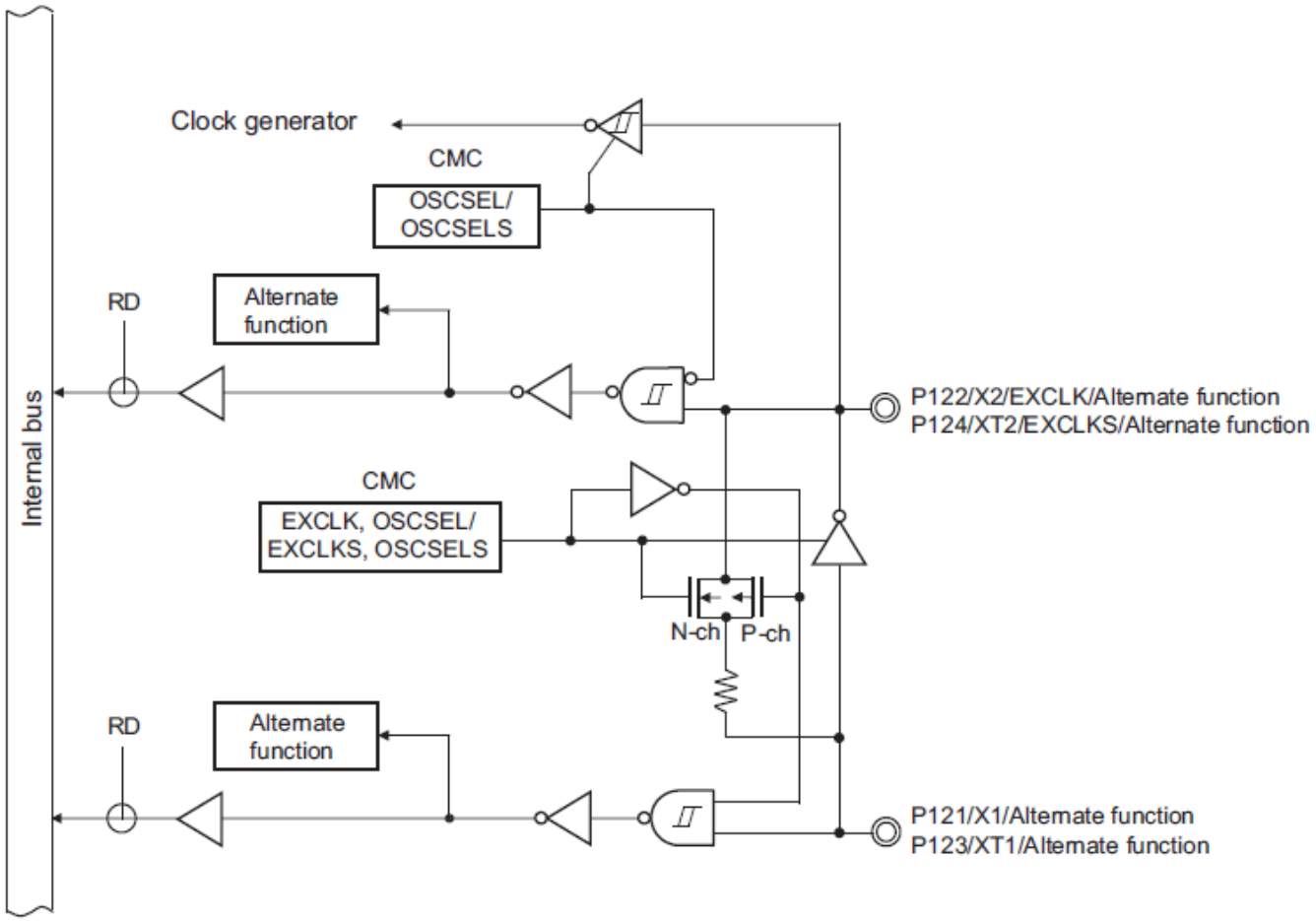


Figure 2-2. Pin Block Diagram for Pin Type 2-1-2



Remark For alternate functions, see **2.1 Port Function**.

Figure 2-3. Pin Block Diagram for Pin Type 2-2-1



Remark For alternate functions, see **2.1 Port Function**.

Figure 2-4. Pin Block Diagram for Pin Type 4-3-1

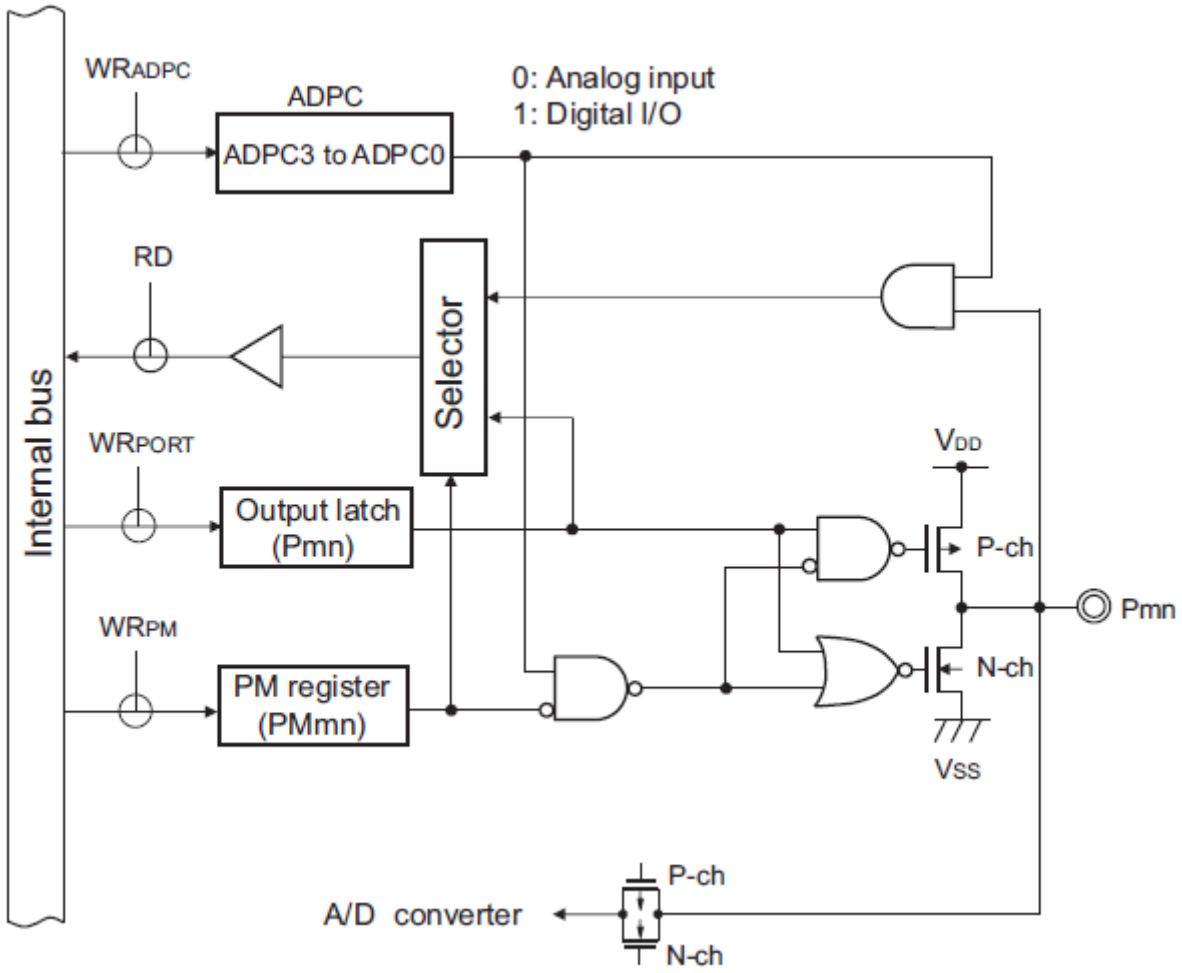


Figure 2-5. Pin Block Diagram for Pin Type 4-18-1

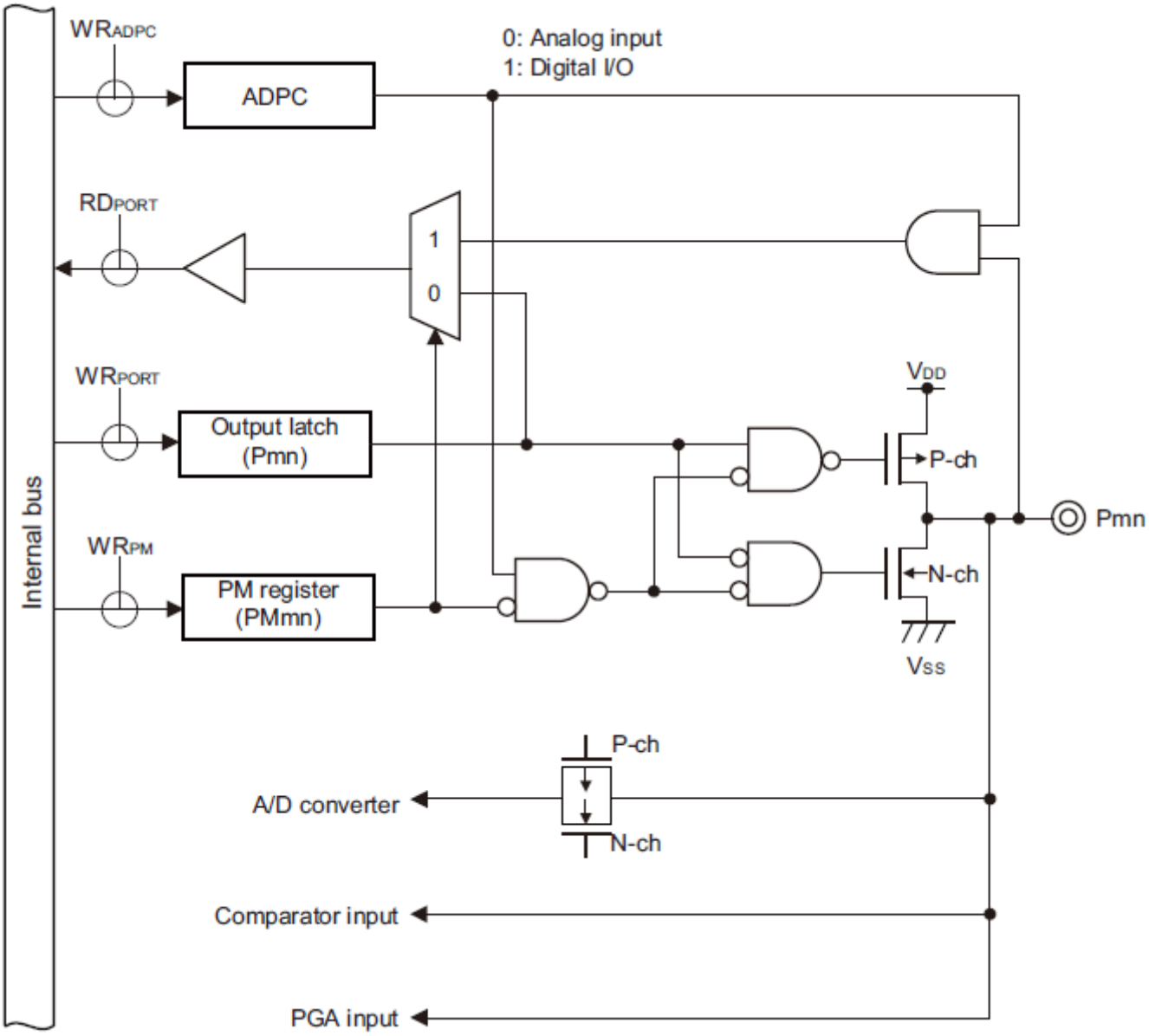
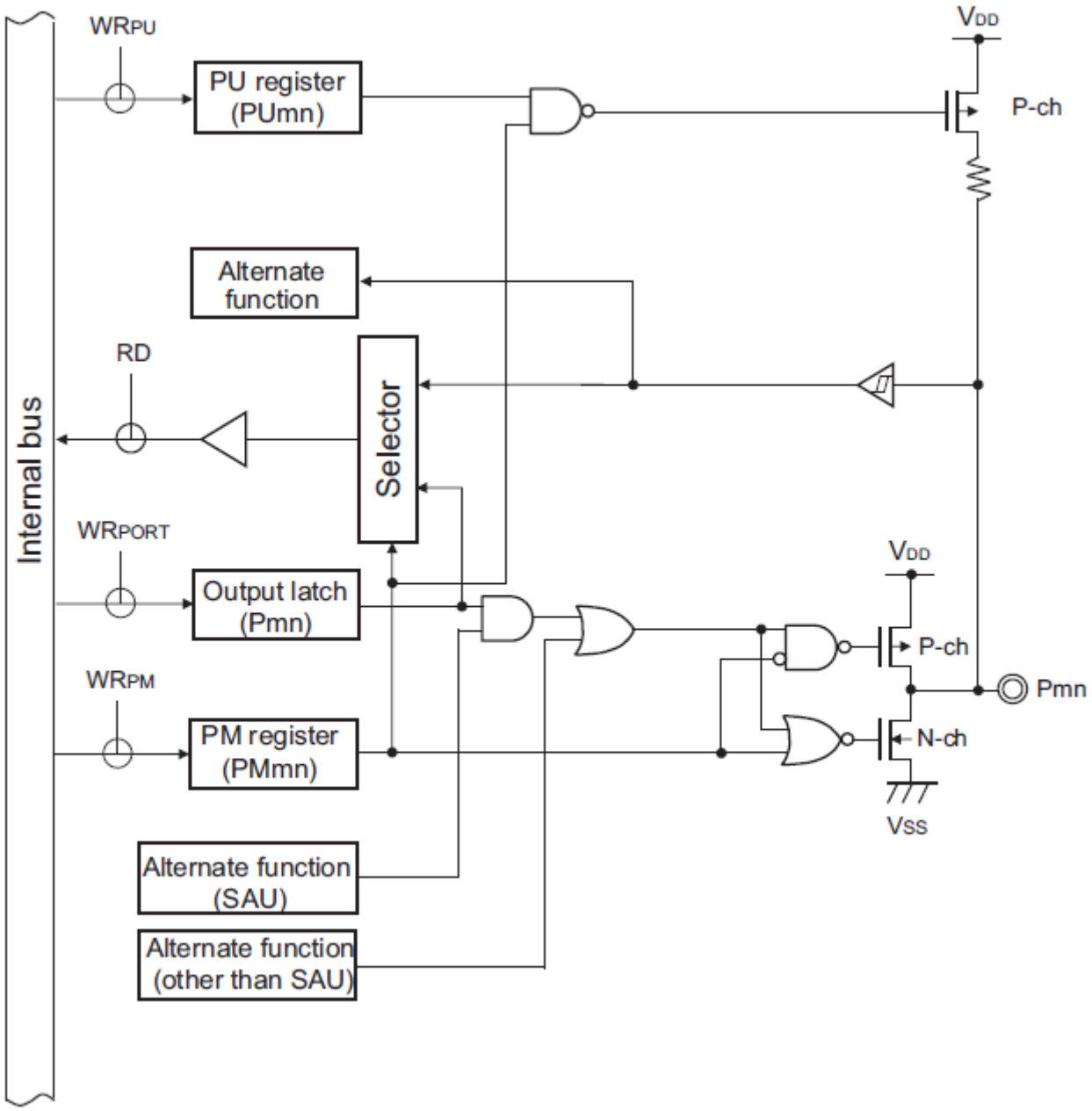


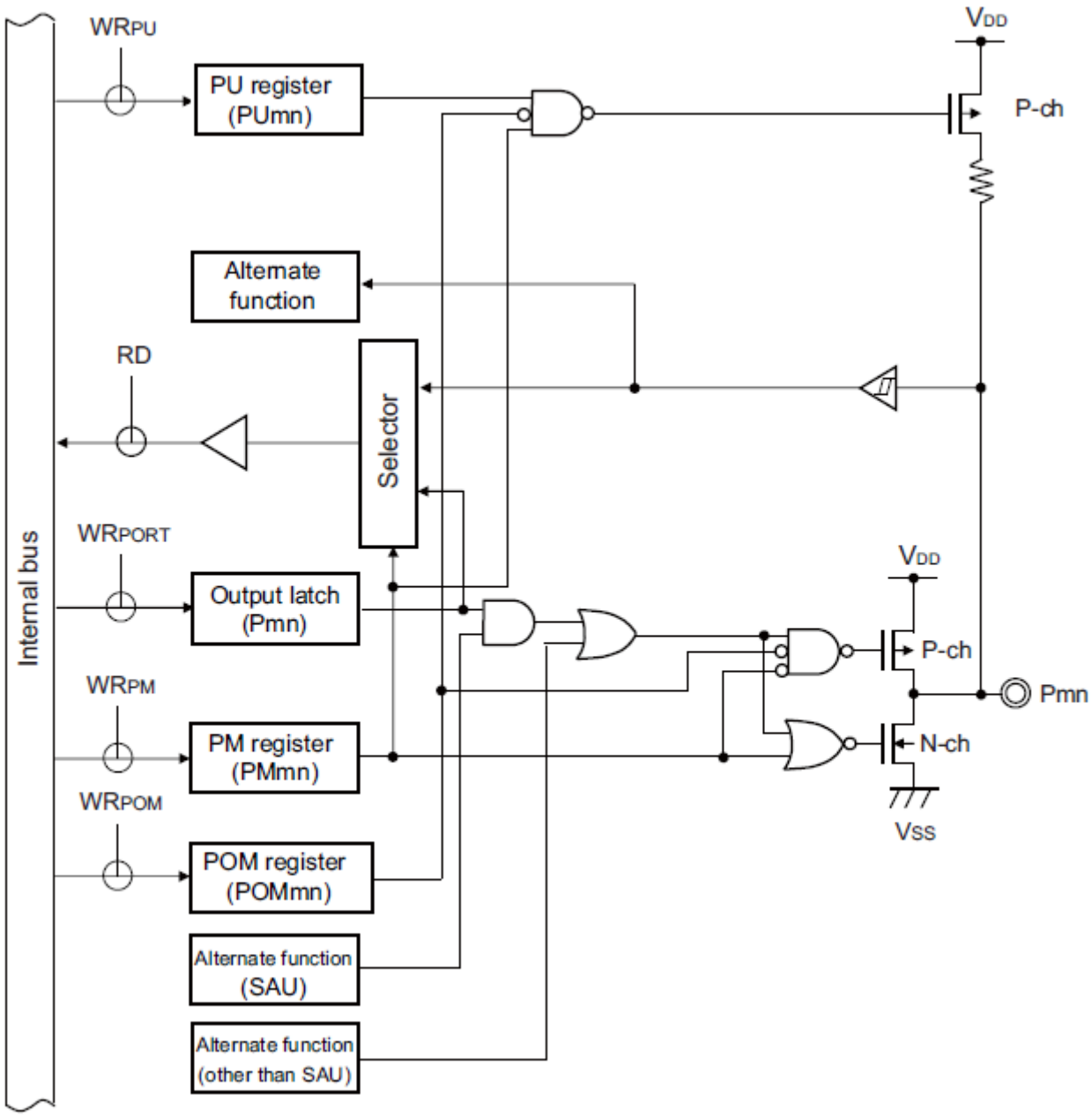
Figure 2-6. Pin Block Diagram for Pin Type 7-1-1



Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

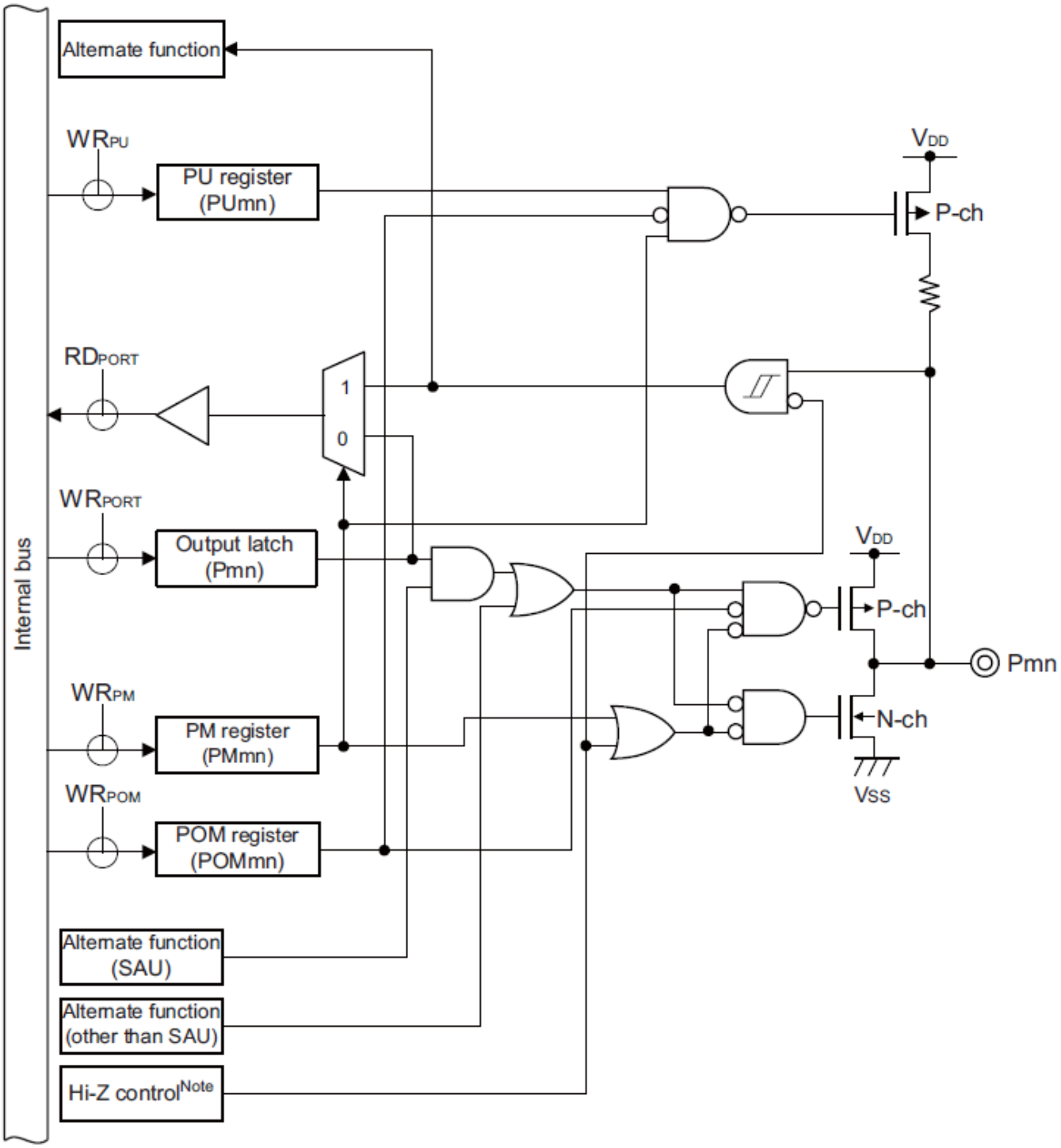
Figure 2-7. Pin Block Diagram for Pin Type 7-1-2



Remarks **1.** For alternate functions, see **2.1 Port Function**.
2. SAU: Serial array unit

Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

Figure 2-8. Pin Block Diagram for Pin Type 7-1-6



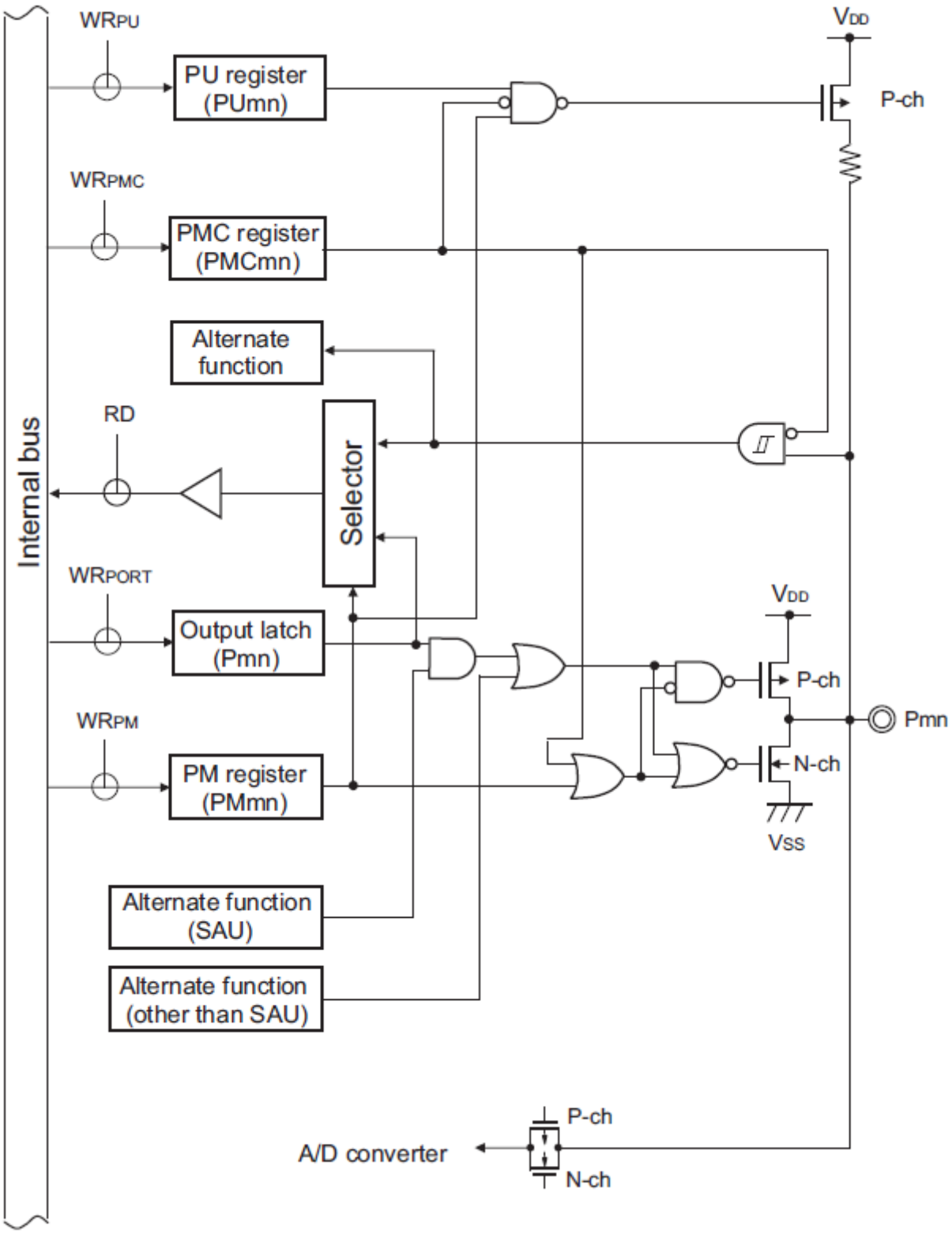
Note P206 does not provide the Hi-Z control function.

Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

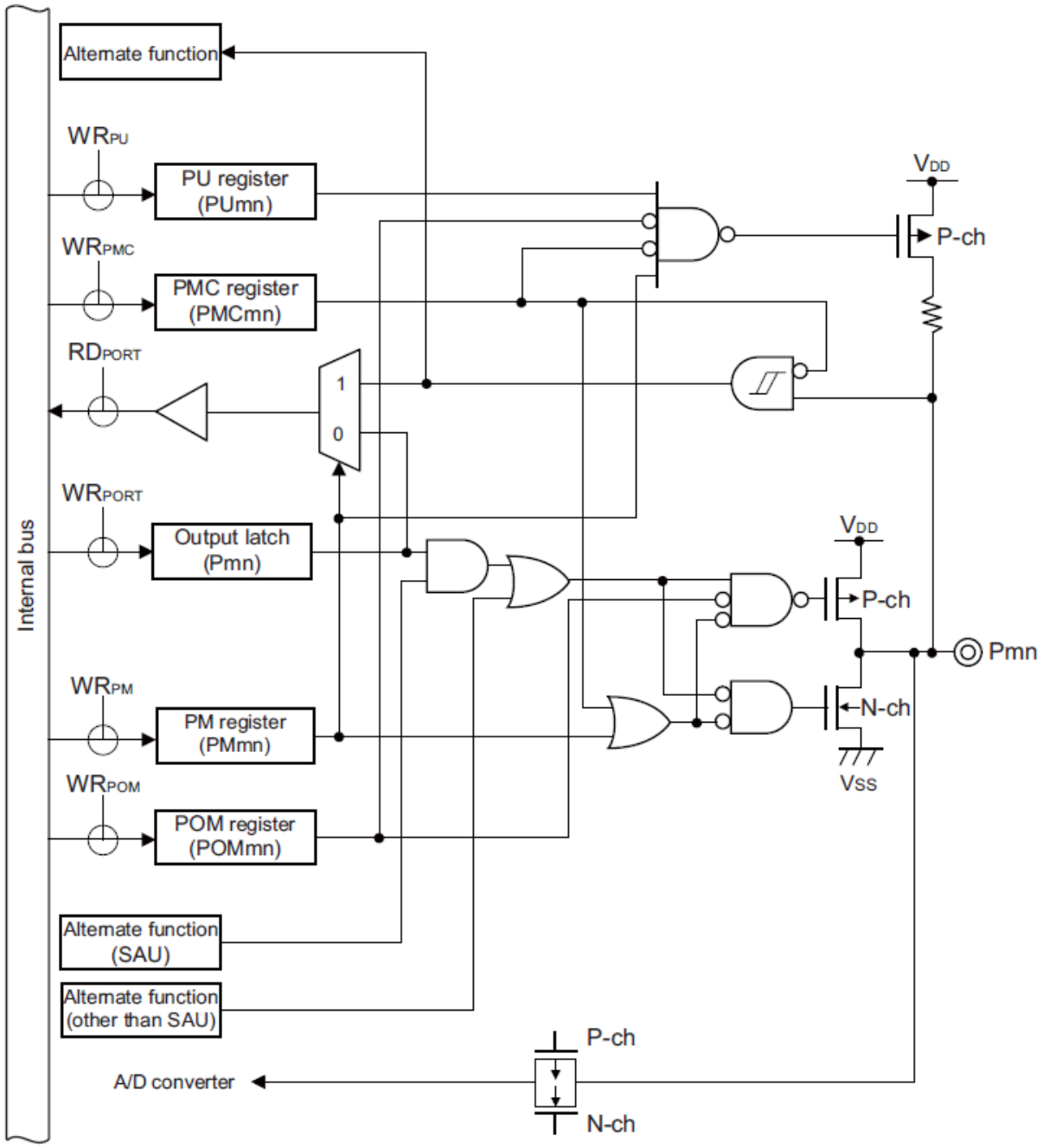
Figure 2-9. Pin Block Diagram for Pin Type 7-3-1



Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

Figure 2-10. Pin Block Diagram for Pin Type 7-3-2

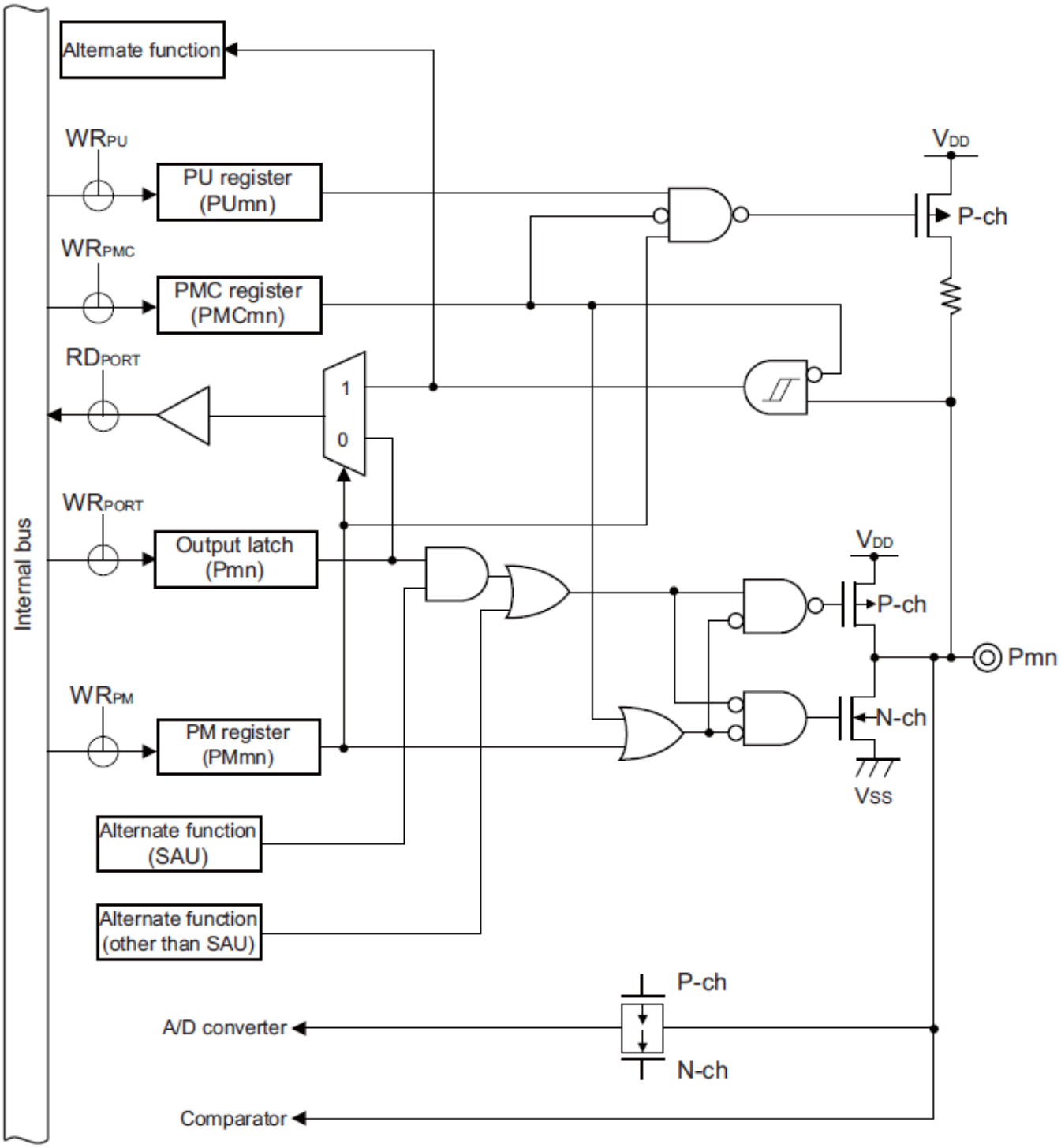


Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

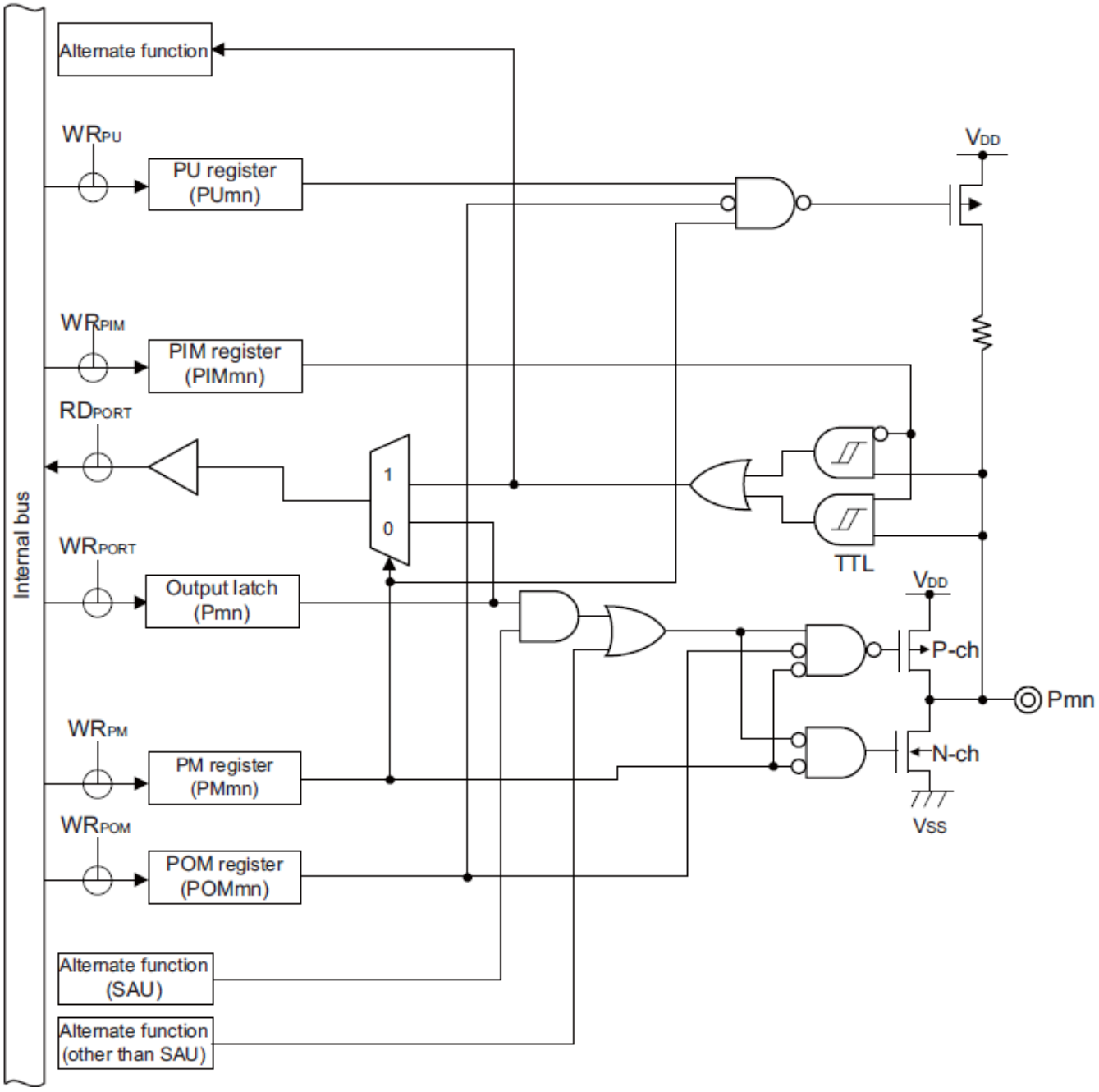
Figure 2-11. Pin Block Diagram for Pin Type 7-9-1



Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

Figure 2-12. Pin Block Diagram for Pin Type 8-1-2

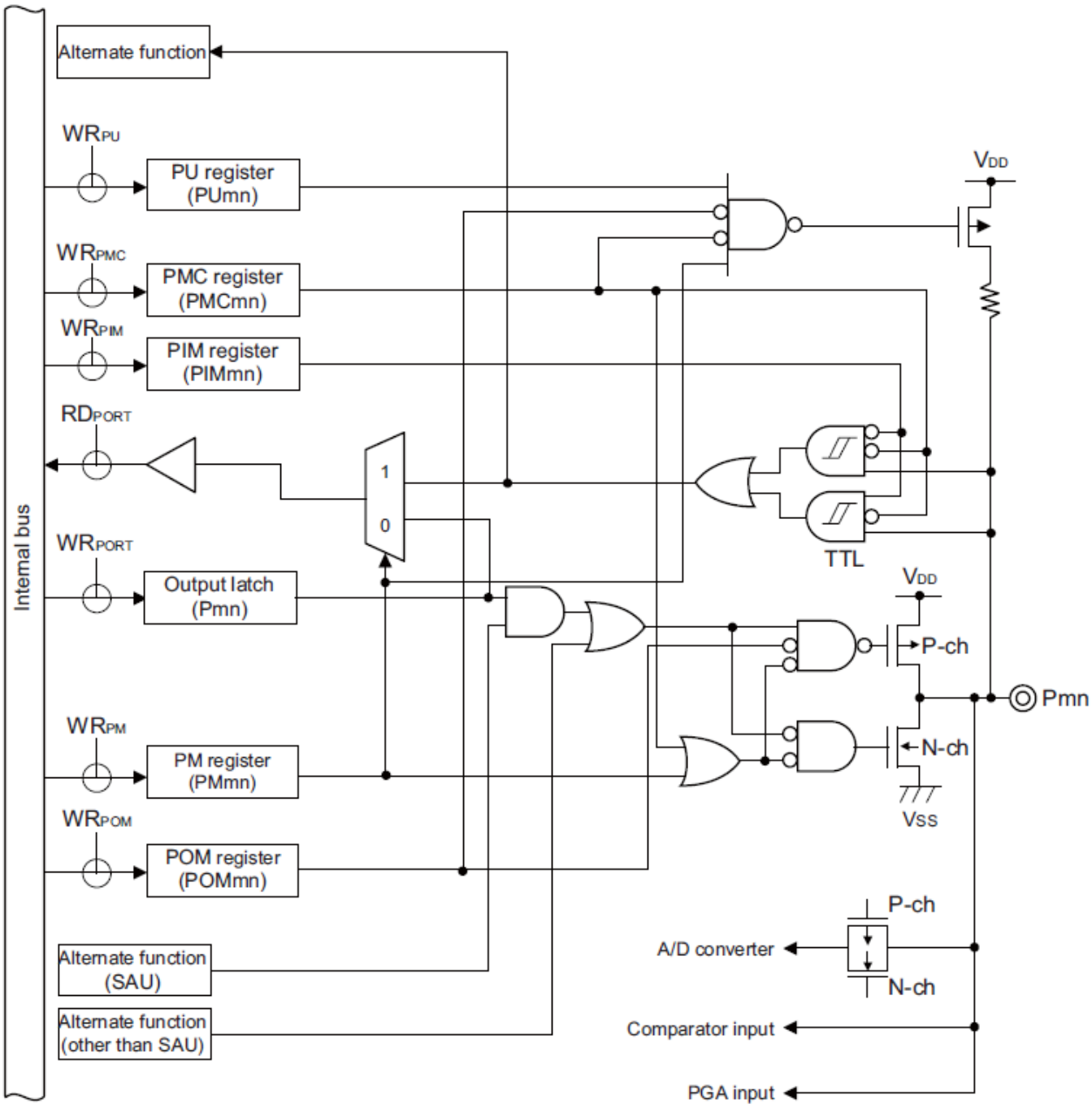


Remarks **1.** For alternate functions, see **2.1 Port Function**.
2. SAU: Serial array unit

Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, a through current may flow through in the case of high level input. It is recommended to input a low level to prevent a through current.

Figure 2-13. Pin Block Diagram for Pin Type 8-18-1



Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

24. 5.6 Controlling Clock
5.6.1 Example of setting high-speed on-chip oscillator(p.166)

Old)

After a reset release, the CPU/peripheral hardware clock (f_{CLK}) always starts operating with the high-speed on-chip oscillator clock. The frequency of the high-speed on-chip oscillator can be selected from 32, 24, 16, 12, 8, 4, and 1 MHz by using FRQSEL0 to FRQSEL3 of the option byte (000C2H). The frequency can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV).

(omitted)

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator
1	0	0	0	32 MHz
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
1	0	1	1	4 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

New)

After a reset release, the CPU/peripheral hardware clock (f_{CLK}) always starts operating with the high-speed on-chip oscillator clock. The frequency of the high-speed on-chip oscillator can be selected from 32, 24, 16, 12, 8, 6, 4, 3, 2 and 1 MHz by using FRQSEL0 to FRQSEL3 of the option byte (000C2H). The frequency can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV).

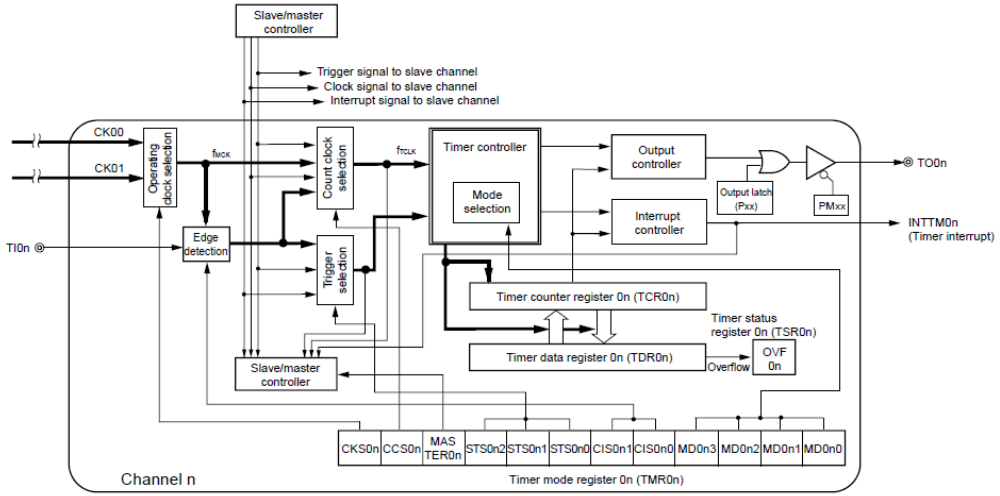
(omitted)

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator
1	0	0	0	32 MHz
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
0	0	1	0	6 MHz
1	0	1	1	4 MHz
0	0	1	1	3 MHz
1	1	0	0	2 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

25. 6.2 Configuration of Timer Array Unit
Internal Block Diagram of Channel of Timer Array Unit figure(p.191)

Old)

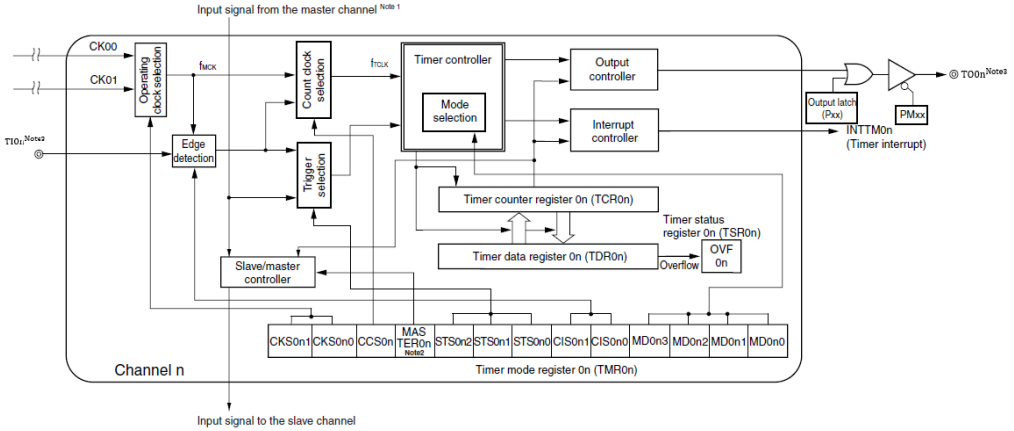
Figure 6-2. Internal Block Diagram of Channel of Timer Array Unit



Remark n=3,6

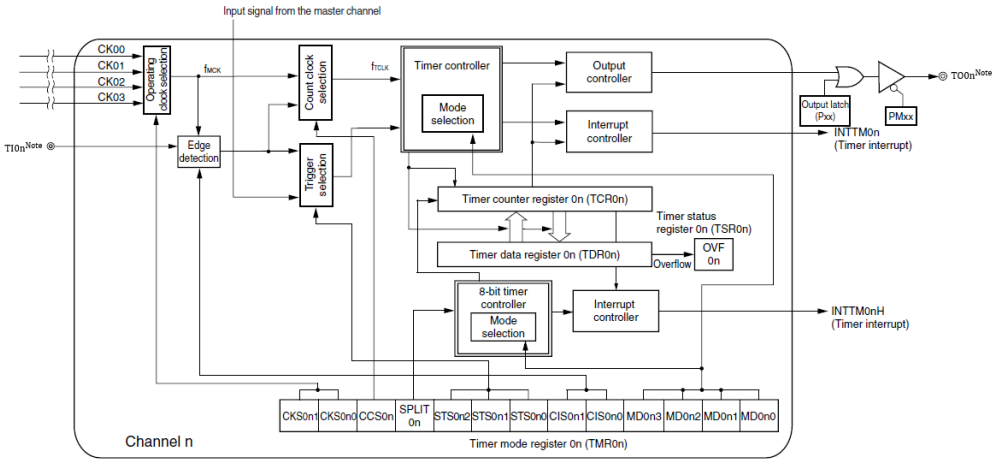
New)

Figure 6-2. Internal Block Diagram of Channel 0,2,4,6 of Timer Array Unit



Note 1.Channels2,4,and 6 only
2.MASTER0n is channels 2,4,6 only
3.TI0n,TO0n is channel 6 only
Remark n=0,2,4,6

Figure 6-3. Internal Block Diagram of Channel 1,3of Timer Array Unit



Note TI0n,TO0n is Channel3 only
Remark n=1,3

Figure 6-4. Internal Block Diagram of Channel 5 of Timer Array Unit

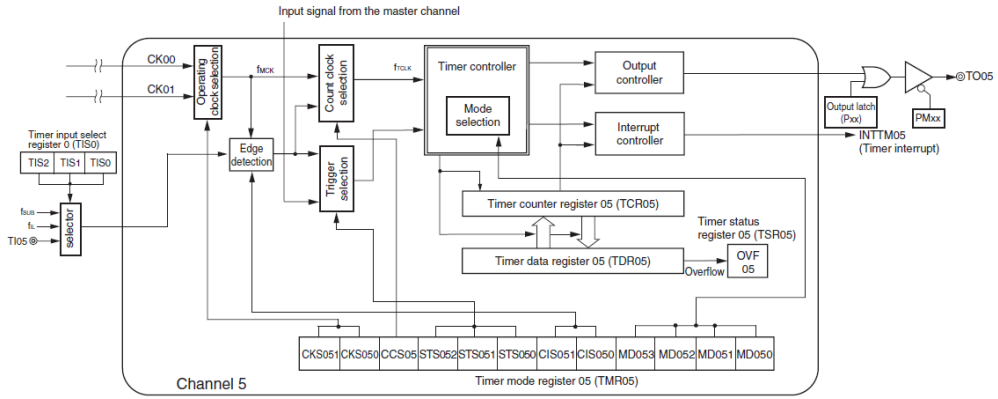
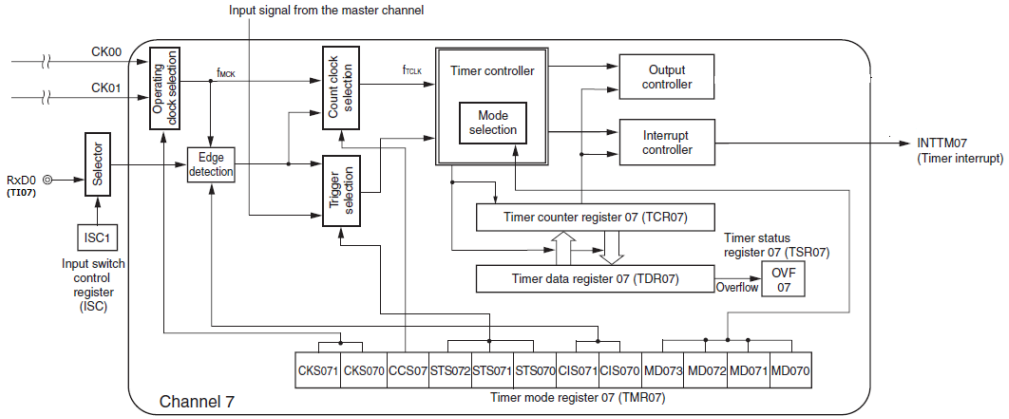


Figure 6-5. Internal Block Diagram of Channel 7 of Timer Array Unit



26. 6.4.1 Basic rules of simultaneous channel operation function(p.217)

Old)

When simultaneously using multiple channels, namely, a combination of a master channel (a reference timer mainly counting the cycle) and slave channels (timers operating according to the master channel), the following rules apply.

(1) Only an even channel **(channel 2, 4)** can be set as a master channel.
(2) **Channels 3, 5, and 6** can be set as a slave channel.
(3) Only channels whose number is greater than the master channel can be set as a slave channel.
Example: If channel 2 is set as a master channel, channel 3 can be set as a slave channel. If channel 4 is set as a master channel, channels 5 and 6 can be set as a slave channel.

(4) Two or more slave channels can be set for one master channel.
(5) When two or more master channels are to be used, slave channels with a master channel between them may not be set.
Example: If channels 2 and 4 are set as master channels, channel 3 can be set as the slave channels of master channel 2. Channels 5 and 6 cannot be set as the slave channels of master channel 2.

(omitted)

New)

When simultaneously using multiple channels, namely, a combination of a master channel (a reference timer mainly counting the cycle) and slave channels (timers operating according to the master channel), the following rules apply.

(1) Only an even channel (channel 0, 2, 4,…) can be set as a master channel.
(2) Except Channel 0 can be set as a slave channel.
(3) Only channels whose number is greater than the master channel can be set as a slave channel.
Example: If channel 2 is set as a master channel, channel 3 can be set as a slave channel. If channel 4 is set as a master channel, channels 5 and 6 can be set as a slave channel.

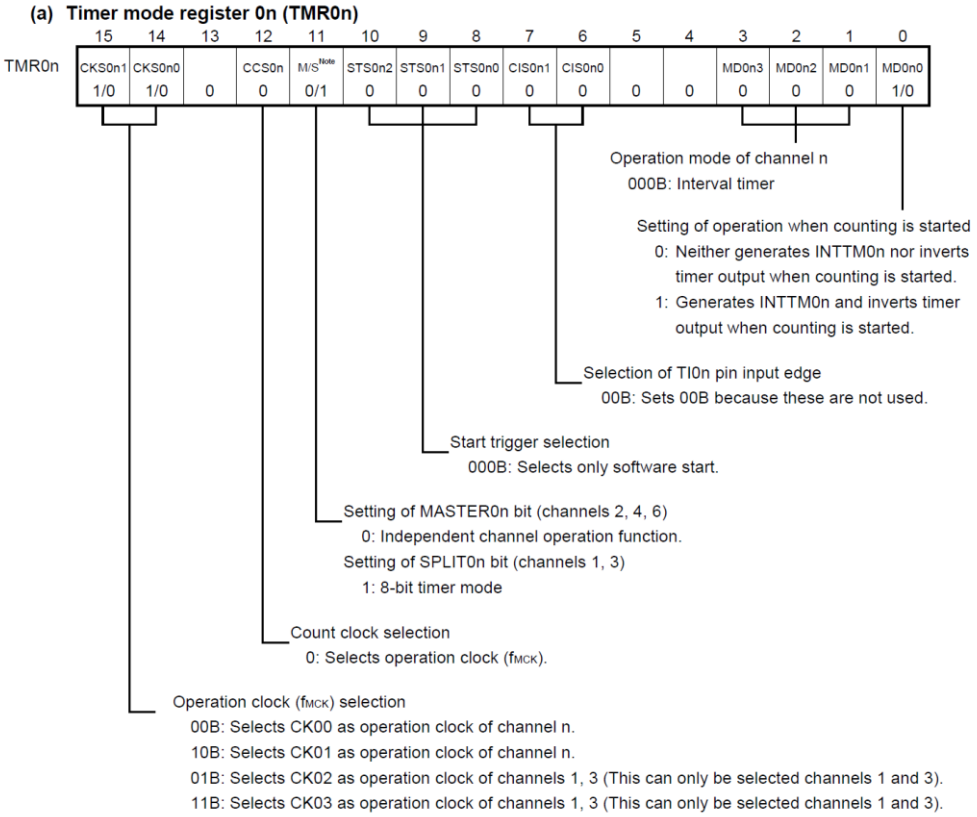
(4) Two or more slave channels can be set for one master channel.
(5) When two or more master channels are to be used, slave channels with a master channel between them may not be set.
Example: If channels 2 and 4 are set as master channels, channel 3 can be set as the slave channels of master channel 2. Channels 5 and 6 cannot be set as the slave channels of master channel 2.

(omitted)

27. 6.7 Independent Channel Operation Function of Timer Array Unit 6.7.1 Operation as interval timer/square wave output(p.239)

Old)

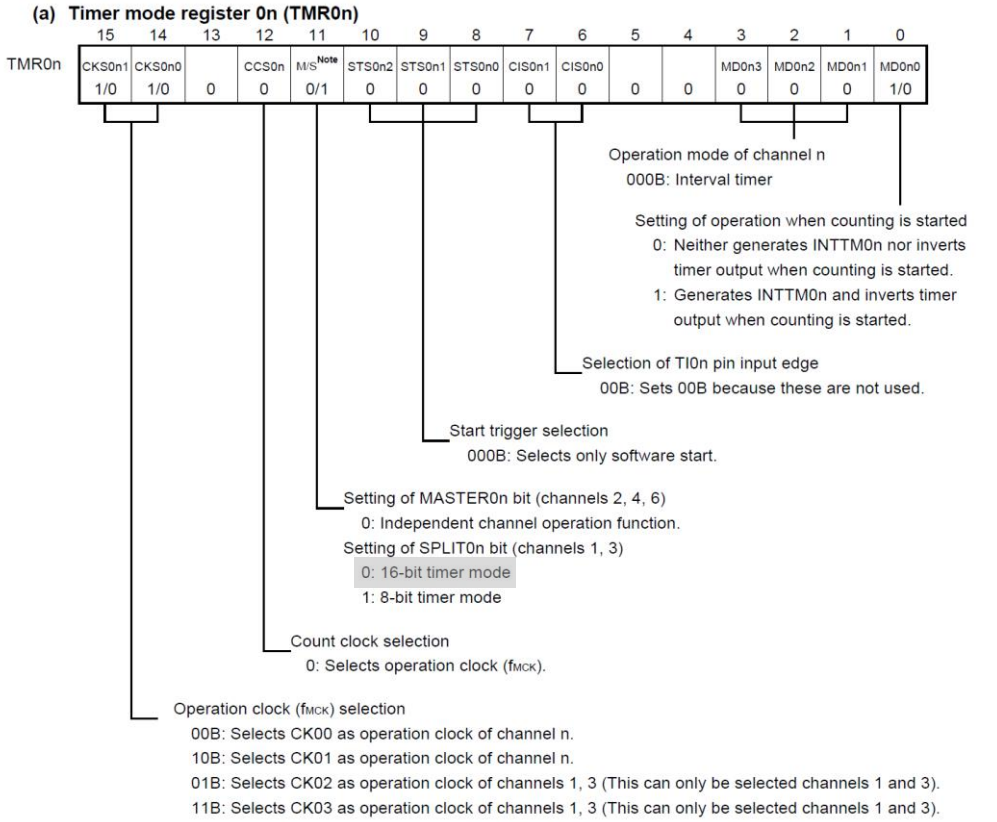
Figure 6-38. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output (1/2)



(omitted)

New)

Figure 6-38. Example of Set Contents of Registers During Operation as Interval Timer/Square Wave Output

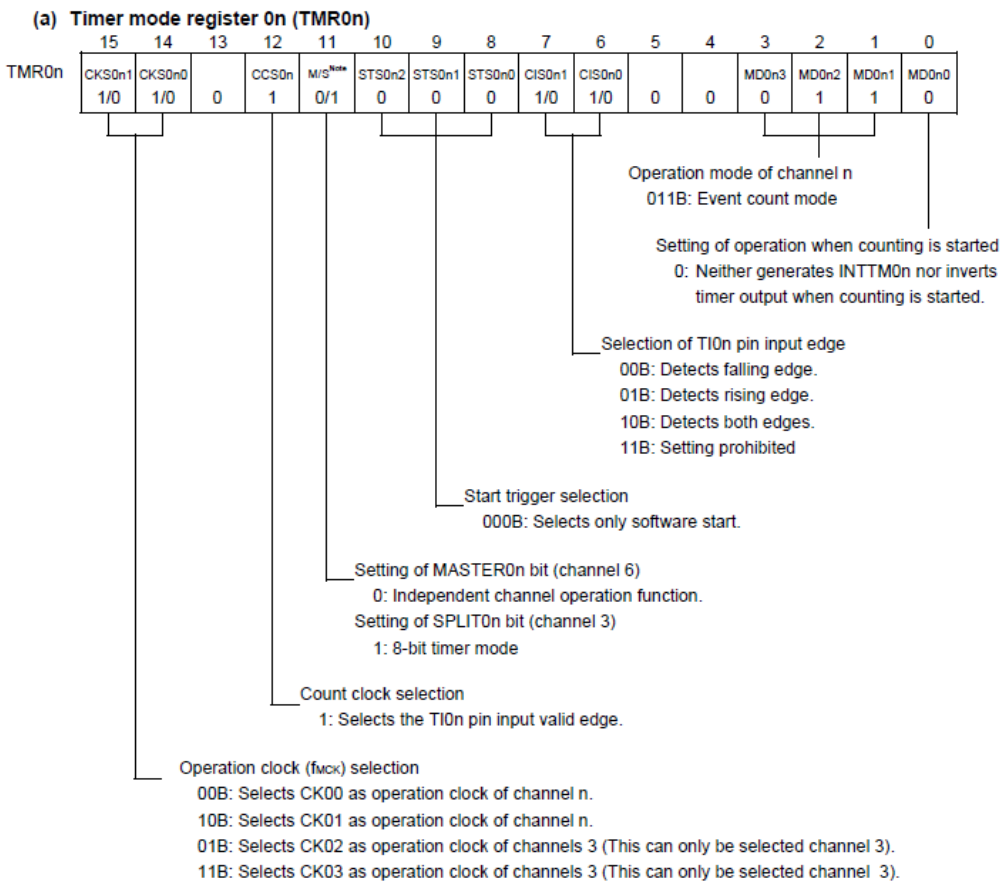


(omitted)

28. 6.7 Independent Channel Operation Function of Timer Array Unit 6.7.2Operation as external event counter(p.245)

Old)

Figure 6-42. Example of Set Contents of Registers in External Event Counter Mode (1/2)



(omitted)

Note TMR06: MASTER06 bit
TMR03: SPLIT03 bit
TMR00,TMR05,TMR07: Fixed to 0
Remark n:Channel number(n=3,5,6)

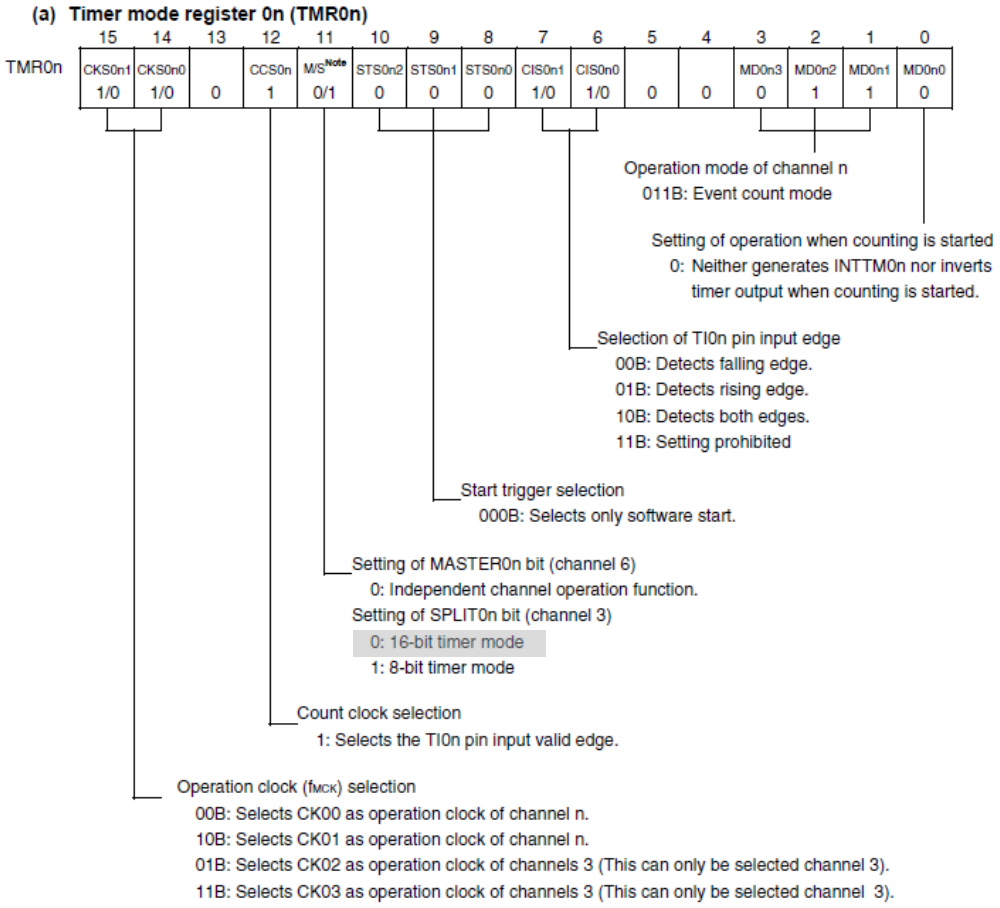
Figure 6-42. Example of Set Contents of Registers in External Event Counter Mode (2/2)

(omitted)

Remark n:Channel number(n=3,5,6)

New)

Figure 6-42. Example of Set Contents of Registers in External Event Counter Mode



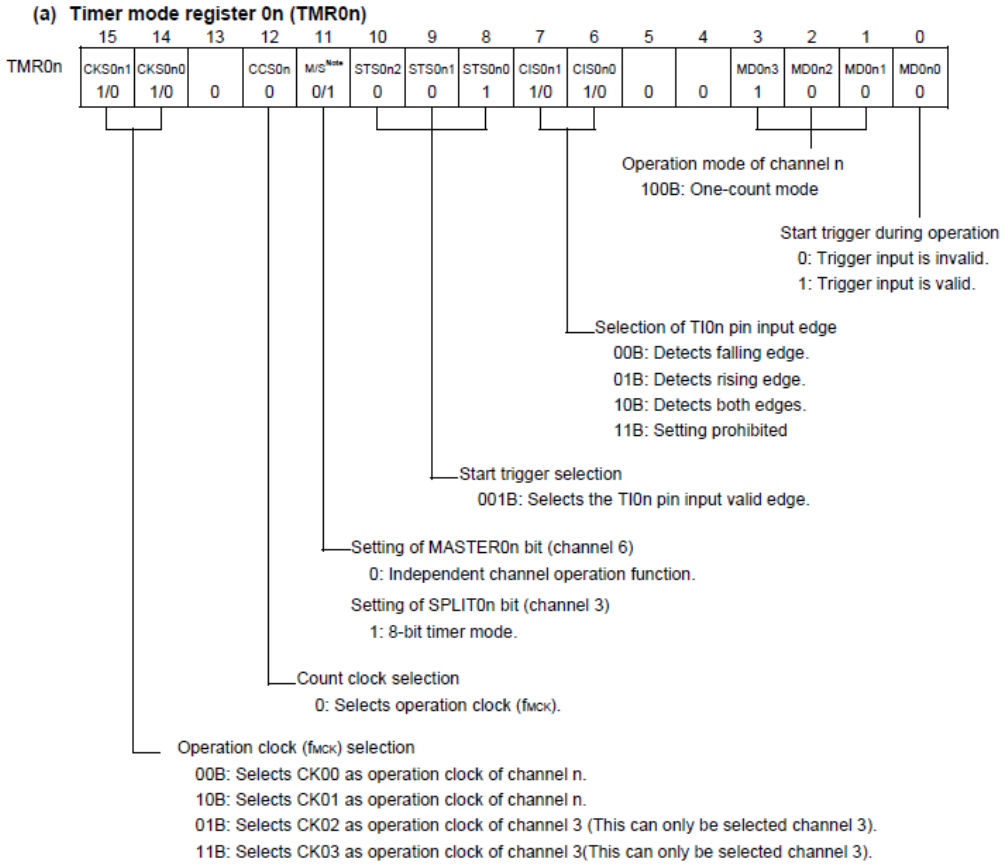
(omitted)

Note TMR06: MASTER06 bit
TMR03: SPLIT03 bit
TMR05,TMR07: Fixed to 0
Remark n:Channel number(n=3,5,6,7)

29. 6.7 Independent Channel Operation Function of Timer Array Unit 6.7.5 Operation as delay counter(p.258)

Old)

Figure 6-54. Example of Set Contents of Registers to Delay Counter (1/2)



(omitted)

Note TMR06: MASTER06 bit
TMR03: SPLIT03 bit
TMR05: Fixed to 0
Remark n:Channel number(n=3,5,6)

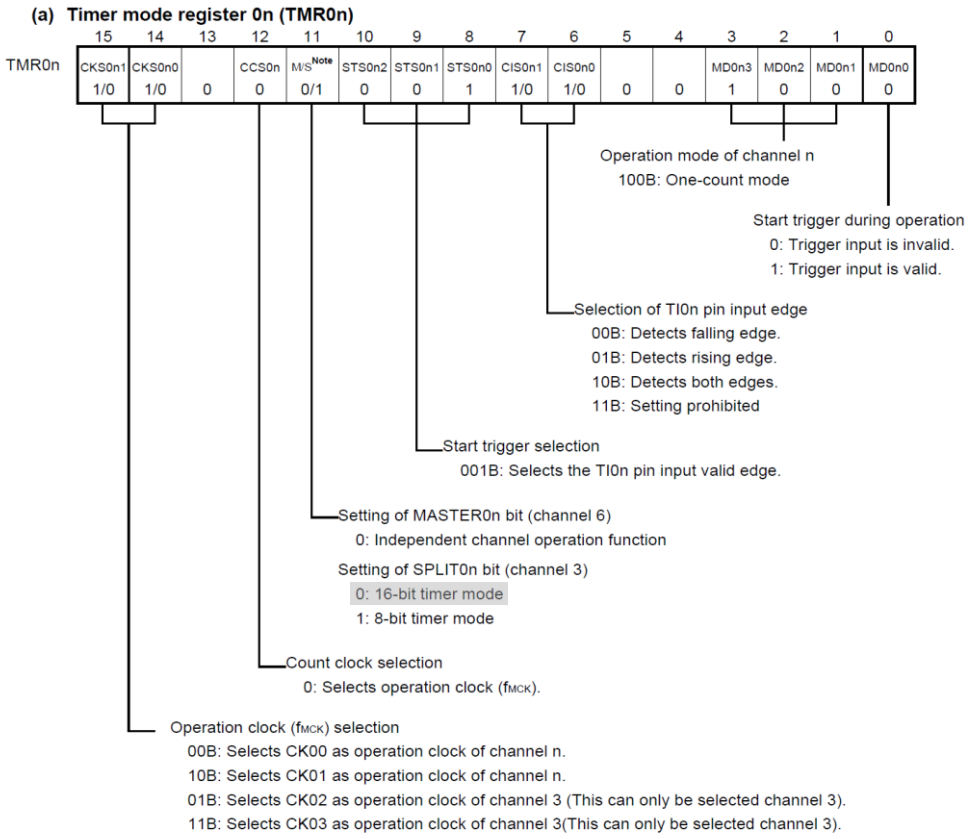
Figure 6-54. Example of Set Contents of Registers to Delay Counter 2/2)

(omitted)

Remark n:Channel number(n=3,5,6)

New)

Figure 6-54. Example of Set Contents of Registers to Delay Counter



(omitted)

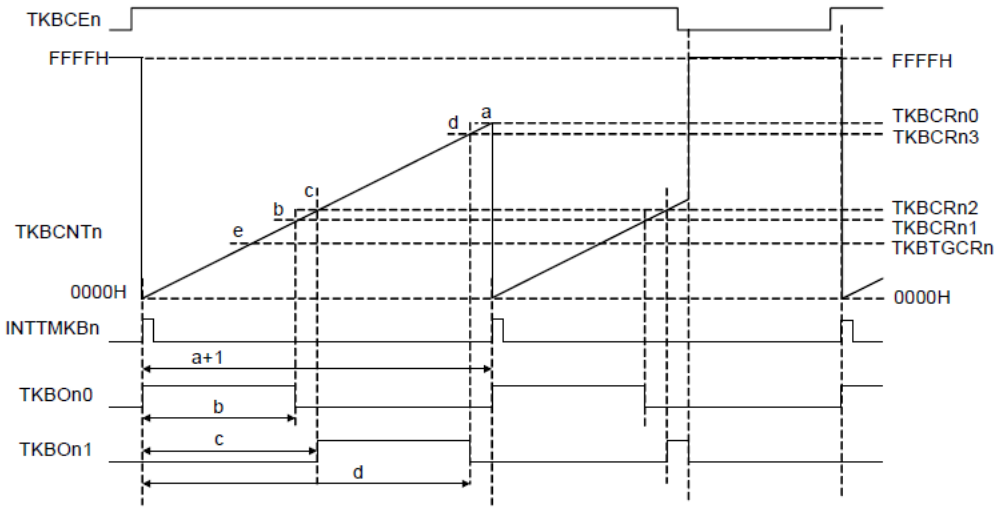
Note TMR06: MASTER06 bit
TMR03: SPLIT03 bit
TMR05,TMR07: Fixed to 0
Remark n:Channel number(n=3,5,6,7)

30. 7.4.3 Stop/restart operation

Figure of Timing of Stop Operation(TKBTOLnp=0, TKBTODnp=0)(p.312)

Old)

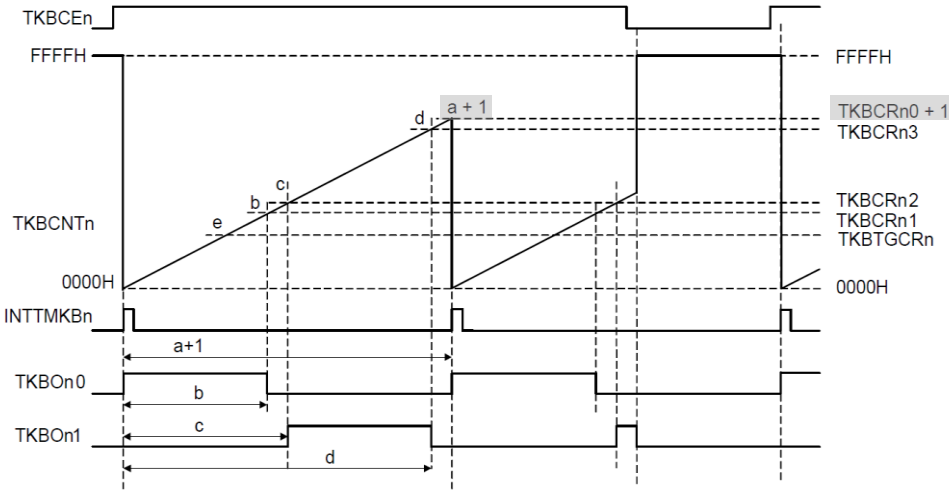
Figure 7-31. Figure of Timing of Stop Operation (TKBTOLnp = 0, TKBTODnp = 0)



(omitted)

New)

Figure 7-31. Figure of Timing of Stop Operation (TKBTOLnp = 0, TKBTODnp = 0)

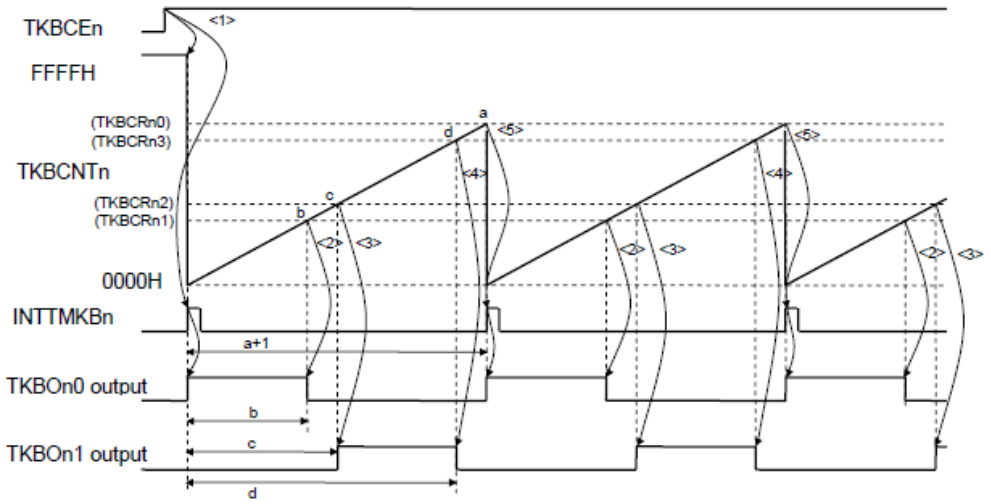


(omitted)

31. 7.4.5 Standalone mode (period controlled by TKBCRn0) Timing Sample for Standalone Mode (Period Controlled by TKBCRn0)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))(p.317)

Old)

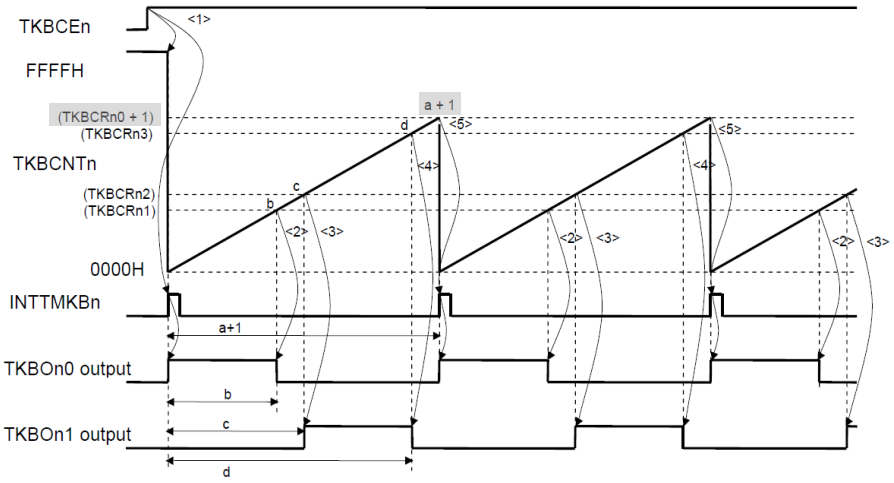
Figure 7-38. Timing Sample for Standalone Mode (Period Controlled by TKBCRn0) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



(omitted)

New)

Figure 7-38. Timing Sample for Standalone Mode (Period Controlled by TKBCRn0) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))

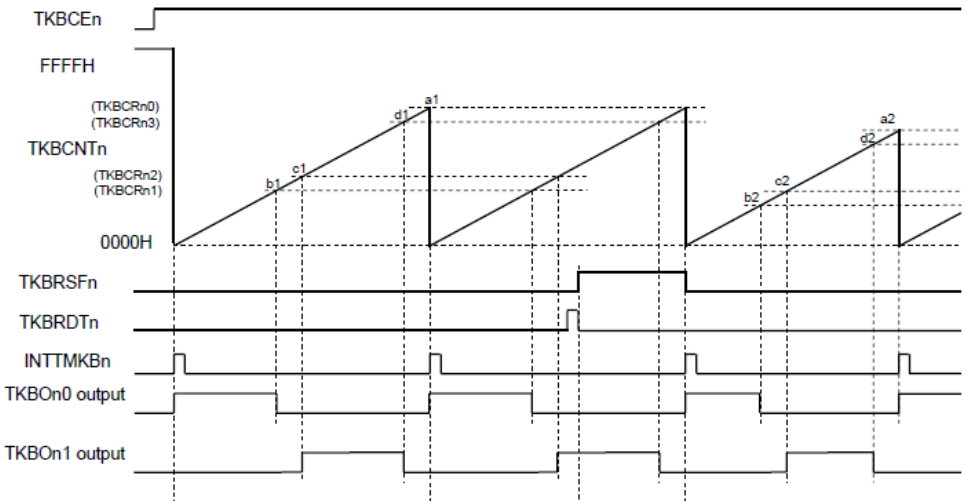


(omitted)

32. 7.4.5 Standalone mode (period controlled by TKBCRn0) Batch Overwrite Function: Figure of the Timing of Buffer Updating During Counting Operation(p.320)

Old)

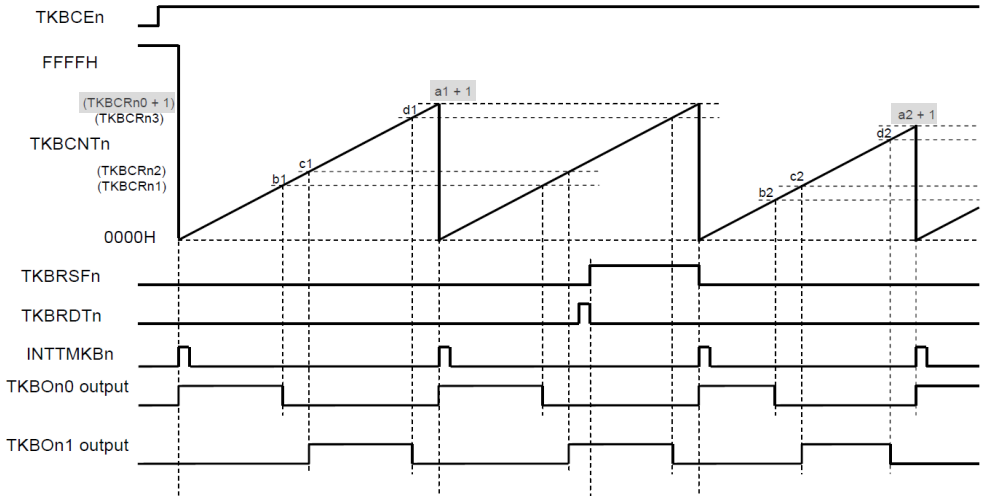
Figure 7-40. Batch Overwrite Function: Figure of the Timing of Buffer Updating During Counting Operation



(omitted)

New)

Figure 7-40. Batch Overwrite Function: Figure of the Timing of Buffer Updating During Counting Operation

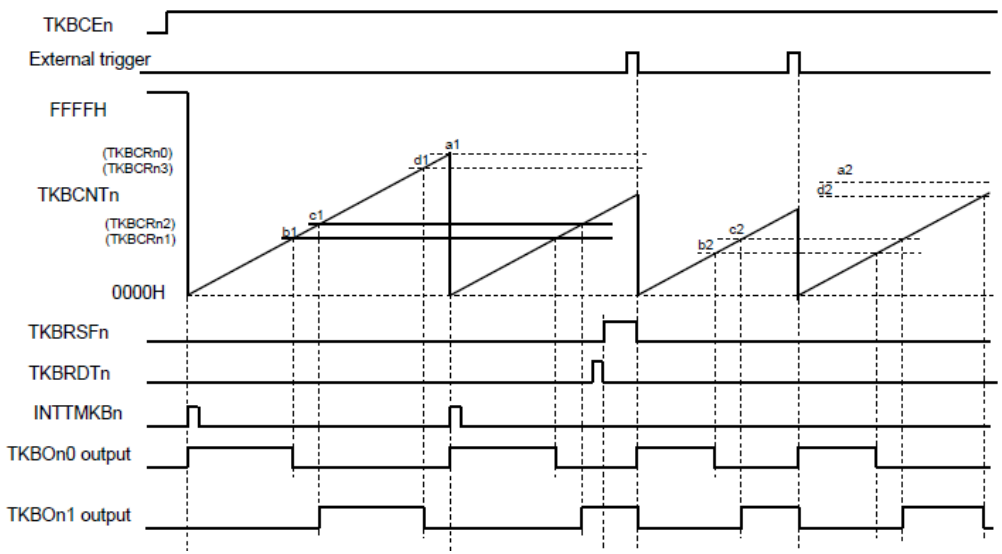


(omitted)

33. 7.4.6 Standalone mode (period controlled by external trigger input) Batch Overwrite Function: Figure of Standalone for External Trigger Input Factor and the Timing of Buffer Updating During Counting Operation (TKBTSEn Bit Set to 1)(p.325)

Old)

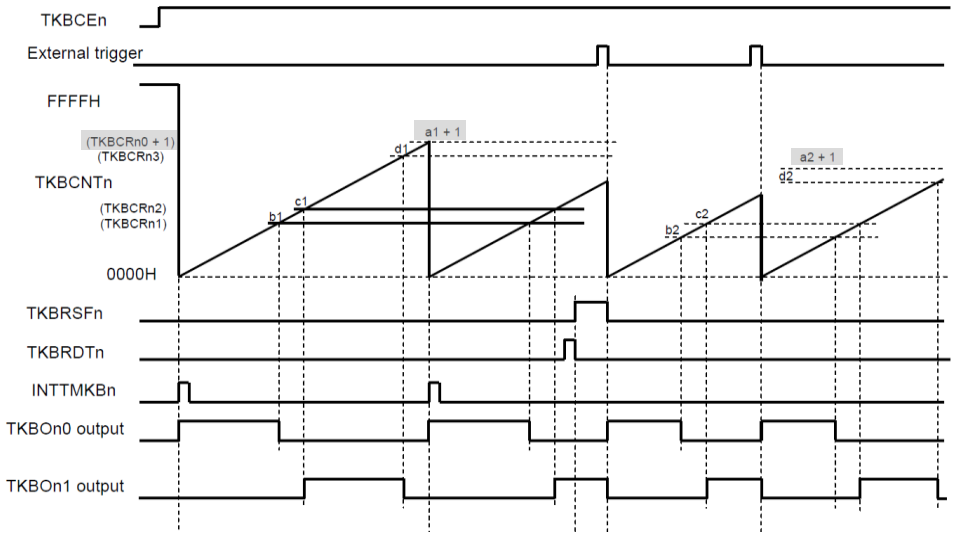
Figure 7-42. Batch Overwrite Function: Figure of Standalone for External Trigger Input Factor and the Timing of Buffer Updating During Counting Operation (TKBTSEn Bit Set to 1)



(omitted)

New)

Figure 7-42. Batch Overwrite Function: Figure of Standalone for External Trigger Input Factor and the Timing of Buffer Updating During Counting Operation (TKBTSEn Bit Set to 1)

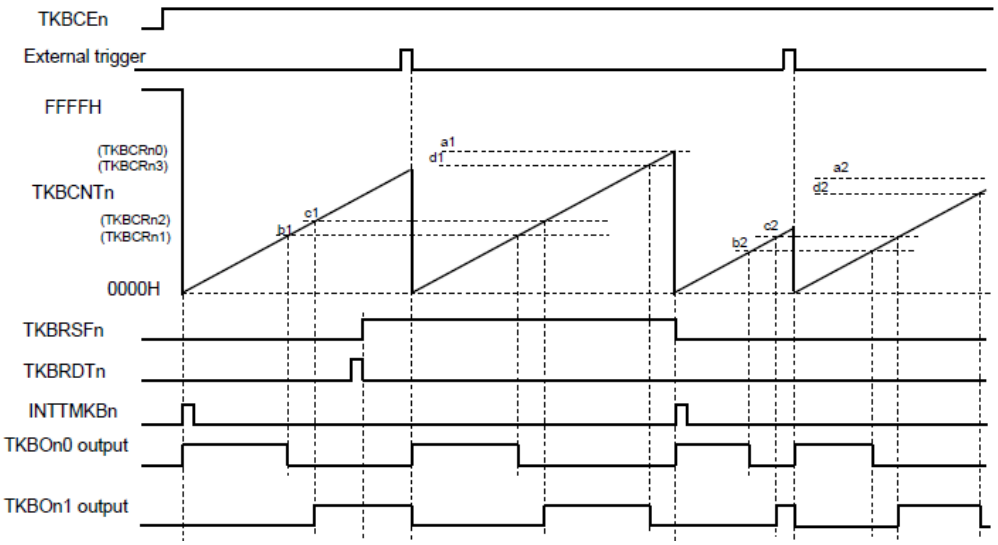


(omitted)

34. 7.4.6 Standalone mode (period controlled by external trigger input) Batch Overwrite Function: Figure of standalone for External Trigger Input Factor and the Timing of Buffer Updating during Counting Operation (TKBTSEn bit clear to 0)(p.327)

Old)

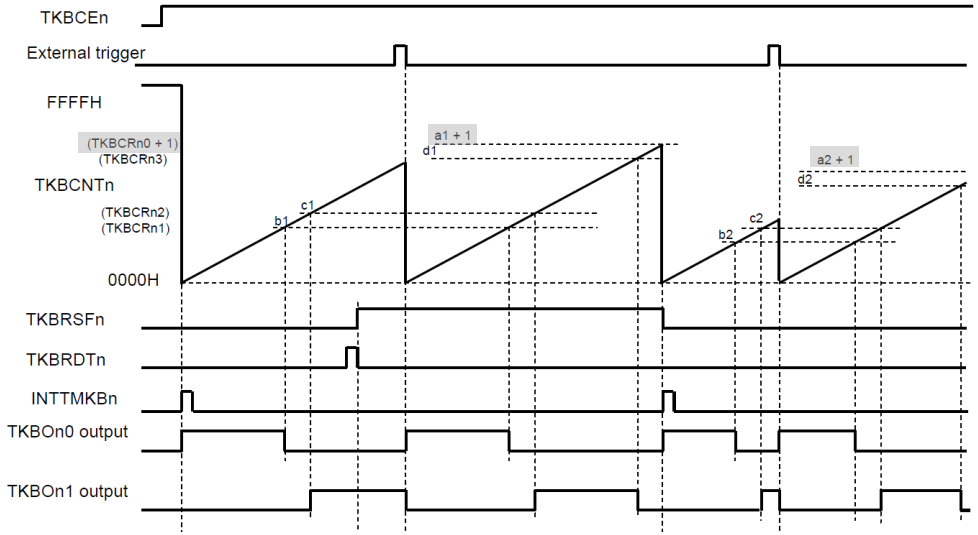
Figure 7-43. Batch Overwrite Function: Figure of standalone for External Trigger Input Factor and the Timing of Buffer Updating during Counting Operation (TKBTSEn bit clear to 0)



(omitted)

New)

Figure 7-43. Batch Overwrite Function: Figure of standalone for External Trigger Input Factor and the Timing of Buffer Updating during Counting Operation (TKBTSEn bit clear to 0)



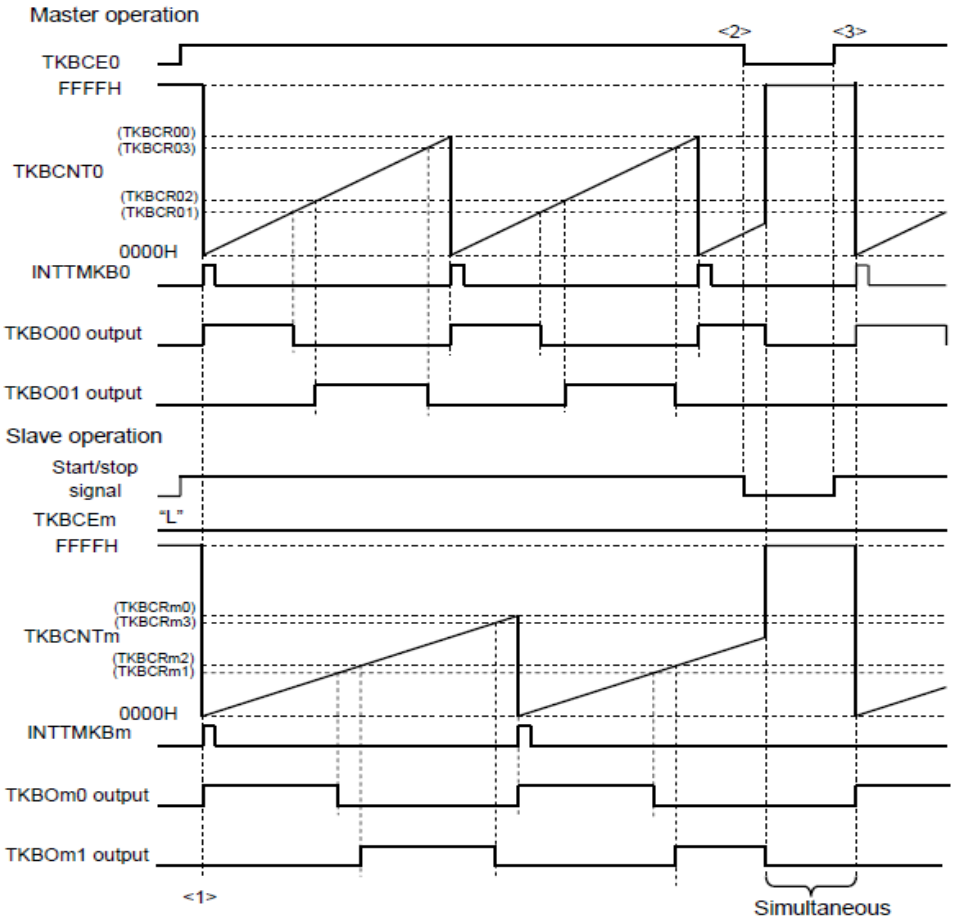
(omitted)

35. 7.4.7 Simultaneous start/stop mode

Figure 7-45. Timing Sample for Simultaneous Start/Stop Mode (Period Controlled by TKBCRn0)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))(p.336)

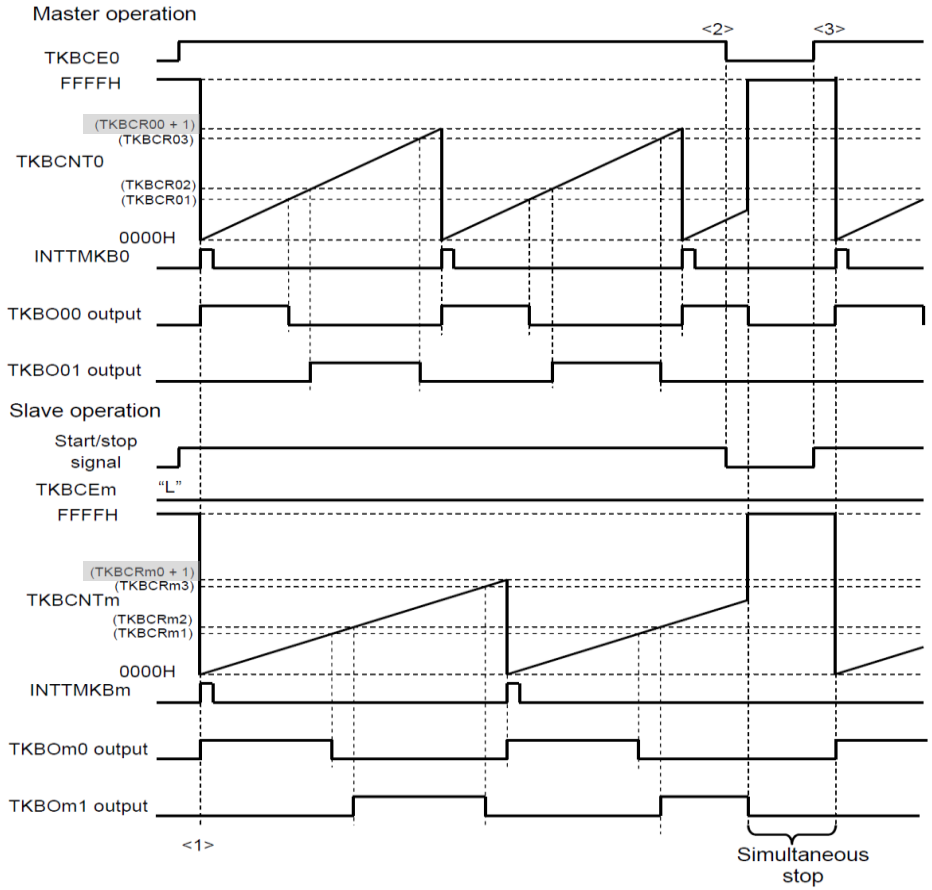
Old)

Figure 7-45. Timing Sample for Simultaneous Start/Stop Mode (Period Controlled by TKBCRn0)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



New)

Figure 7-45. Timing Sample for Simultaneous Start/Stop Mode (Period Controlled by TKBCRn0)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))

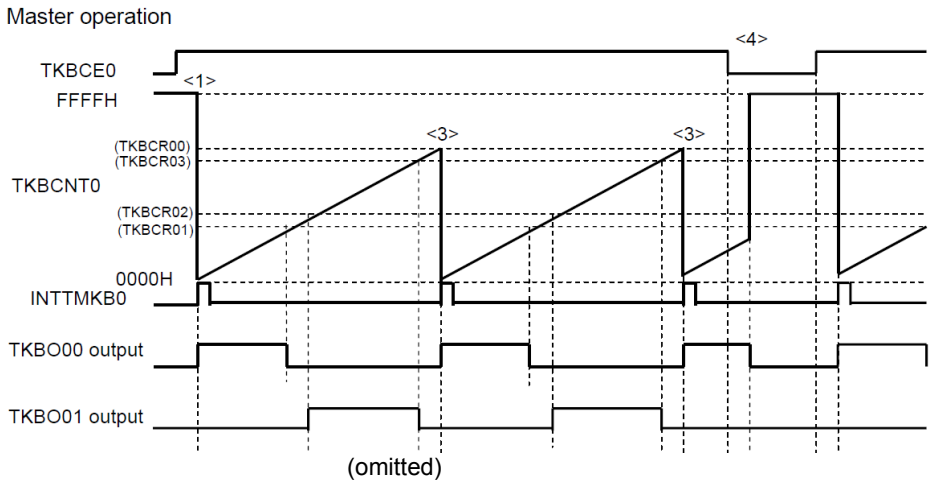


36. 7.4.8 Synchronous start/clear mode

Figure 7-47. Timing Sample for Synchronous Start/Clear Mode (Period Controlled by Master)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))(p.343)

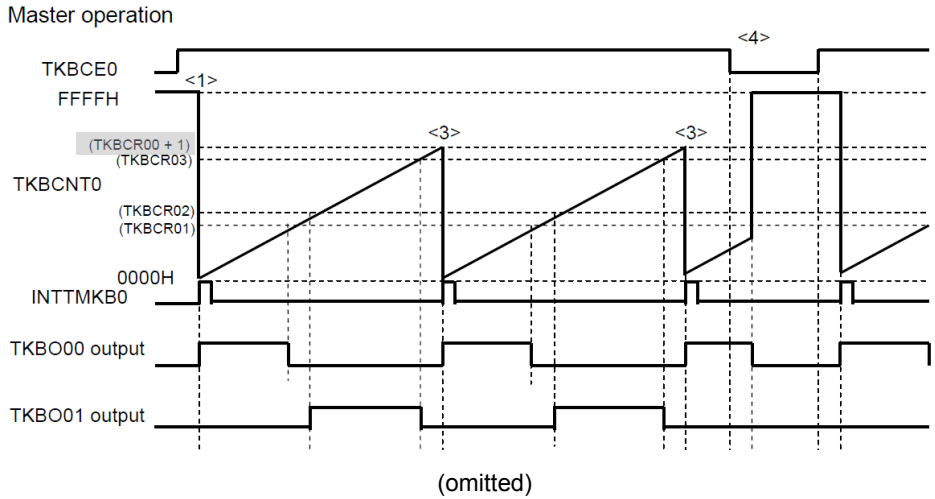
Old)

Figure 7-47. Timing Sample for Synchronous Start/Clear Mode (Period Controlled by Master) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



New)

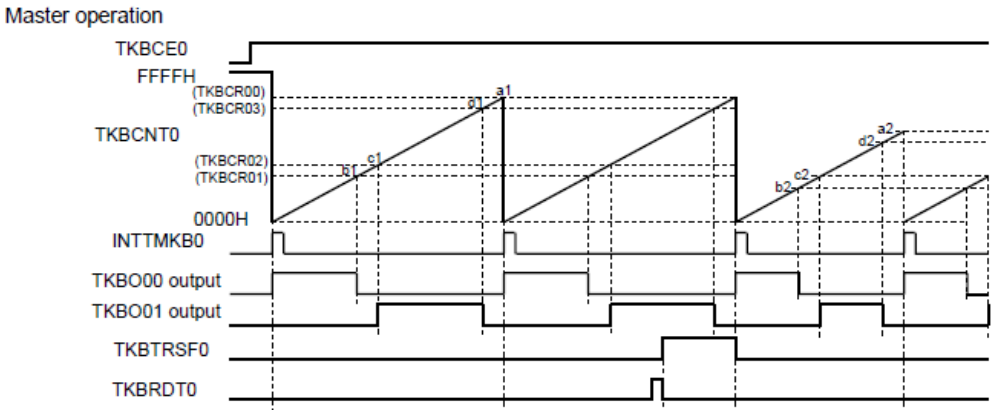
Figure 7-47. Timing Sample for Synchronous Start/Clear Mode (Period Controlled by Master) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



37. 7.4.8 Synchronous start/clear mode Figure7-48.Timing Sample for Synchronous Start/Clear Mode (Period Controlled by Master)(at Batch Overwrite)(p.345)

Old)

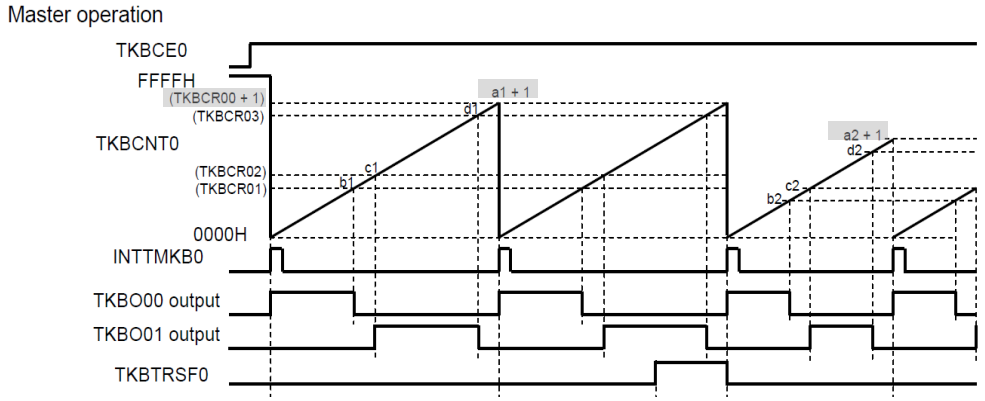
Figure 7-48. Timing Sample for Synchronous Start/Clear Mode
(Period Controlled by Master)(at Batch Overwrite)



(omitted)

New)

Figure 7-48. Timing Sample for Synchronous Start/Clear Mode
(Period Controlled by Master)(at Batch Overwrite)

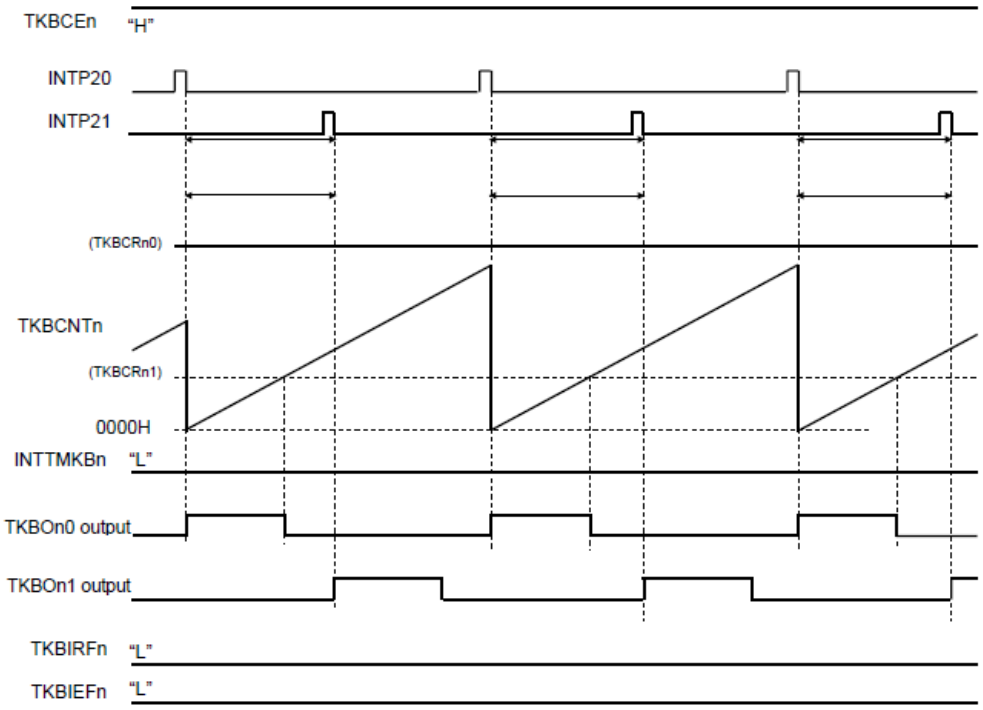


(omitted)

38. 7.4.9 Interleave PFC (Power Factor Correction) output mode Figure 7-49.Operation Outline of Basic Operation for Interleave PFC Mode (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))(p.347)

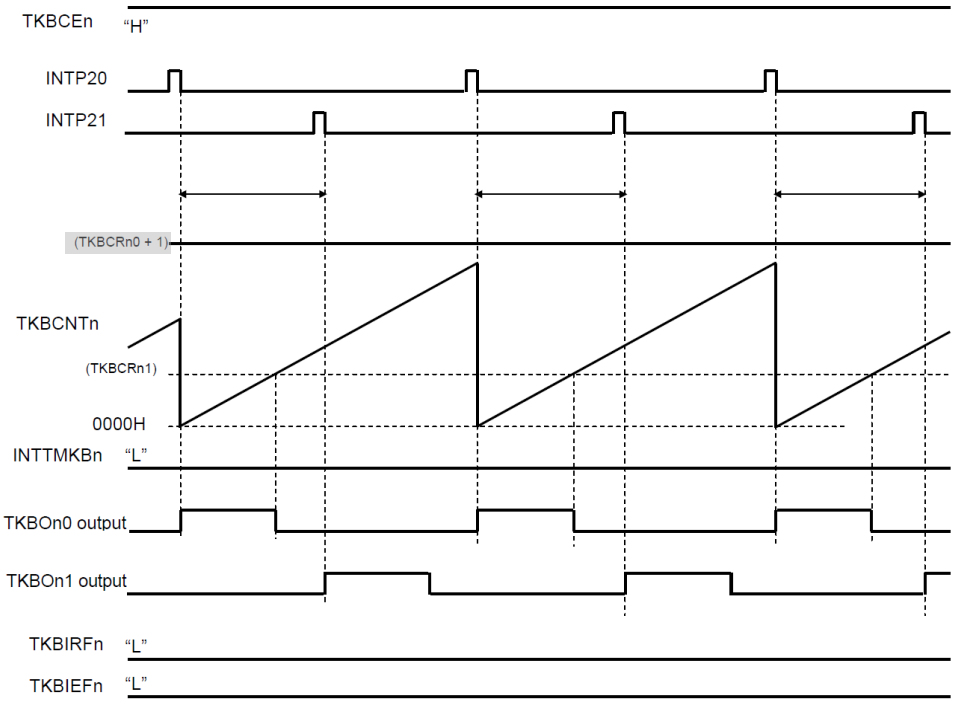
Old)

Figure 7-49. Operation Outline of Basic Operation for Interleave PFC Mode (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



New)

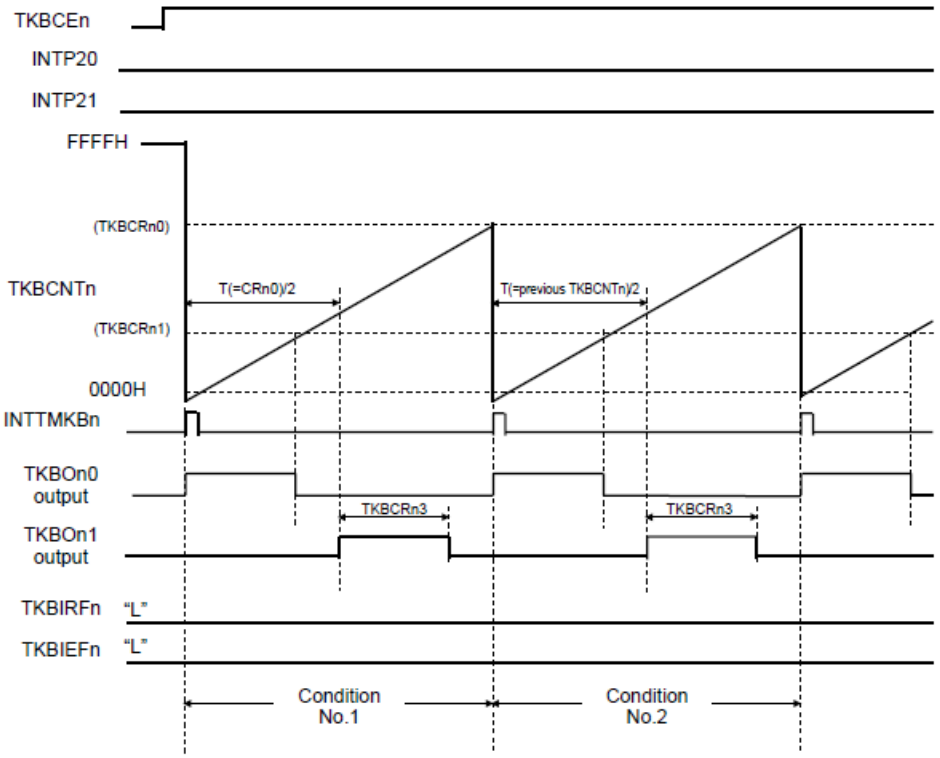
Figure 7-49. Operation Outline of Basic Operation for Interleave PFC Mode (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



39. 7.4.9 Interleave PFC (Power Factor Correction) output mode Figure 7-50. Figure of Timing of Interleave PFC Mode (Operation for Conditions No. 1 and No. 2)(p.349)

Old)

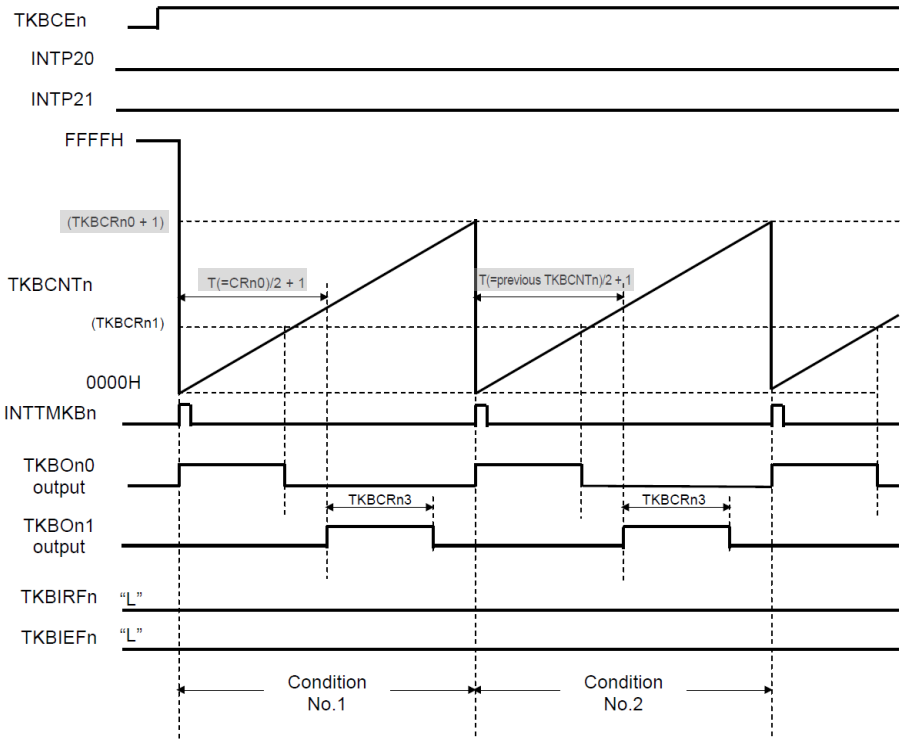
Figure 7-50. Figure of Timing of Interleave PFC Mode
(Operation for Conditions No. 1 and No. 2)



(omitted)

New)

Figure 7-50. Figure of Timing of Interleave PFC Mode
(Operation for Conditions No. 1 and No. 2)(at Default Value of Output is Low Level(TKBTODnp=0) and Active Level Is High Level(TKBTOLnp=0))

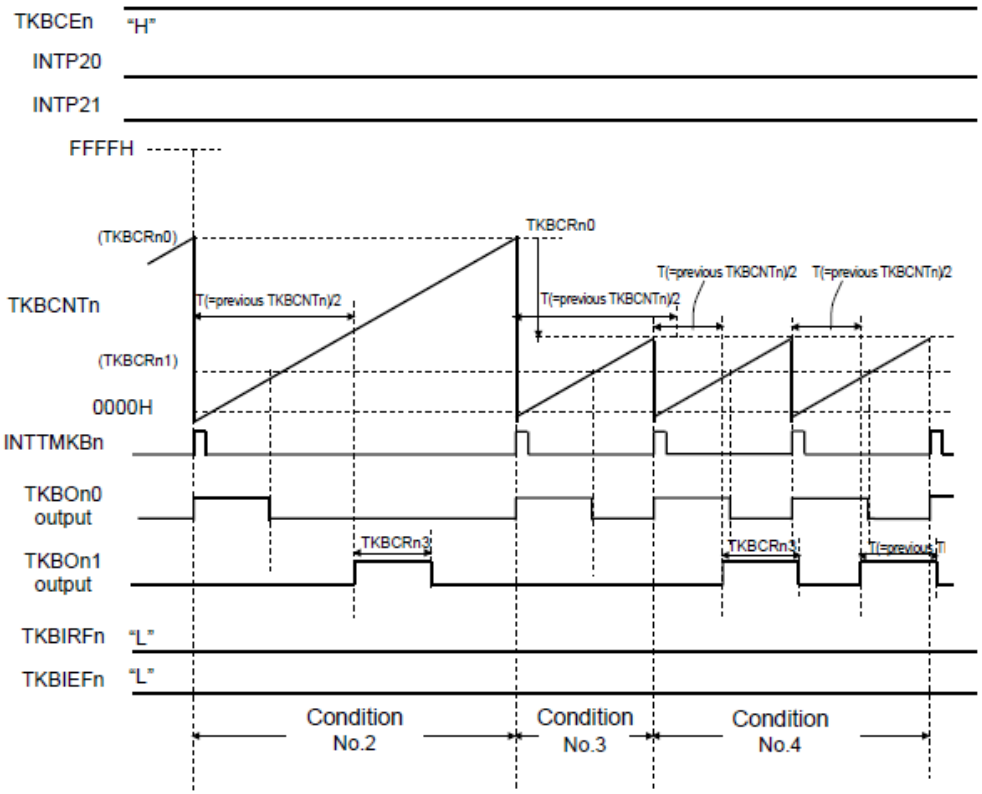


(omitted)

40. 7.4.9 Interleave PFC (Power Factor Correction) output mode Figure 7-51. Figure of Timing of Interleave PFC Mode (Below T/2s No. 3 and No. 4) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))(p.350)

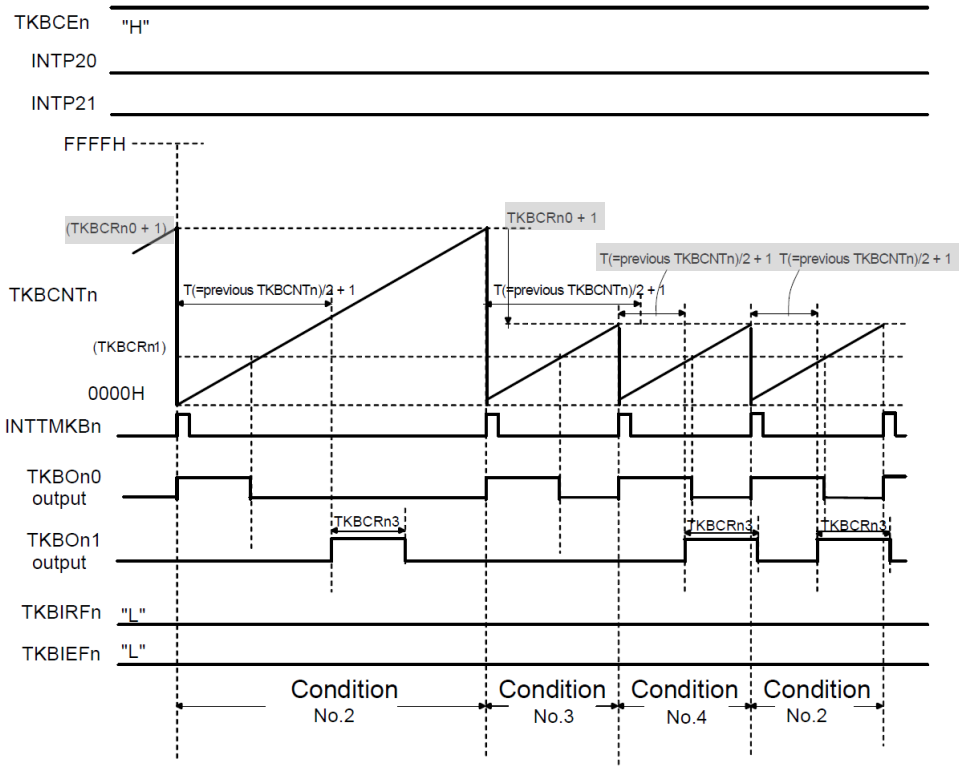
Old)

Figure 7-51. Figure of Timing of Interleave PFC Mode (Below T/2s No. 3 and No. 4) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



New)

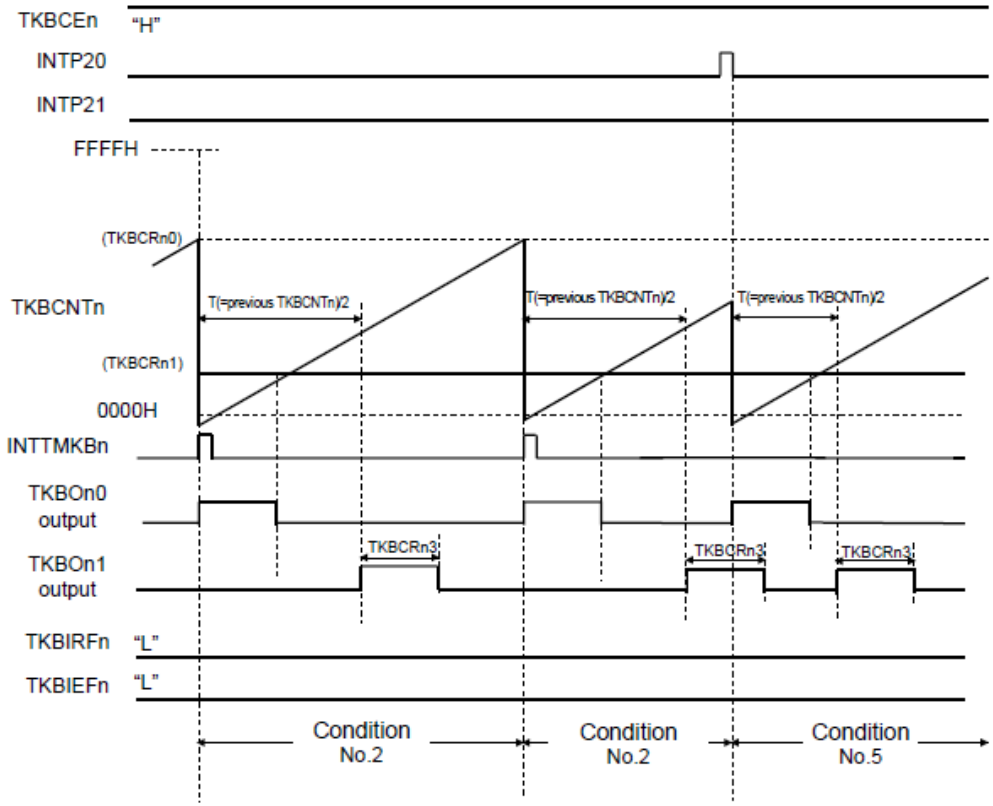
Figure 7-51. Figure of Timing of Interleave PFC Mode (Below T/2s No. 3 and No. 4) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



41. 7.4.9 Interleave PFC (Power Factor Correction) output mode Figure 7-52. Figure of Timing of Interleave PFC Mode (Operation for Condition No. 5: INTP21 not yet Reached)(p.351)

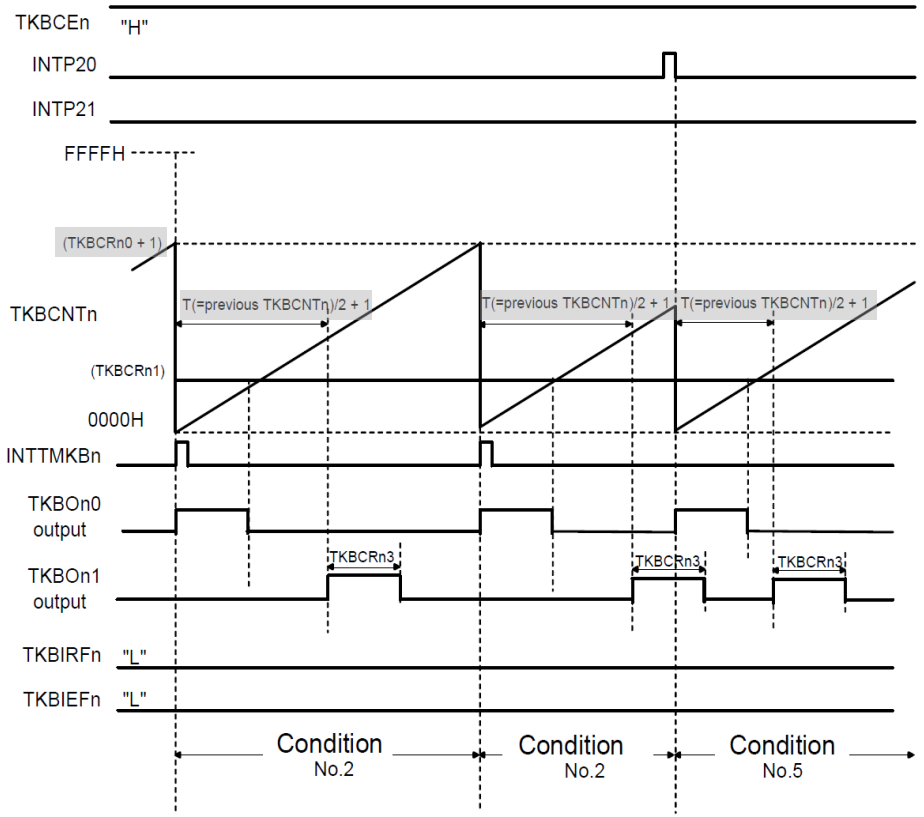
Old)

Figure 7-52. Figure of Timing of Interleave PFC Mode (Operation for Condition No. 5: INTP21 not yet Reached)



New)

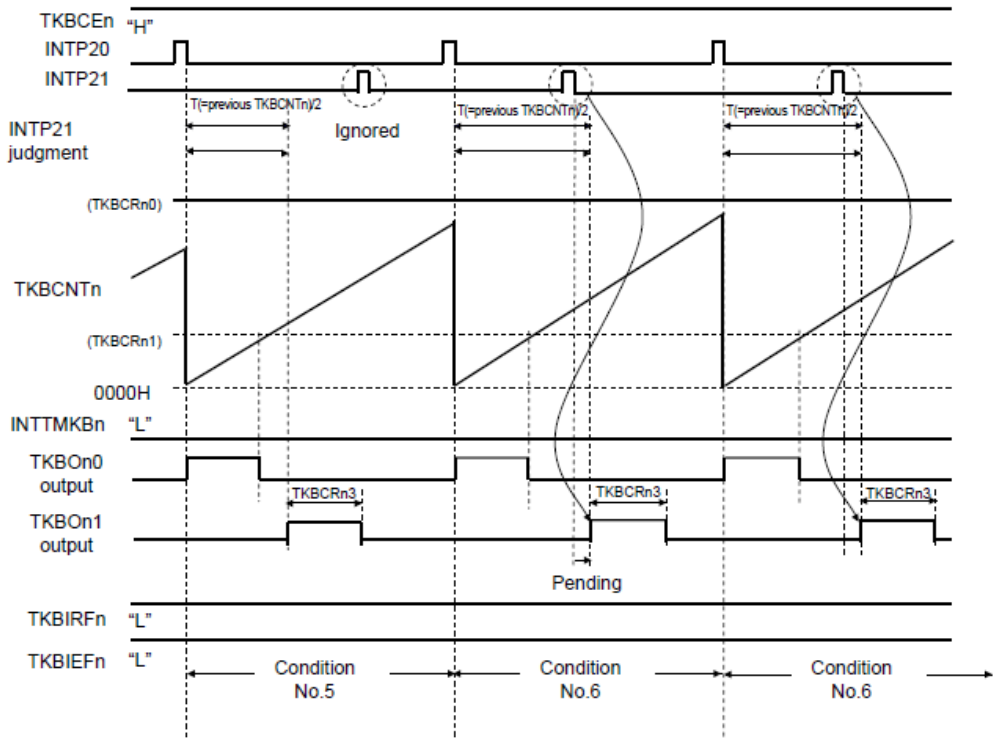
Figure 7-52. Figure of Timing of Interleave PFC Mode (Operation for Condition No. 5)(at Default Value of Output Is Low Level(TKBTODnp=0)and Active Level Is High Level(TKBTOLnp=0))



42. 7.4.9 Interleave PFC (Power Factor Correction) output mode Figure 7-53.Figure of Timing of Interleave PFC Mode (Operation for Conditions No. 6) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))(p.352)

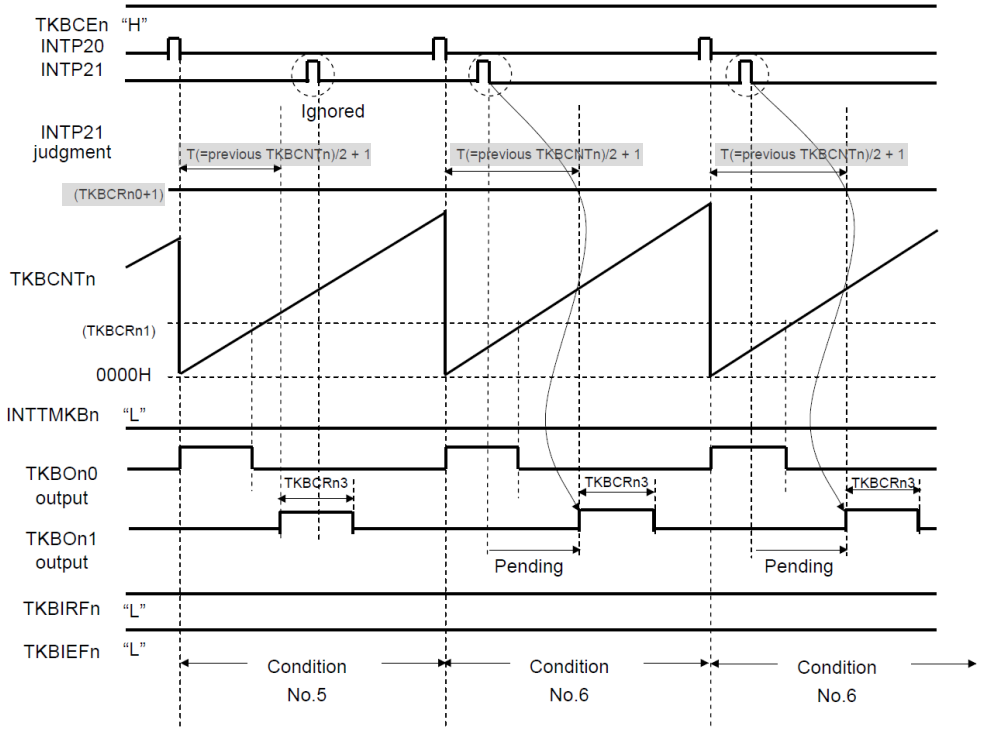
Old)

Figure 7-53. Figure of Timing of Interleave PFC Mode (Operation for Conditions No. 6) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



New)

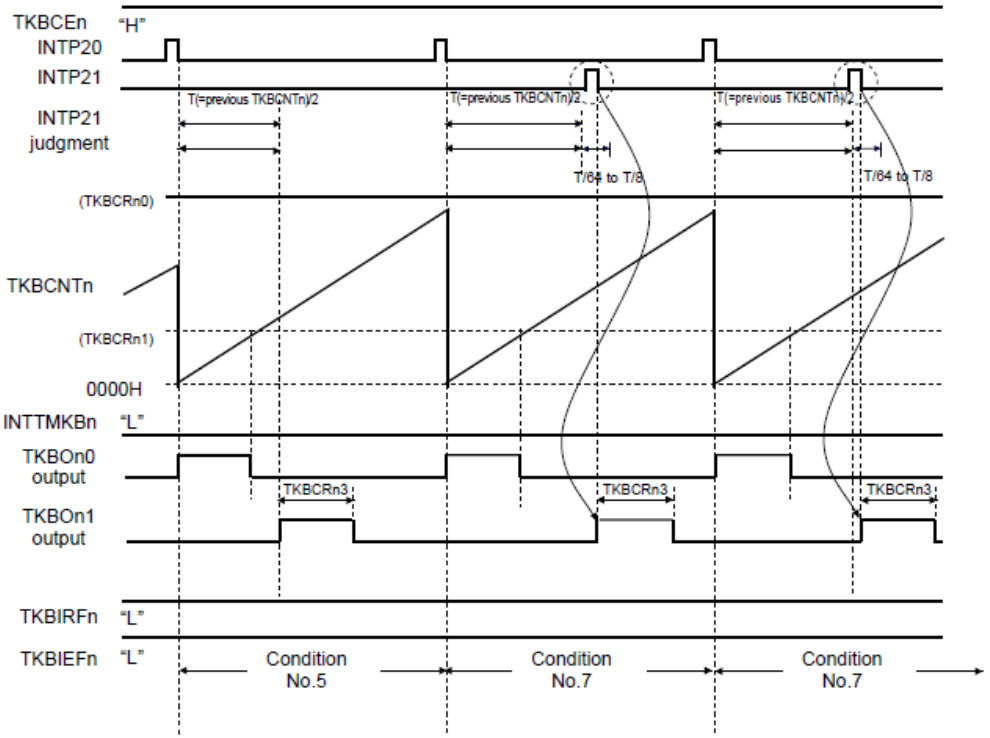
Figure 7-53. Figure of Timing of Interleave PFC Mode (Operation for Conditions No. 6) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



43. 7.4.9 Interleave PFC (Power Factor Correction) output mode Figure7-54.Figure of Timing of Interleave PFC Output Mode (Operation for Conditions No. 7)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))(p.353)

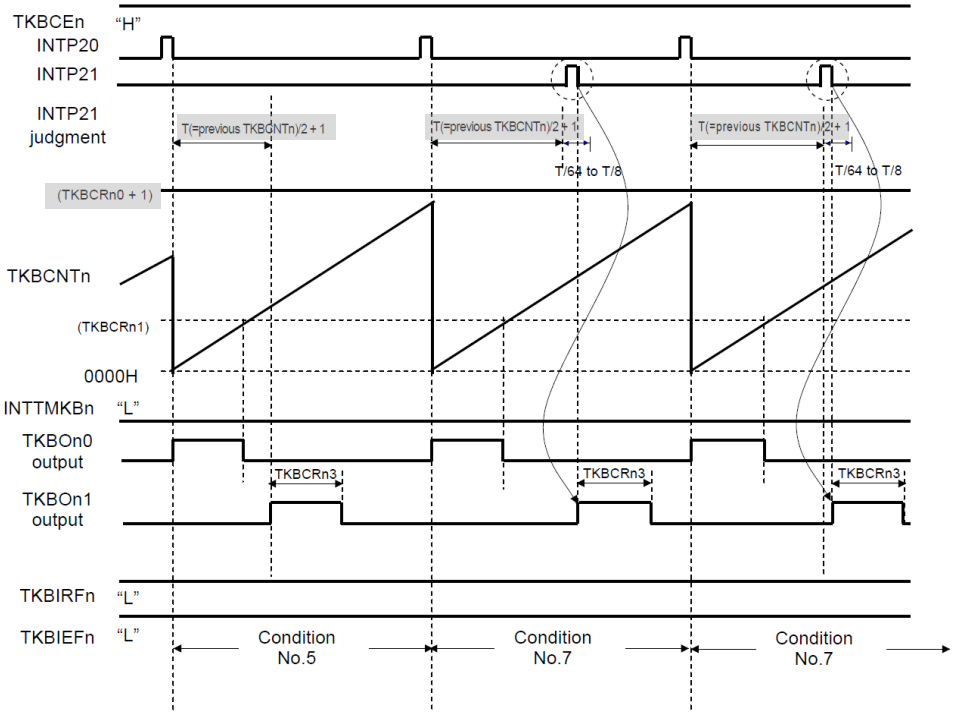
Old)

Figure 7-54. Figure of Timing of Interleave PFC Output Mode (Operation for Conditions No. 7)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



New)

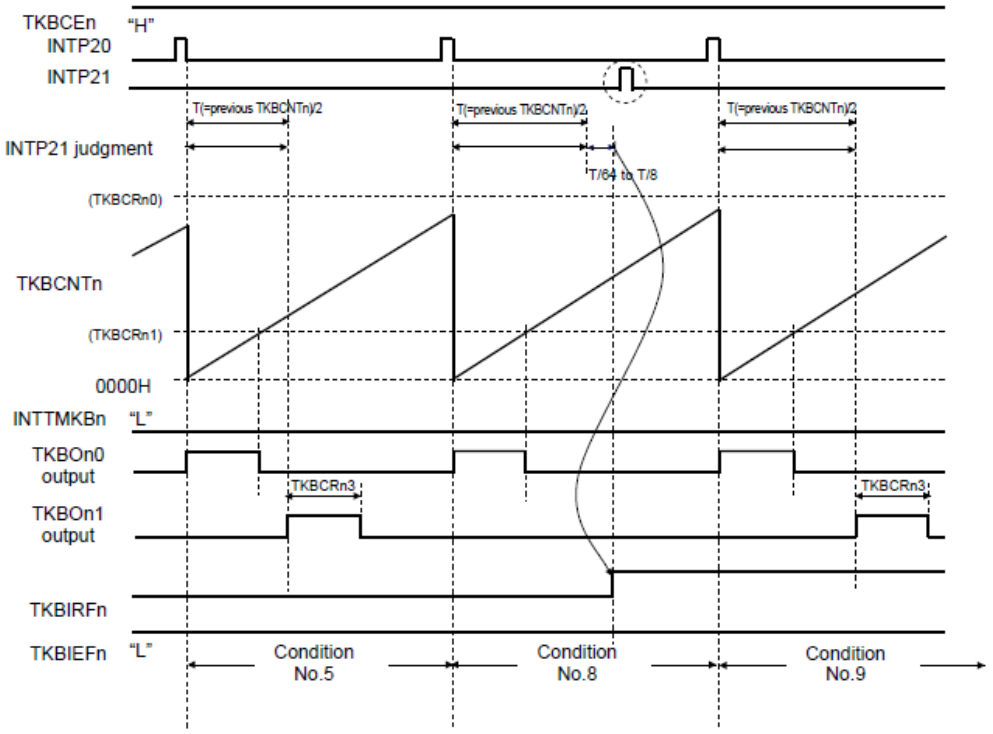
Figure 7-54. Figure of Timing of Interleave PFC Output Mode (Operation for Conditions No. 7)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



44. 7.4.9 Interleave PFC (Power Factor Correction) output mode Figure 7-55.Figure of Timing of Interleave PFC Output Mode (Operation for Conditions No. 8 to 9)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))(p.354)

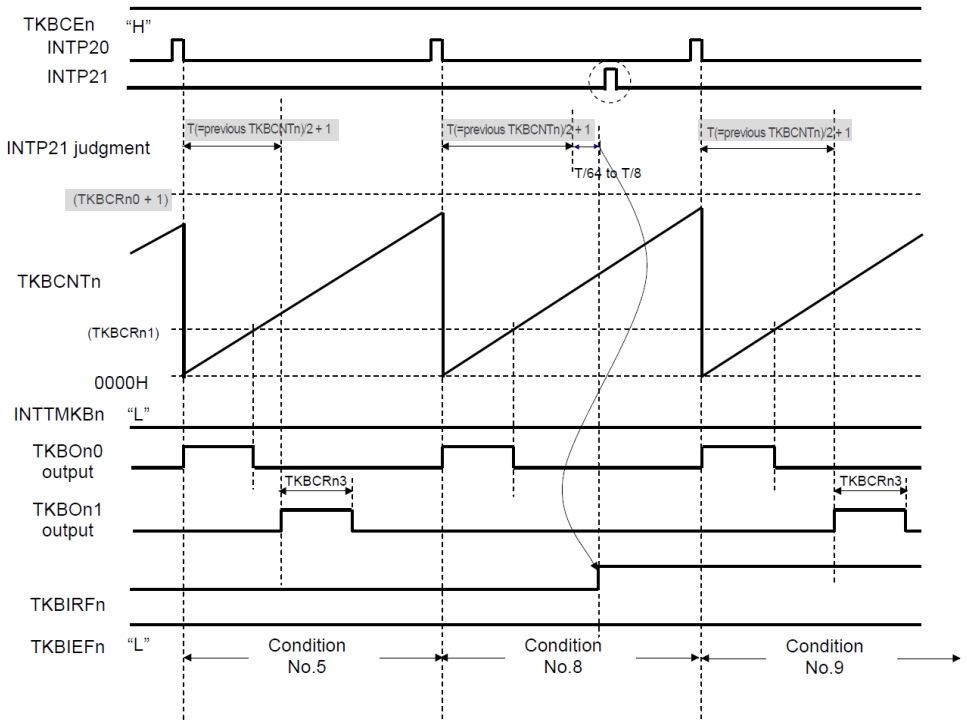
Old)

Figure 7-55. Figure of Timing of Interleave PFC Output Mode (Operation for Conditions No. 8 to 9) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



New)

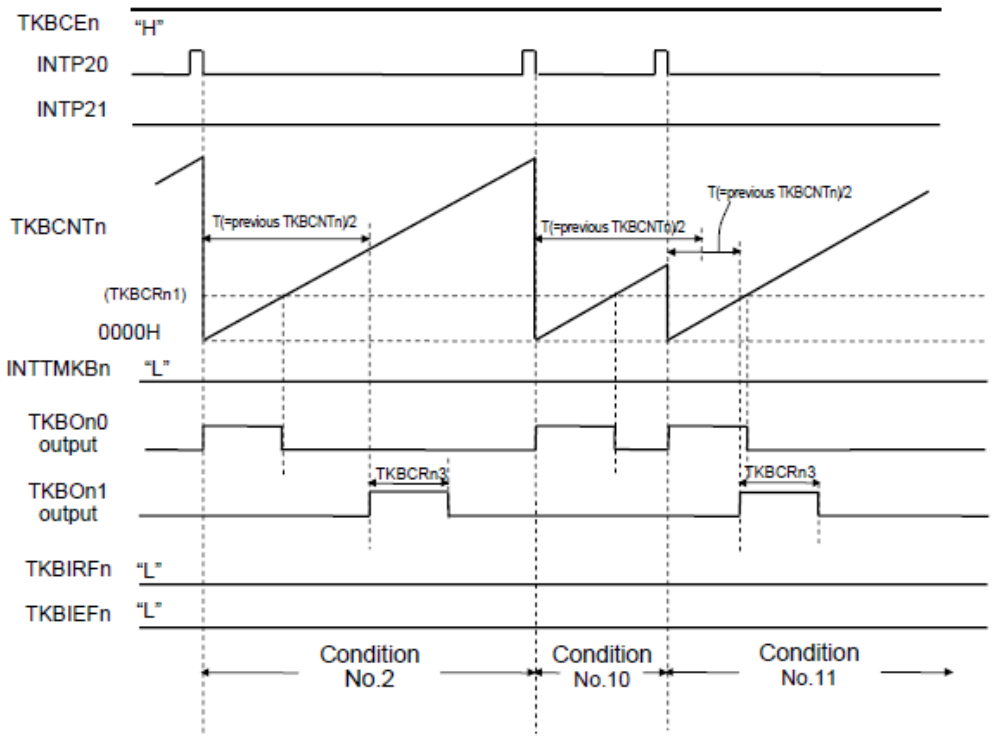
Figure 7-55. Figure of Timing of Interleave PFC Output Mode (Operation for Conditions No. 8 to 9) (at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



45. 7.4.9 Interleave PFC (Power Factor Correction) output mode Figure7-56.Figure of Timing of Interleave PFC Output Mode (Operation for Conditions No. 10 and No. 11)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))(p.355)

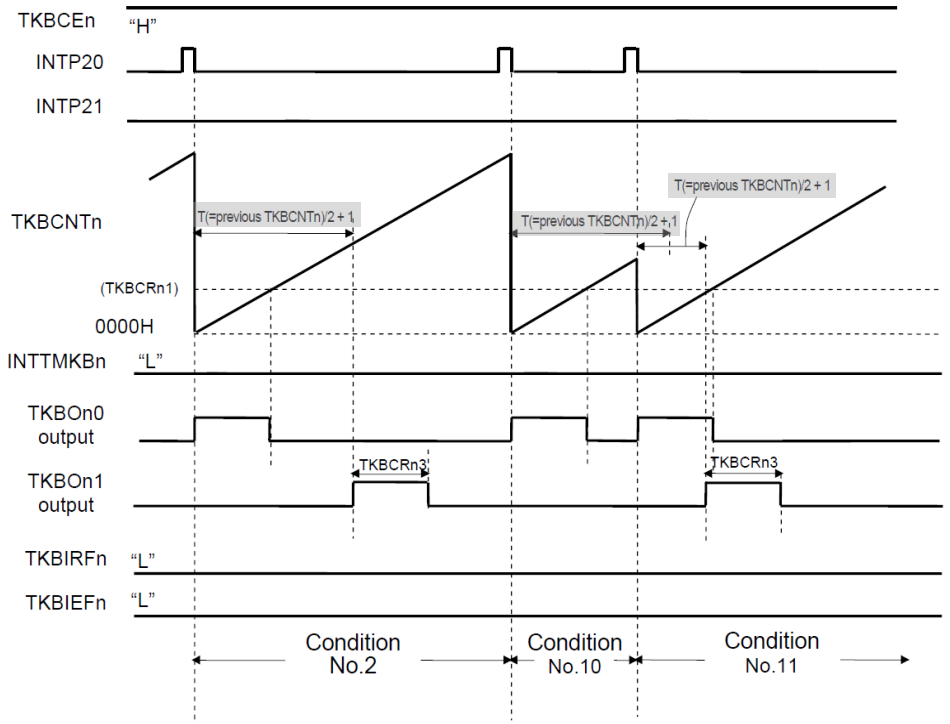
Old)

Figure 7-56. Figure of Timing of Interleave PFC Output Mode (Operation for Conditions No. 10 and No. 11)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



New)

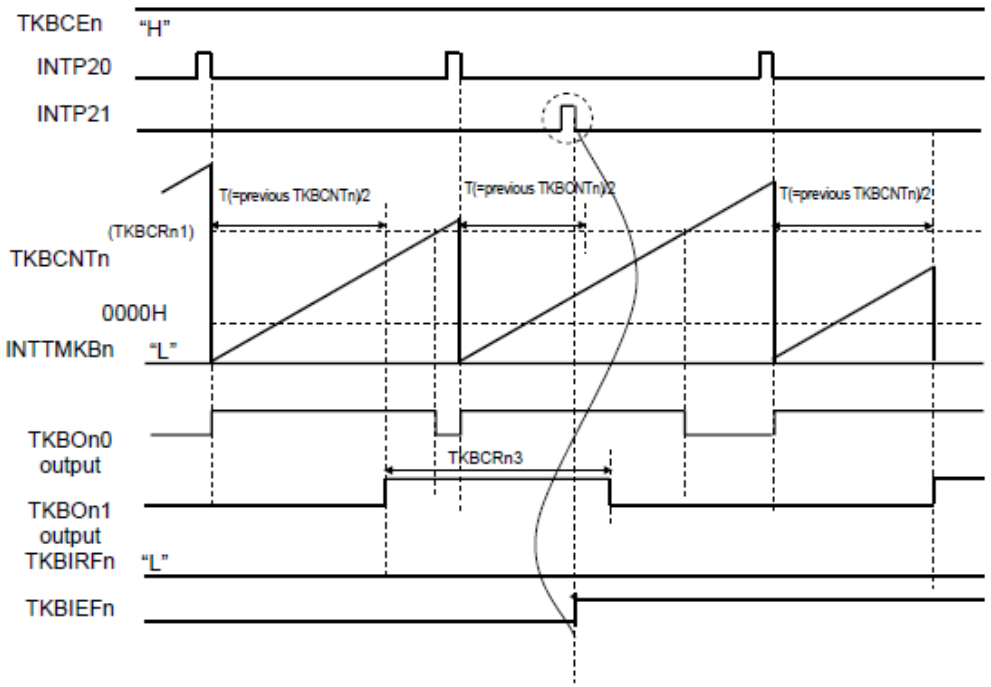
Figure 7-56. Figure of Timing of Interleave PFC Output Mode (Operation for Conditions No. 10 and No. 11)(at Default Value of Output Is Low Level (TKBTODnp = 0) and Active Level Is High Level (TKBTOLnp = 0))



46. 7.4.9 Interleave PFC (Power Factor Correction) output mode Figure 7-57. Figure of Timing of Interleave PFC Output Mode (In Case When Trigger Was Again Generated During TKBOn1)(p.356)

Old)

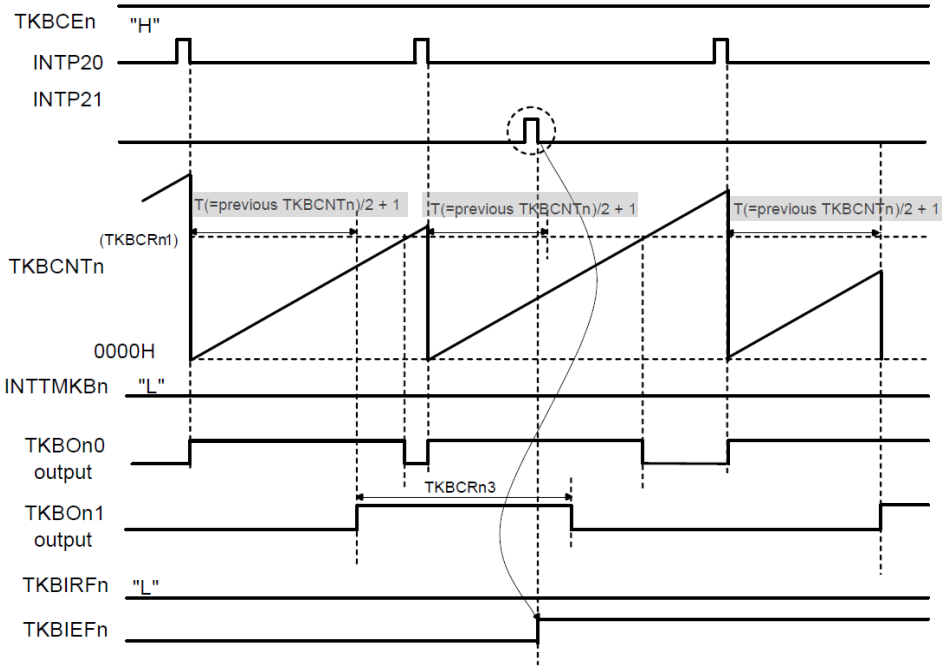
Figure 7-57. Figure of Timing of Interleave PFC Output Mode
(In Case When Trigger Was Again Generated During TKBOn1)



Trigger is ignored when the subsequent TKBOn1 output trigger is generated during the previous TKBOn1 period output. This is when TKBIEFn is set by "1".

New)

Figure 7-57. Figure of Timing of Interleave PFC Output Mode
(In Case When INTP21 Input Was Detected During TKBOn1 Output)



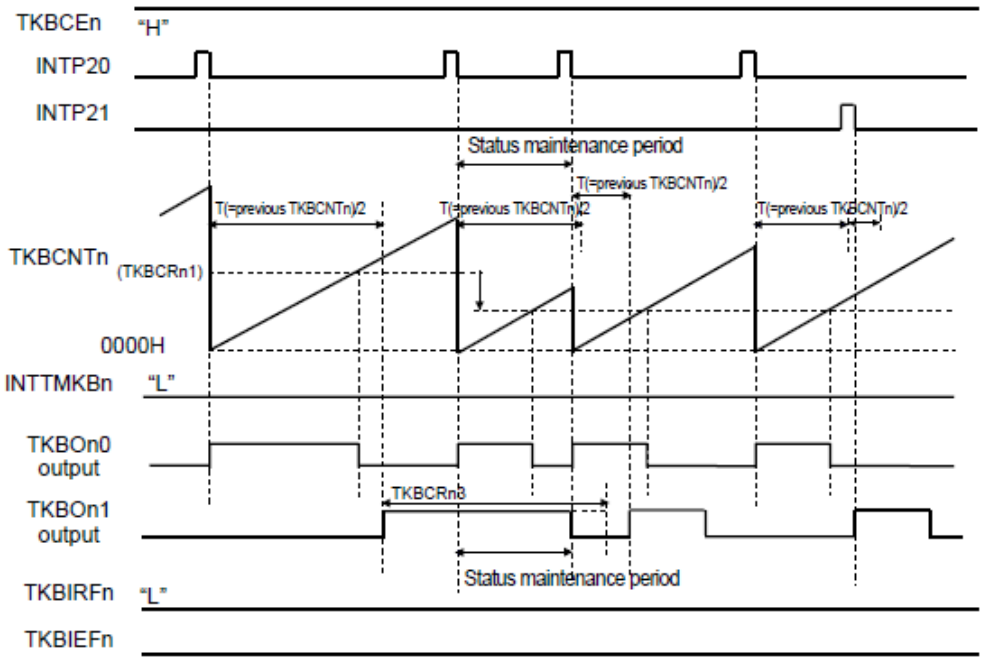
When INTP21 input is detected during TKBOn1 output of the previous period, this trigger is ignored. This is when TKBIEFn is set by "1".

47. 7.4.9 Interleave PFC (Power Factor Correction) output mode

Figure 7-58. Figure of Timing of Interleave PFC Output Mode (Output of TKBOn1 Is at the Width of the Previous Output Width and Exceeds Period of Status Maintenance)(p.357)

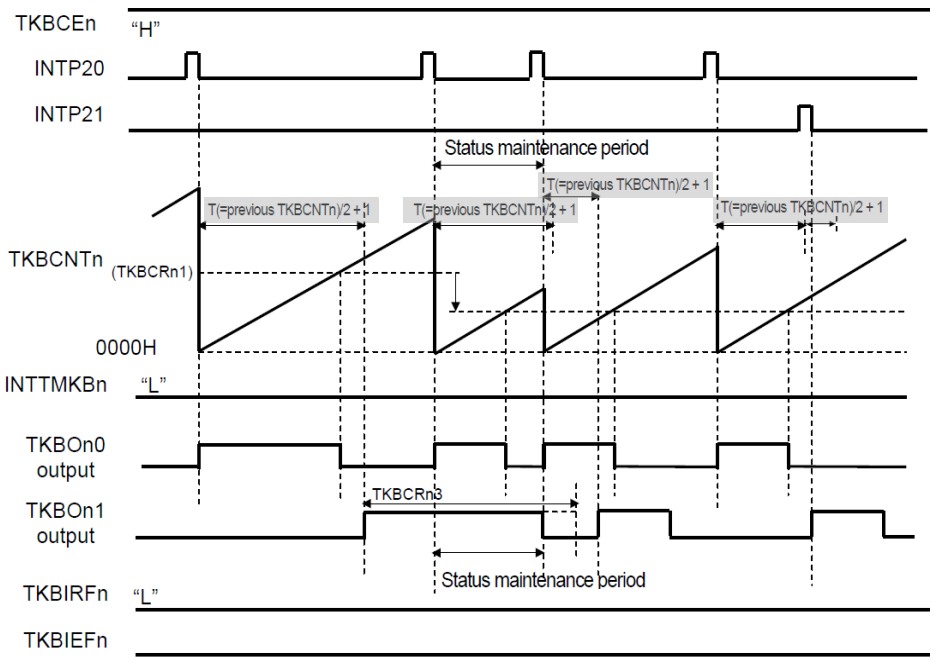
Old)

Figure 7-58. Figure of Timing of Interleave PFC Output Mode
(Output of TKBOn1 Is at the Width of the Previous Output Width and Exceeds Period of Status Maintenance)



New)

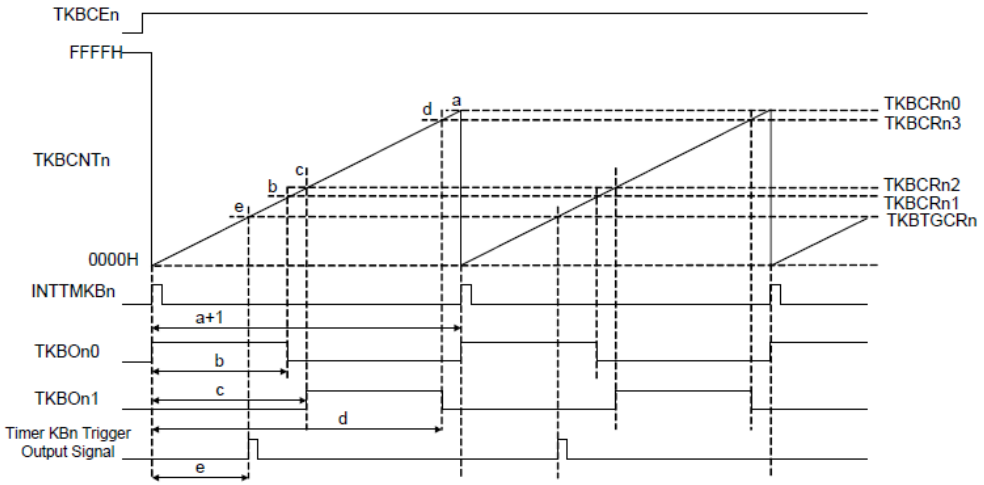
Figure 7-58. Figure of Timing of Interleave PFC Output Mode
(Output of TKBOn1 Is at the Width of the Previous Output Width and Exceeds Period of Status Maintenance)



48. 7.5.1 A/D conversion start timing signal output function Figure 7-59. A/D Conversion Start Timing Signal Output Function for Standalone Mode(Period Controlled by TKB0CR0)

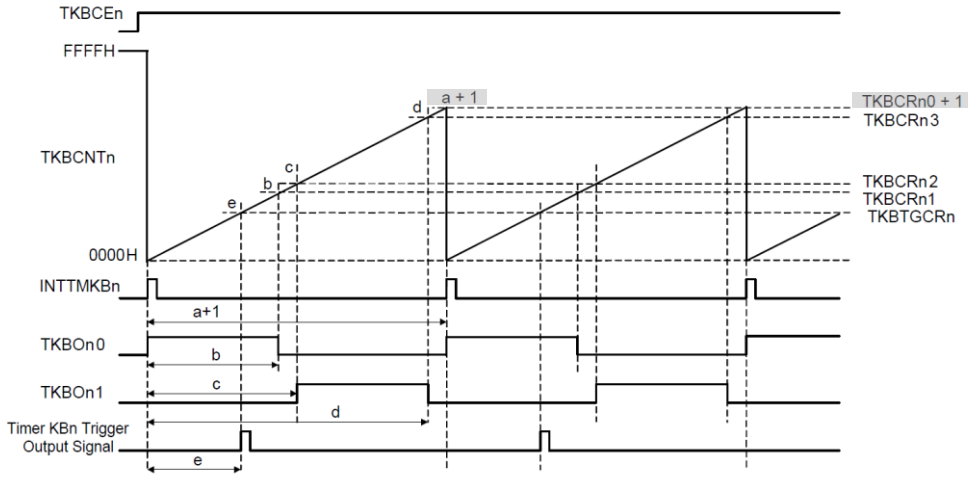
Old)

Figure 7-59. A/D Conversion Start Timing Signal Output Function for Standalone Mode (Period Controlled by TKB0CR0)



New)

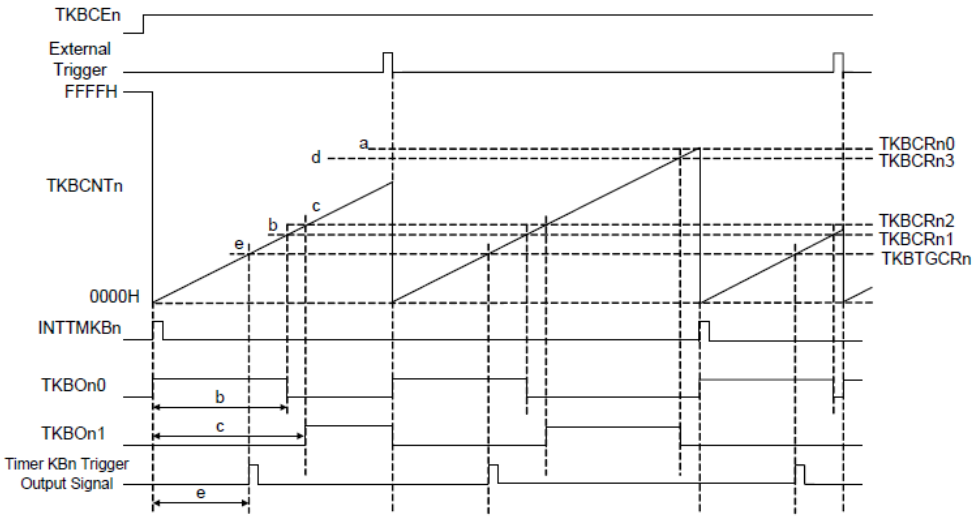
Figure 7-59. A/D Conversion Start Timing Signal Output Function for Standalone Mode (Period Controlled by TKB0CR0)



49. 7.5.1 A/D conversion start timing signal output function Figure 7-60. A/D Conversion Start Timing Signal Output Function for Standalone Mode (Period Controlled by External Trigger Input)(p.361)

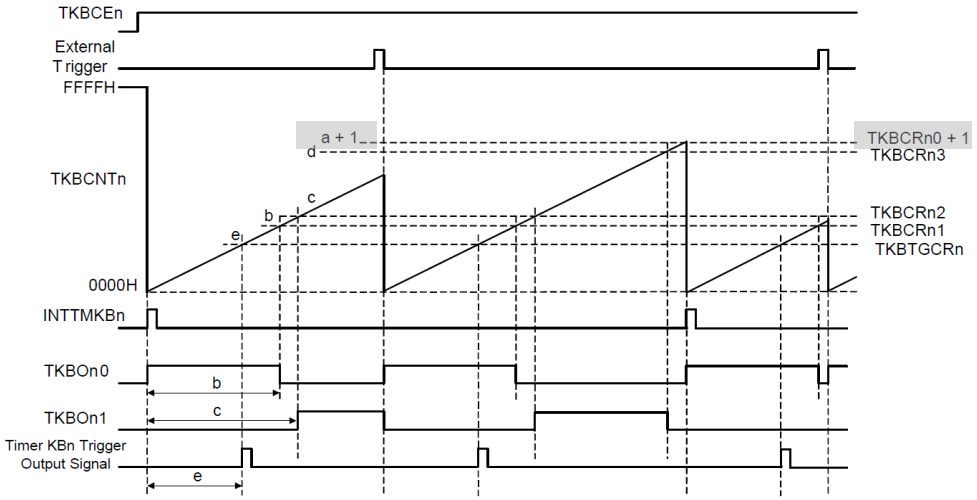
Old)

Figure 7-60. A/D Conversion Start Timing Signal Output Function for Standalone Mode (Period Controlled by External Trigger Input)



New)

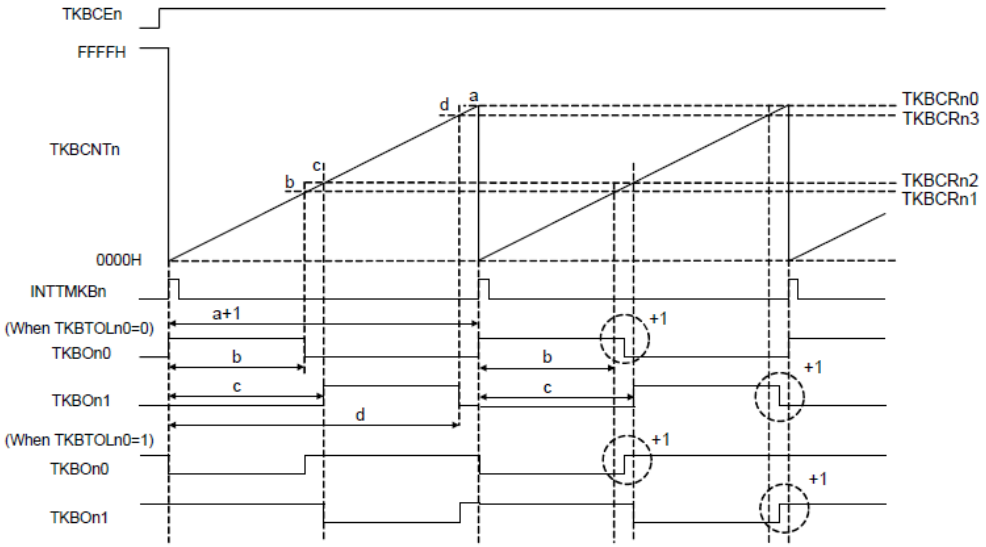
Figure 7-60. A/D Conversion Start Timing Signal Output Function for Standalone Mode (Period Controlled by External Trigger Input)



50. 7.5.2 PWM output dithering function
Figure 7-62. Figure of Waveform at Dithering Operation(p.363)

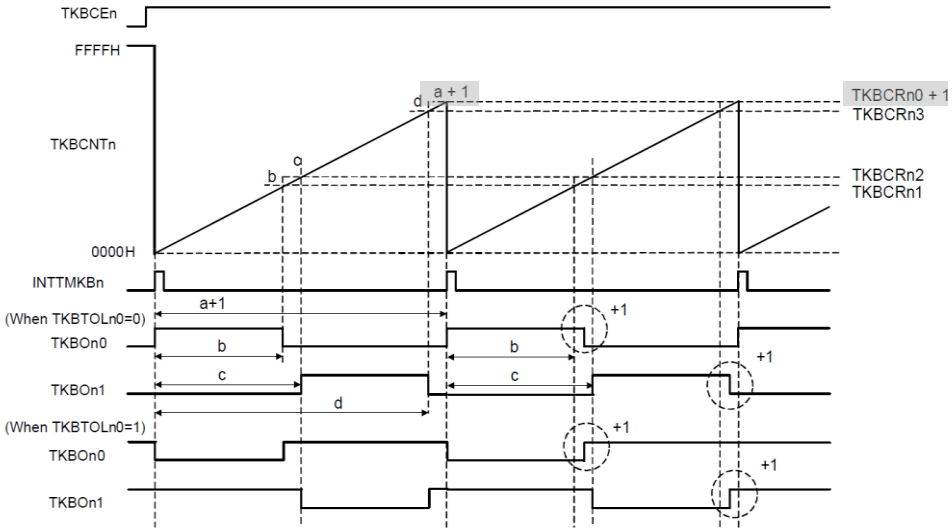
Old)

Figure 7-62. Figure of Waveform at Dithering Operation



New)

Figure 7-62. Figure of Waveform at Dithering Operation

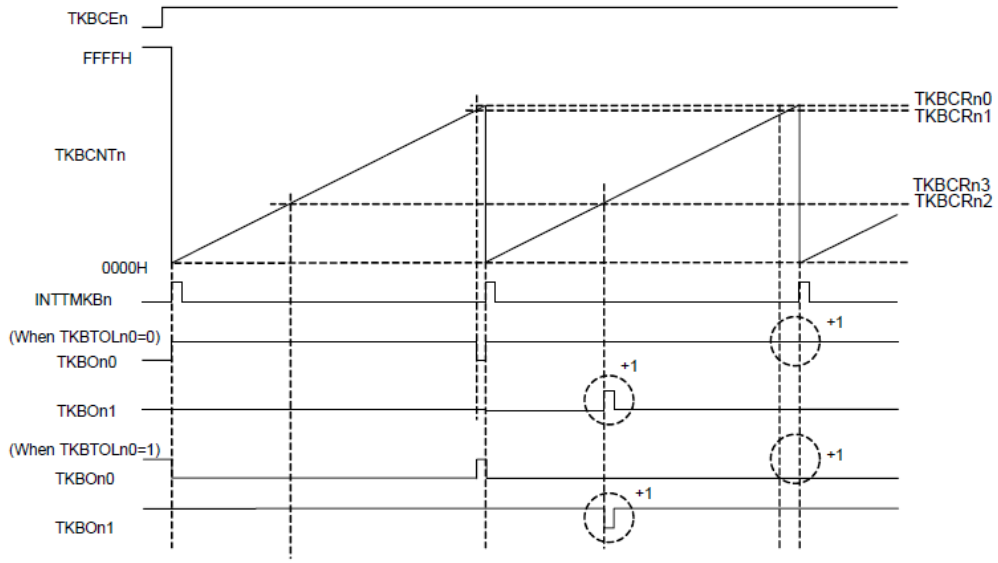


51. 7.5.2 PWM output dithering function

Figure 7-63. Figure of Waveform at Dithering Operation (When TKBCRn1 = TKBCRn0 (100% Nearest Neighbor), TKBCRn2 = TKBCRn3(0% Nearest Neighbor)(p.363)

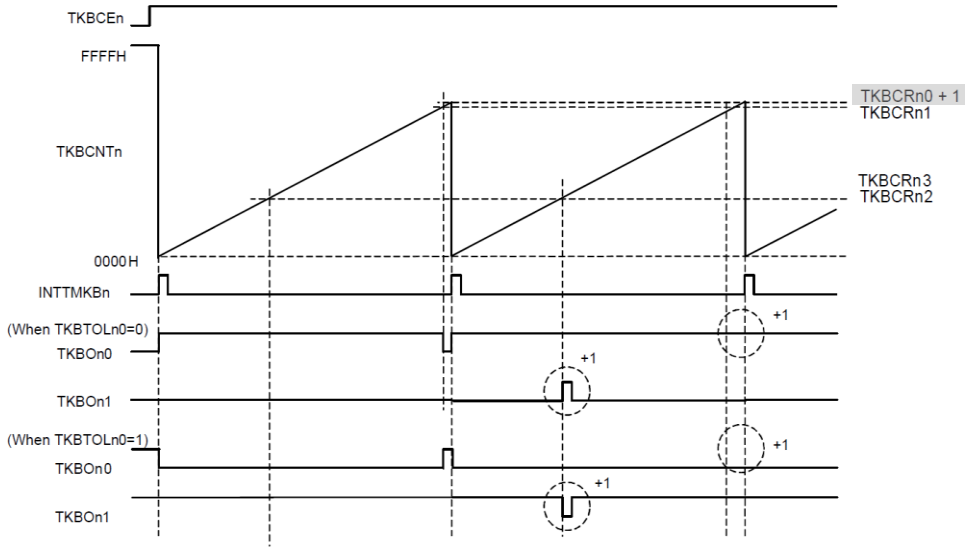
Old)

Figure 7-63. Figure of Waveform at Dithering Operation
(When TKBCRn1 = TKBCRn0 (100% Nearest Neighbor), TKBCRn2 = TKBCRn3(0% Nearest Neighbor)



New)

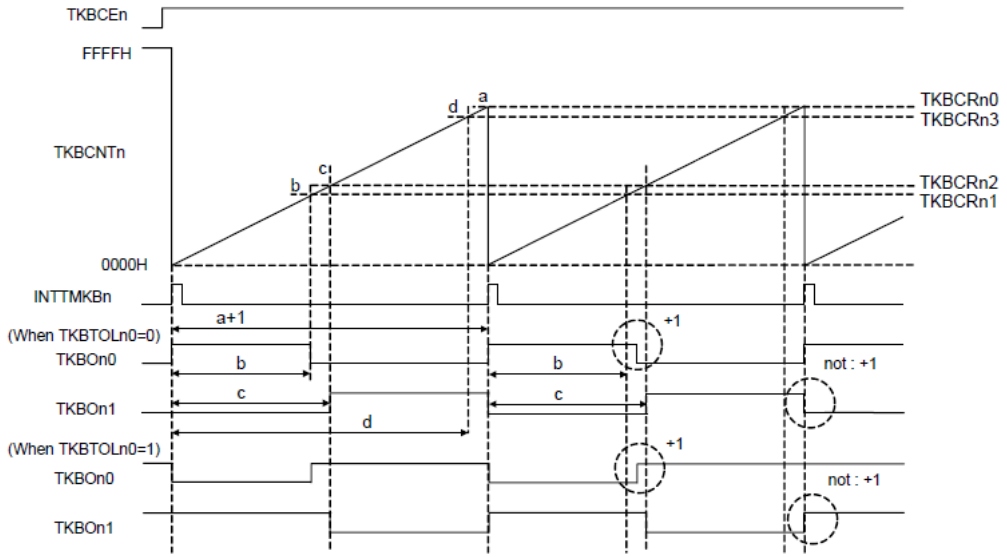
Figure 7-63. Figure of Waveform at Dithering Operation
(When TKBCRn1 = TKBCRn0 (100% Nearest Neighbor), TKBCRn2 = TKBCRn3(0% Nearest Neighbor)



52. 7.5.2 PWM output dithering function
Figure 7-64. Figure of Waveform at Dithering Operation (When TKBCRn3 = TKBCRn0+1)(p.364)

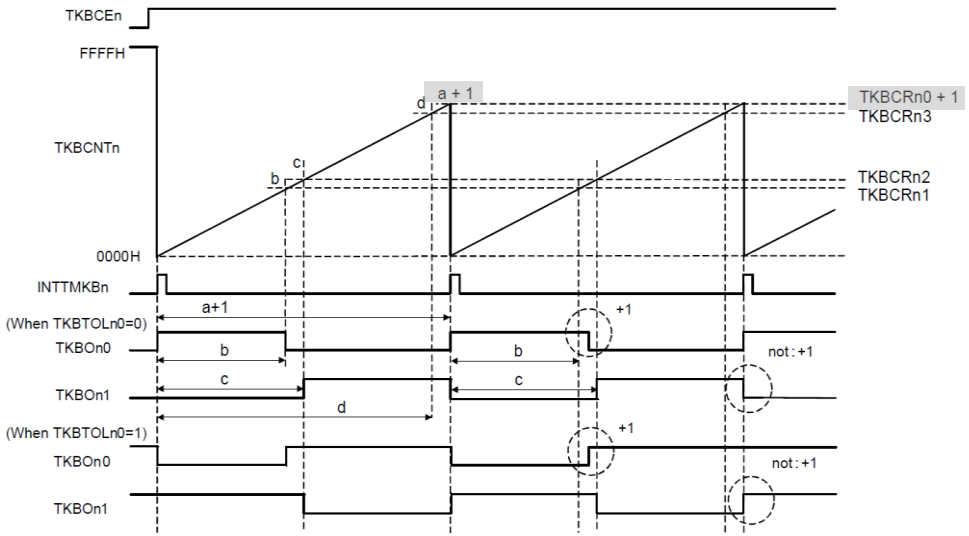
Old)

Figure 7-64. Figure of Waveform at Dithering Operation
(When TKBCRn3 = TKBCRn0+1)



New)

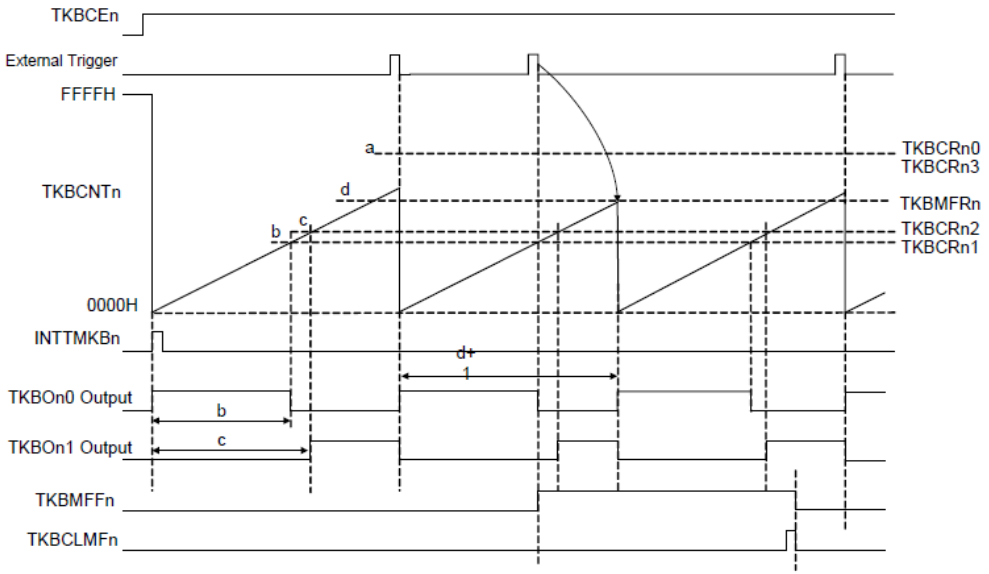
Figure 7-64. Figure of Waveform at Dithering Operation
(When TKBCRn3 = TKBCRn0+1)



53. 7.5.6 Maximum frequency limit function
Figure 7-70. Maximum Frequency Limit Function(p.373)

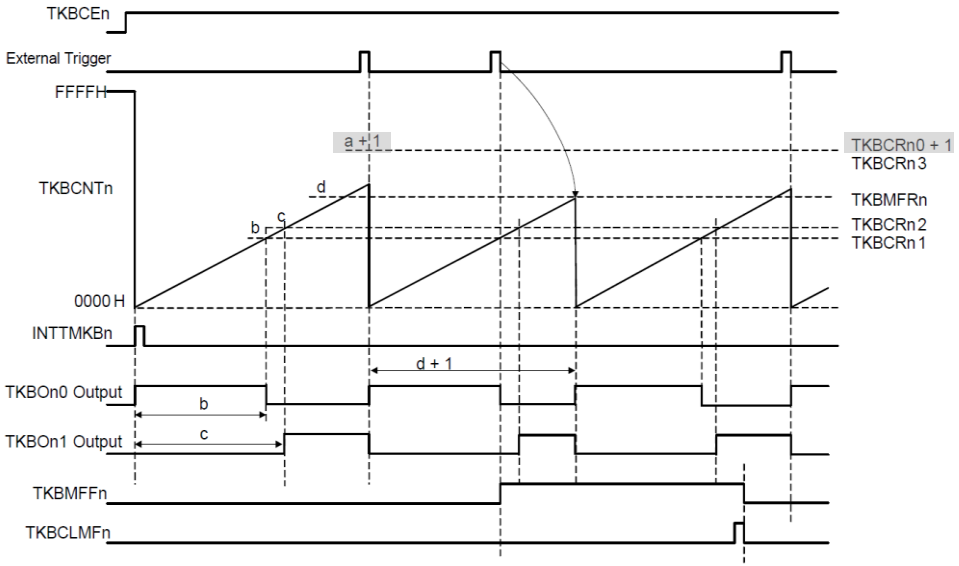
Old)

Figure 7-70. Maximum Frequency Limit Function



New)

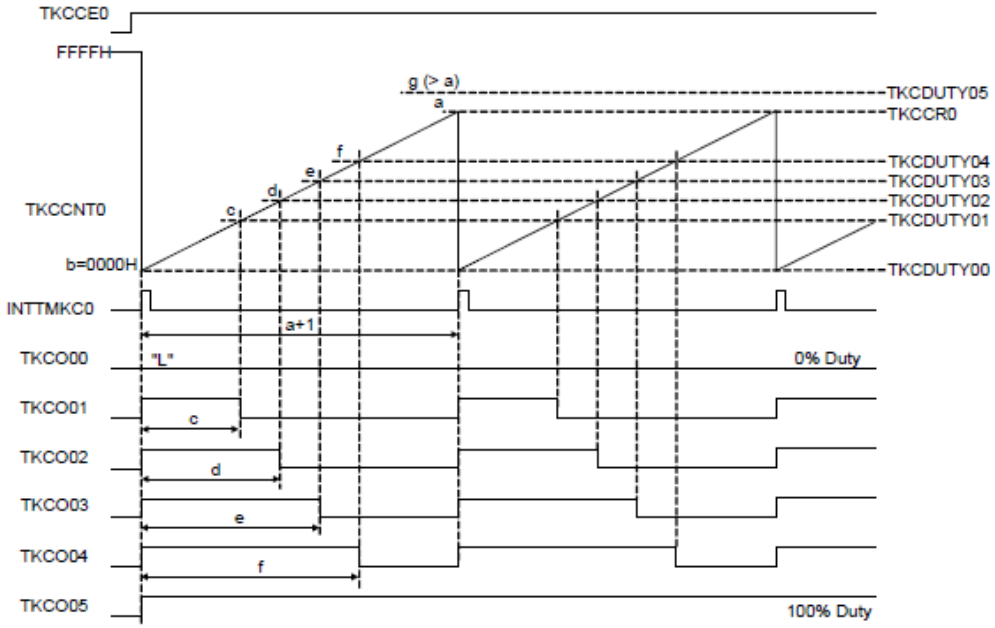
Figure 7-70. Maximum Frequency Limit Function



54. 8.4.1 PWM output function
Figure 8-17.Basic Timing Sample(at TKCTOL0m=0,TKCTOD0m = 0) for PWM Output Function(p.412)

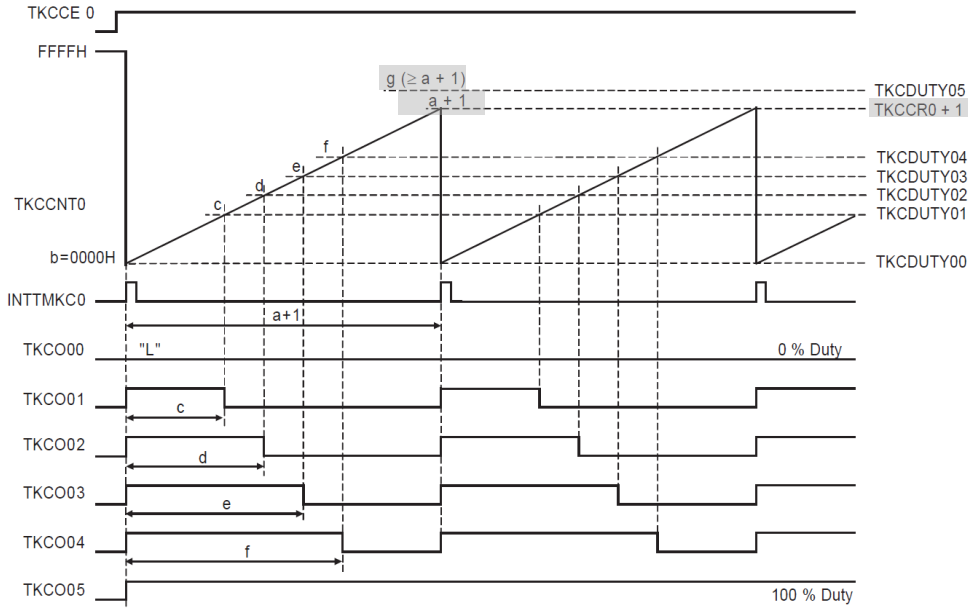
Old)

Figure 8-17.Basic Timing Sample(at TKCTOL0m=0,TKCTOD0m = 0)for PWM Output Function



New)

Figure 8-17.Basic Timing Sample(at TKCTOL0m=0,TKCTOD0m = 0)for PWM Output Function



55. 10.2 Configuration of 12-bit Interval Timer(p.446)

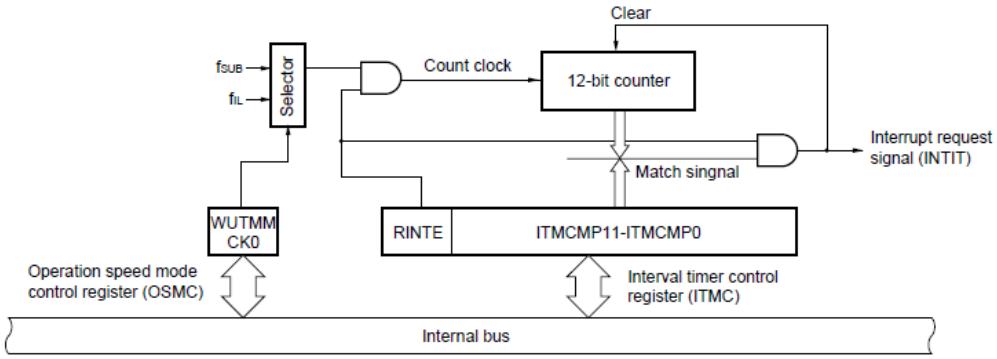
Old)

The 12-bit interval timer includes the following hardware.

Table 10-1. Configuration of 12-bit Interval Timer

Item	Configuration
Counter	12-bit counter
Control registers	Peripheral enable register 0 (PER0)
	Operation speed mode control register (OSMC)
	Interval timer control register (ITMC)

Figure 10-1. Block Diagram of 12-bit Interval Timer



Caution The subsystem clock (f_{SUB}) can be selected as the operating clock only for 38-pin products.

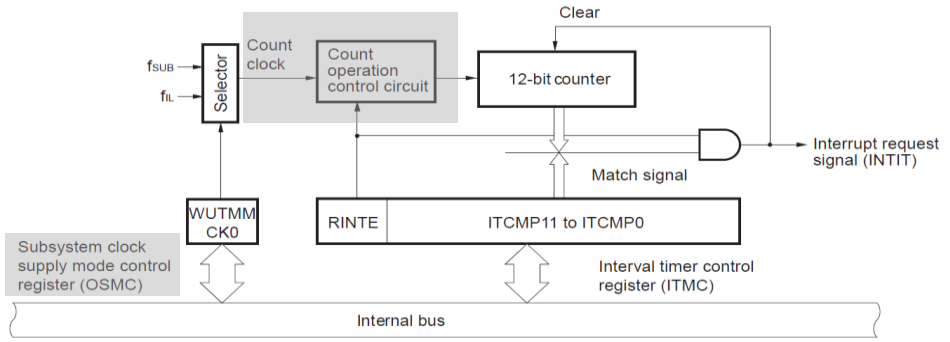
New)

The 12-bit interval timer includes the following hardware.

Table 10-1. Configuration of 12-bit Interval Timer

Item	Configuration
Counter	12-bit counter
Control registers	Peripheral enable register 0 (PER0)
	Subsystem clock supply mode control register (OSMC)
	Interval timer control register (ITMC)

Figure 10-1. Block Diagram of 12-bit Interval Timer



Caution The subsystem clock (f_{SUB}) can be selected as the count clock only for 38-pin products.

56. 11.4.3 Setting window open period of watchdog timer(p.457)

Old)

(omitted)

Remark If the overflow time is set to $2^9/f_{IL}$, the window close time and open time are as follows.

	Setting of Window Open Period		
	50%	75% + 1/2f_{IL}	100%
Window close time	0 to 20.08 ms	0 to 10.04 ms	None
Window open time	20.08 to 29.68 ms	10.04 to 29.68 ms	0 to 29.68 ms

(omitted)

New)

(omitted)

Remark If the overflow time is set to $2^9/f_{IL}$, the window close time and open time are as follows.

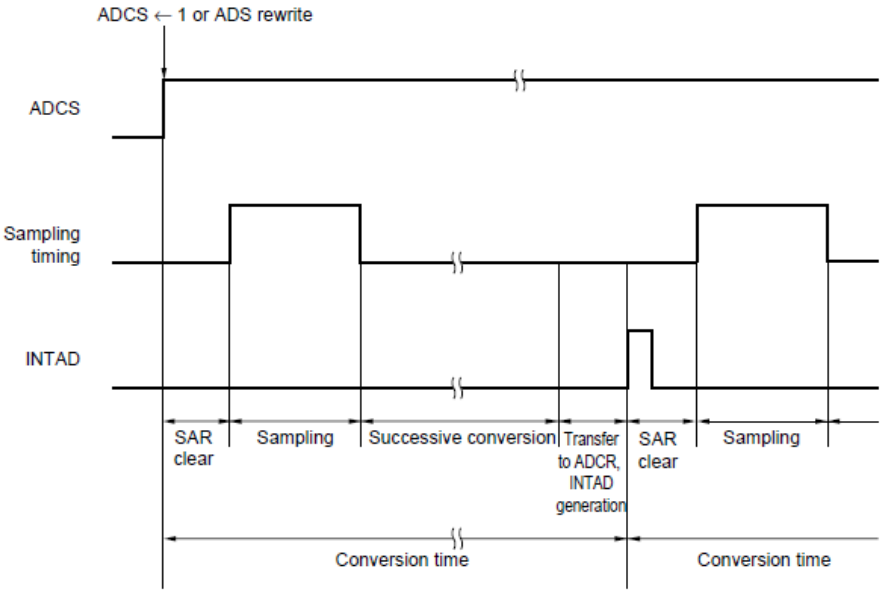
	Setting of Window Open Period		
	50%	75%	100%
Window close time	0 to 20.08 ms	0 to 10.04 ms	None
Window open time	20.08 to 29.68 ms	10.04 to 29.68 ms	0 to 29.68 ms

(omitted)

57. 12.3.2 A/D converter mode register 0 (ADM0)(p.472)

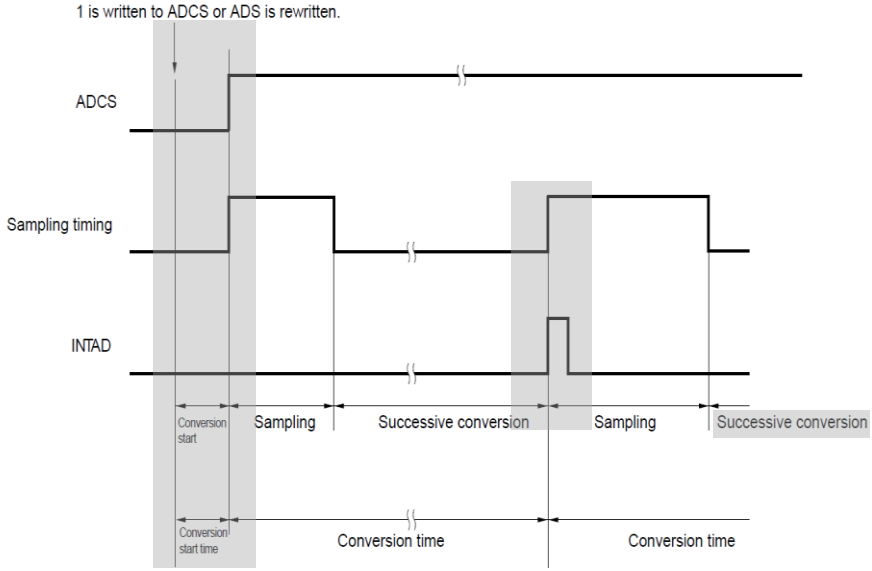
Old)

Figure 12-5. A/D Converter Sampling and A/D Conversion Timing (Example for Software Trigger Mode)



New)

Figure 12-5. A/D Converter Sampling and A/D Conversion Timing (Example for Software Trigger Mode)



58. 12.3.9 Conversion result comparison lower limit setting register (ADLL)(p.479)

Old)

This register is used to specify the setting for checking the lower limit of the A/D conversion results.

The A/D conversion results and ADLL register value are compared, and interrupt signal (INTAD) generation is controlled in the range specified for the ADRCK bit of A/D converter mode register 2 (ADM2) (shown in **Figure 12-8**).

The ADLL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 12-13. Format of Conversion Result Comparison Lower Limit Setting Register (ADLL)

Address: F0012H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADLL	ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0

Caution When 10-bit resolution A/D conversion is selected, the higher eight bits of the 10-bit A/D conversion result register (ADCR) are compared with the ADLL register.

New)

This register is used to specify the setting for checking the lower limit of the A/D conversion results.

The A/D conversion results and ADLL register value are compared, and interrupt signal (INTAD) generation is controlled in the range specified for the ADRCK bit of A/D converter mode register 2 (ADM2) (shown in **Figure 12-8**).

The ADLL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 12-13. Format of Conversion Result Comparison Lower Limit Setting Register (ADLL)

Address: F0012H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADLL	ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0

Caution 1. When 10-bit resolution A/D conversion is selected, the higher eight bits of the 10-bit A/D conversion result register (ADCR) are compared with the ADLL register.

2. Only write new values to the ADUL and ADLL registers while conversion is stopped (ADCS = 0, ADCE = 0).

3. The setting of the ADUL registers must be greater than that of the ADLL register.

59. 12.3.10 A/D test register (ADTES)(p.480)

Old)

This register is used to select the + side reference voltage (AV_{REFP}) or – side reference voltage (AV_{REFM}) of the A/D converter, the analog input channel (ANIxx), or the PGAOUT as the A/D conversion target for the A/D test function.

The ADTES register can be set by an 8-bit memory manipulation instruction.
Reset signal generation clears this register to 00H.

Figure 12-14. Format of A/D Test Register (ADTES)

Address: F0013H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTES	0	0	0	0	0	0	ADTES1	ADTES0

ADTES1	ADTES0	A/D conversion target
0	0	ANIxx, PGAOUT (This is specified using the analog input channel specification register (ADS).)
1	0	AV_{REFM}
1	1	AV_{REFP}
Other than above		Setting prohibited

Caution For details of the A/D test function, see CHAPTER 25 SAFETY FUNCTIONS.

New)

This register is used to select the + side reference voltage or – side reference voltage for the converter, an analog input channel (ANIxx), the temperature sensor output voltage, the internal reference voltage (1.45 V), or PGAOUT as the target for A/D conversion.

When using this register to test the converter, set as follows.

- For zero-scale measurement, select the – side reference voltage as the target for conversion.
- For full-scale measurement, select the + side reference voltage as the target for conversion.

The ADTES register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 12-14. Format of A/D Test Register (ADTES)

Address: F0013H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTES	0	0	0	0	0	0	ADTES1	ADTES0

ADTES1	ADTES0	A/D conversion target
0	0	ANIxx/temperature sensor output voltage[Note] /internal reference voltage (1.45 V)[Note]/ PGAOUT (This is specified using the analog input channel specification register (ADS).)
1	0	The – side reference voltage (selected by the ADREFM bit of the ADM2 register)
1	1	The + side reference voltage (selected by the ADREFP1 or ADREFP0 bit of the ADM2 register)
Other than above		Setting prohibited

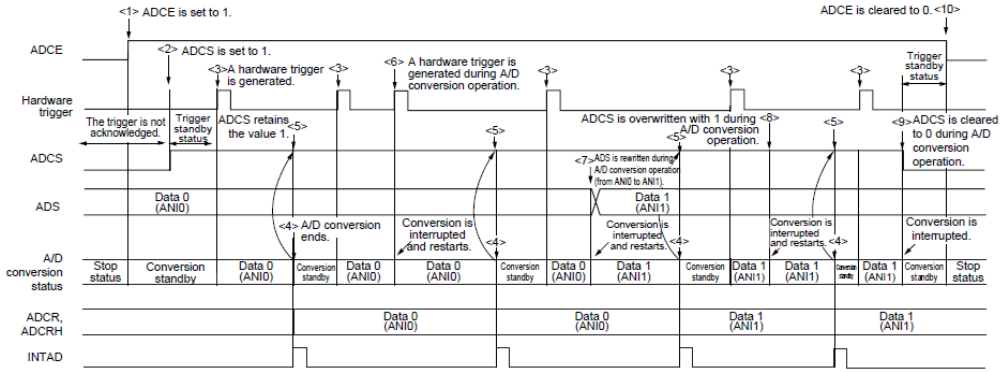
Note The temperature sensor output voltage and internal reference voltage (1.45 V) can be selected only in the HS (high-speed main) mode.

60. 12.6.6 Hardware trigger no-wait mode (select mode, one-shot conversion mode)(p.493)

Old)

(omitted)

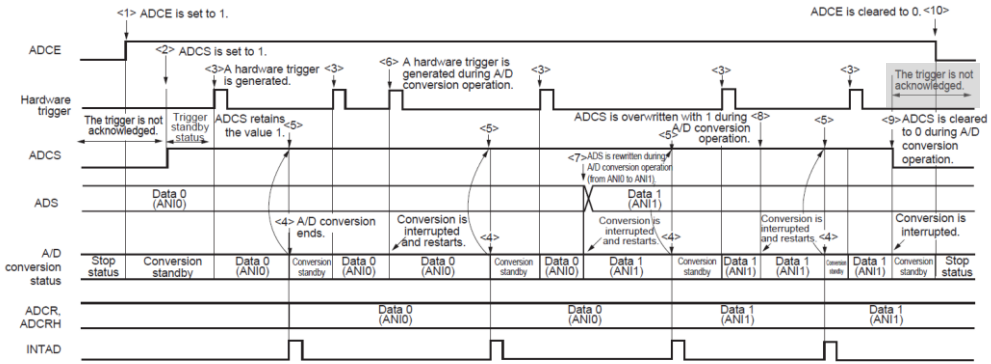
Figure 12-25. Example of Hardware Trigger No-wait Mode
(Select Mode, One-shot Conversion Mode) Operation Timing



New)

(omitted)

Figure 12-25. Example of Hardware Trigger No-wait Mode
(Select Mode, One-shot Conversion Mode) Operation Timing

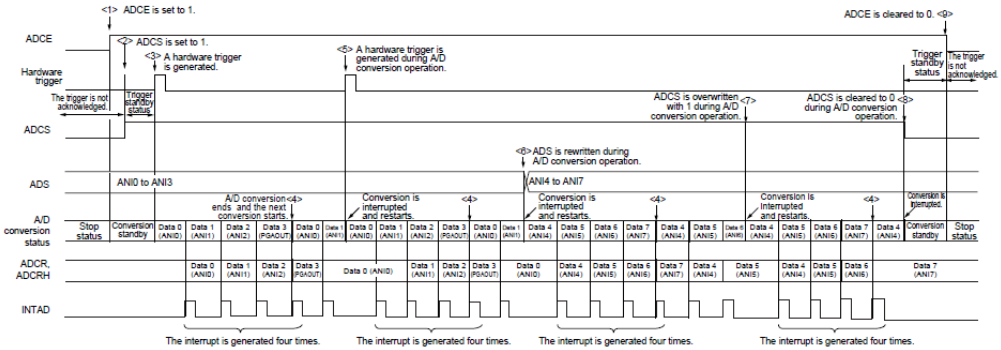


61. 12.6.7 Hardware trigger no-wait mode (scan mode, sequential conversion mode)(p.494)

Old)

(omitted)

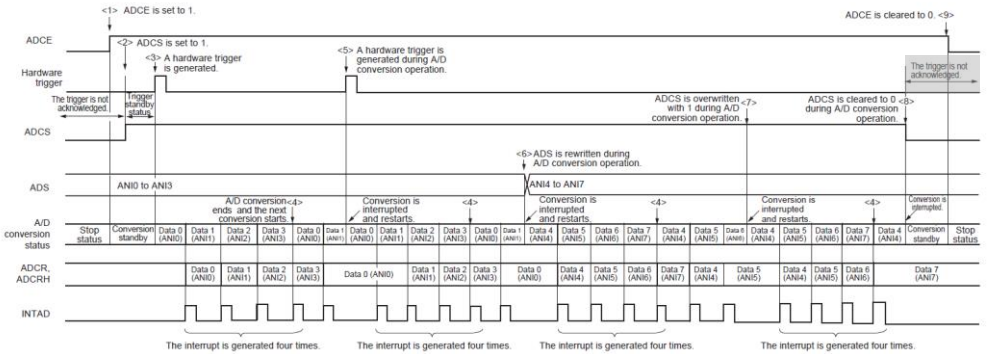
Figure 12-26. Example of Hardware Trigger No-wait Mode
(Scan Mode, Sequential Conversion Mode) Operation Timing



New)

(omitted)

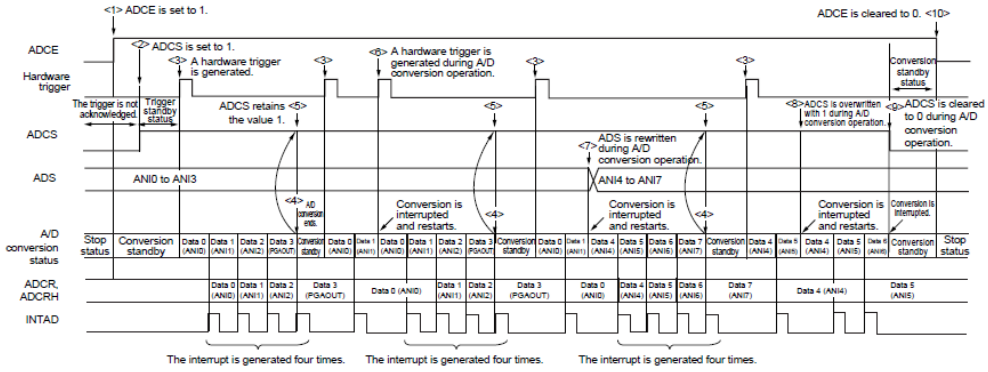
Figure 12-26. Example of Hardware Trigger No-wait Mode
(Scan Mode, Sequential Conversion Mode) Operation Timing



62. 12.6.8 Hardware trigger no-wait mode (scan mode, one-shot conversion mode)(p.495)

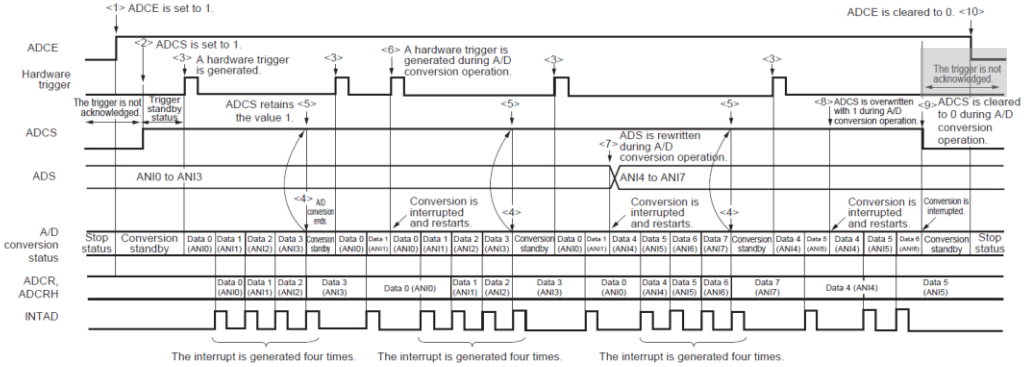
Old)

Figure 12-27. Example of Hardware Trigger No-wait Mode (Scan Mode, One-shot Conversion Mode) Operation Timing



New)

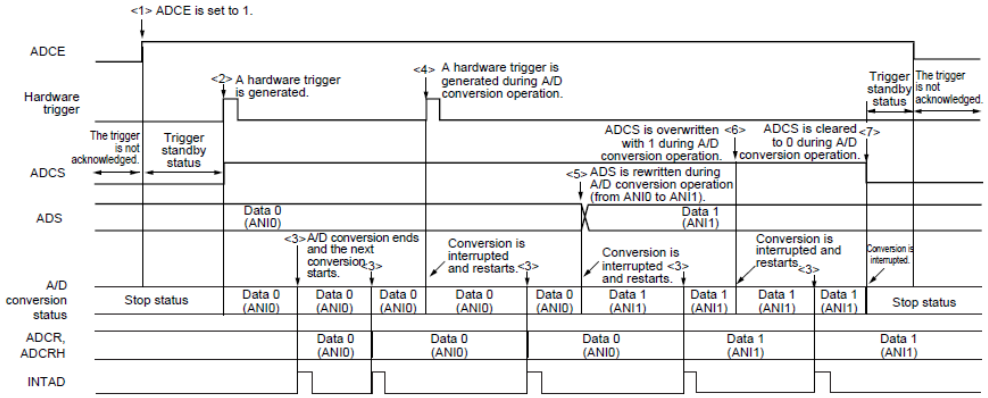
Figure 12-27. Example of Hardware Trigger No-wait Mode (Scan Mode, One-shot Conversion Mode) Operation Timing



63. 12.6.9 Hardware trigger wait mode (select mode, sequential conversion mode)(p.496)

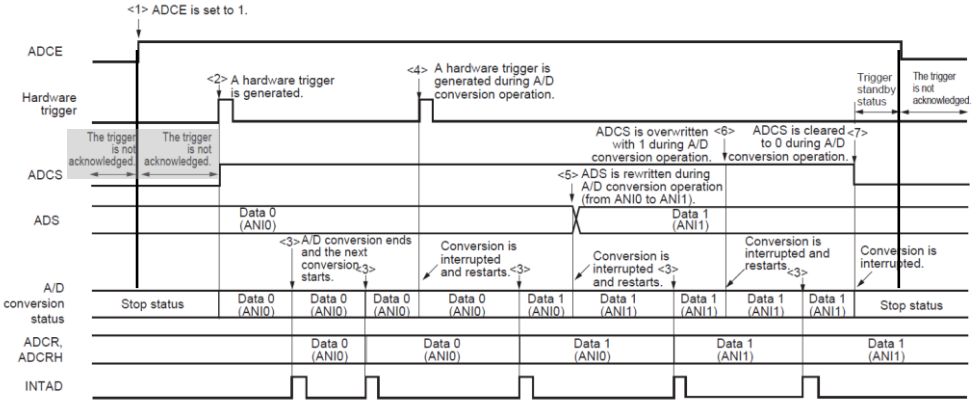
Old)

Figure 12-28. Example of Hardware Trigger Wait Mode
(Select Mode, Sequential Conversion Mode) Operation Timing



New)

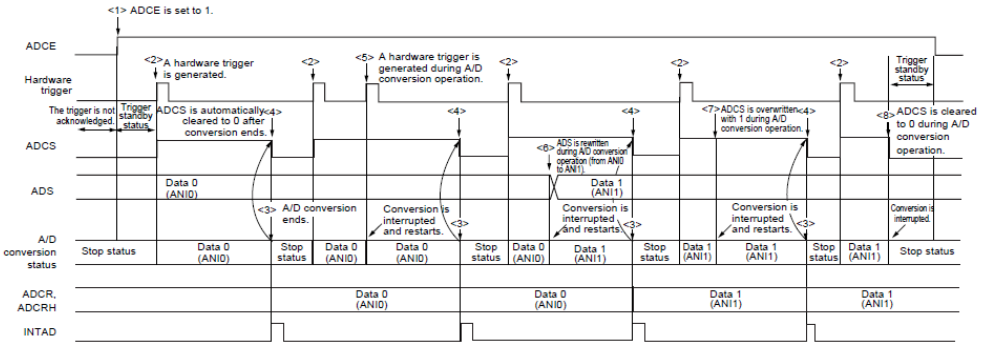
Figure 12-28. Example of Hardware Trigger Wait Mode
(Select Mode, Sequential Conversion Mode) Operation Timing



64. 12.6.10 Hardware trigger wait mode (select mode, one-shot conversion mode)(p.497)

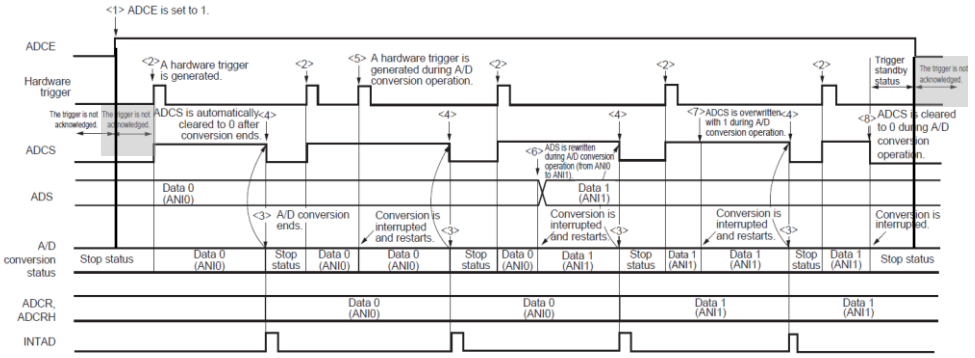
Old)

Figure 12-29. Example of Hardware Trigger Wait Mode
(Select Mode, One-Shot Conversion Mode) Operation Timing



New)

Figure 12-29. Example of Hardware Trigger Wait Mode
(Select Mode, One-Shot Conversion Mode) Operation Timing



65. 15.3.14 Serial standby control register0(SSC0)(p.572)

Old)

The SSC0 register is used to control the startup of reception (the SNOOZE mode) while in the STOP mode when receiving CSI00 or UART0 serial data.

The SSC0 register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSC0 register can be set with an 8-bit memory manipulation instruction with SSC0L.

Reset signal generation clears the SSC0 register to 0000H.

Caution The maximum transfer rate in the SNOOZE mode is as follows.

• When using CSI00: 1 Mbps
• When using UART0: 9600 bps

New)

The SSC0 register is used to control the startup of reception (the SNOOZE mode) while in the STOP mode when receiving CSI00 or UART0 serial data.

The SSC0 register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SSC0 register can be set with an 8-bit memory manipulation instruction with SSC0L.

Reset signal generation clears the SSC0 register to 0000H.

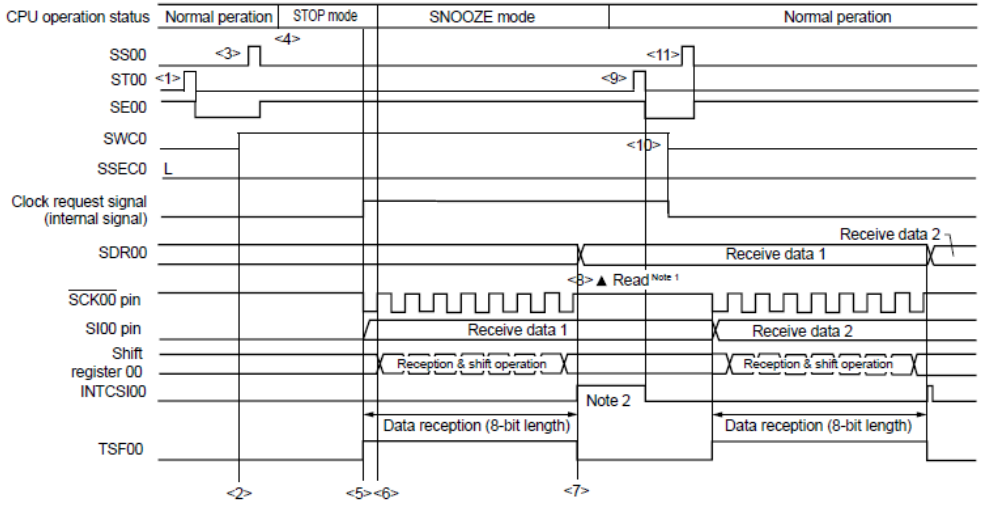
Caution The maximum transfer rate in the SNOOZE mode is as follows.

• When using CSI00: Up to 1 Mbps
• When using UART0: 4800 bps only

66. 15.5.7 SNOOZE mode function (only CSI00)(p.638)

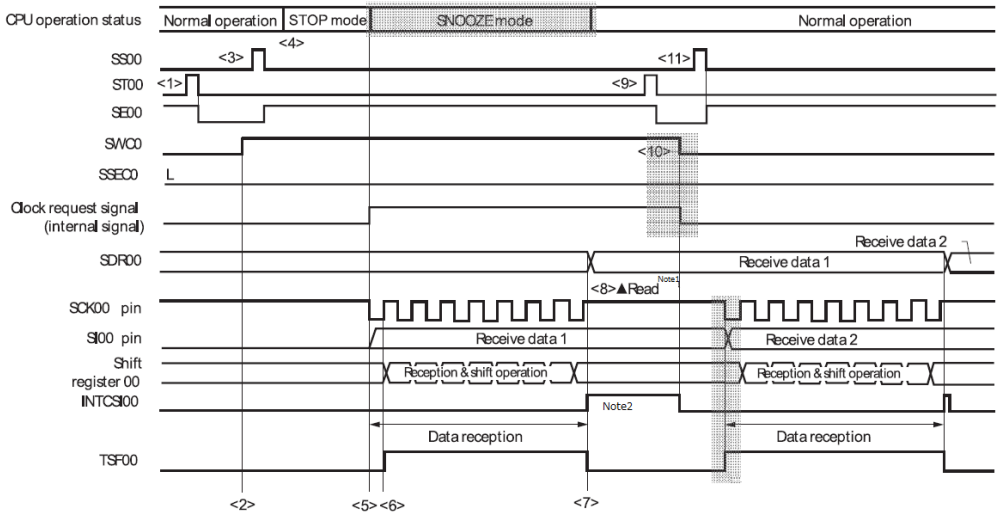
Old)

Figure 15-71. Timing Chart of SNOOZE Mode Operation (Once Startup)
(Type 1: DAPmn = 0, CKPmn = 0)



New)

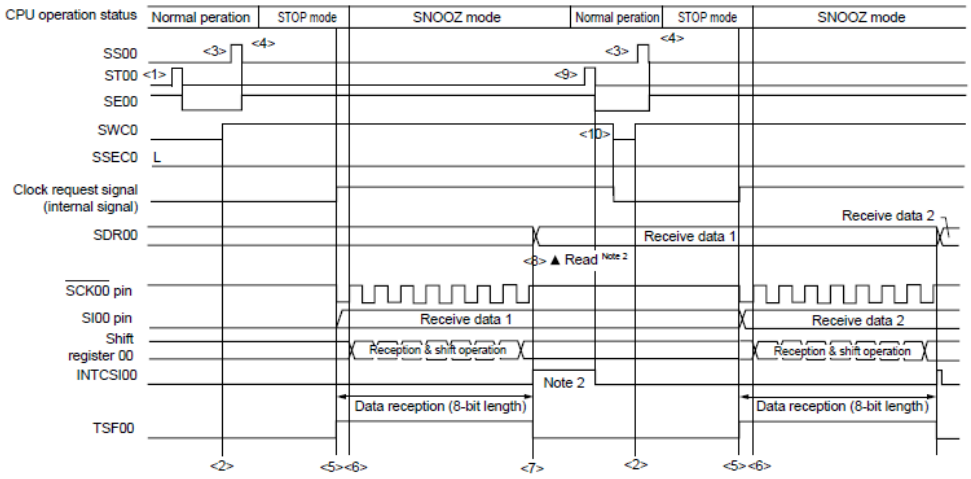
Figure 15-71. Timing Chart of SNOOZE Mode Operation (Once Startup)
(Type 1: DAPmn = 0, CKPmn = 0)



67. 15.5.7 SNOOZE mode function (only CSI00)(p.640)

Old)

Figure 15-73. Timing Chart of SNOOZE Mode Operation (Continuous Startup) (Type 1: DAPmn = 0, CKPmn = 0)



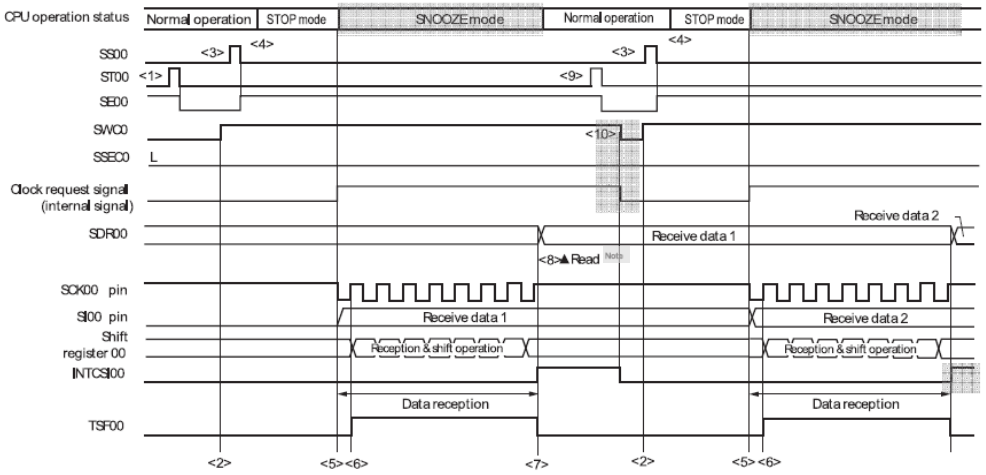
Notes 1. Only read received data while SWCm = 1 and before the next edge of the $\overline{\text{SCKp}}$ pin input is detected.

2. The transfer end interrupt (INTCSIp) is cleared either when SWCm is cleared to 0 or when the next edge of the SCKp pin input is detected.

Caution Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm0 bit to 1 (clear the SEm0 bit, and stop the operation).
And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE release).

New)

Figure 15-73. Timing Chart of SNOOZE Mode Operation (Continuous Startup) (Type 1: DAPmn = 0, CKPmn = 0)



Notes Only read received data while SWCm = 1 and before the next edge of the SCKp pin input is detected.

Caution 1.Before switching to the SNOOZE mode or after reception operation in the SNOOZE mode finishes, set the STm0 bit to 1 (clear the SEm0 bit, and stop the operation).
And after completion the receive operation, also clearing SWCm bit to 0 (SNOOZE release).

2.When SWCm=1,the BFFm1 and OVFm1 flags will not change

68. 15.6.3 SNOOZE mode function(p.664)

Old)

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

Only UART0 can be set to the SNOOZE mode.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

Remark m = 0; n = 0; q = 0

New)

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

Only UART0 can be set to the SNOOZE mode.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

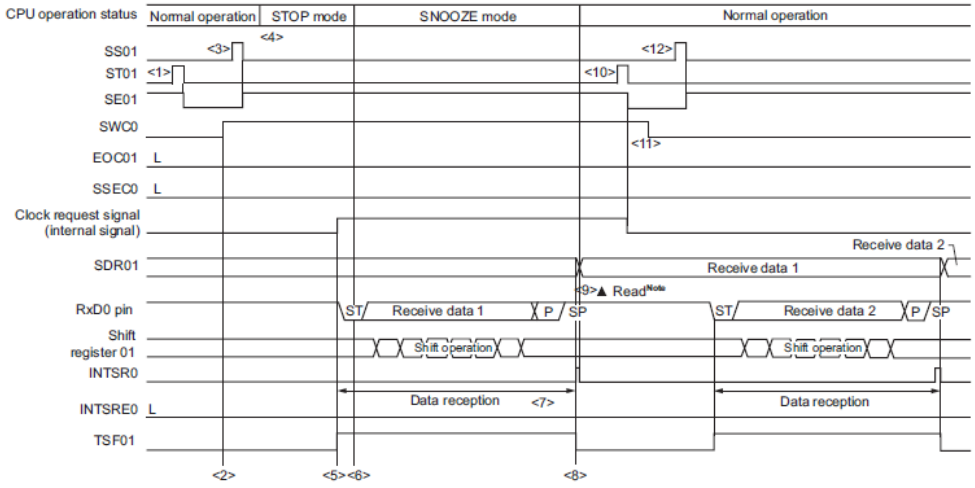
5. The CPU shifts from the STOP mode to the SNOOZE mode on detecting the valid edge of the RxDq signal. Note,however,that transfer through the UART channel may not start and the CPU may remain in the SNOOZE node if an input pulse on the RxDq pin is too short to be detected as a start bit. In such cases, data may note be received correctly, and this may lead to a framing error or parity error in the next UART transfer.

Remark m = 0; n = 0; q = 0

69. 15.6.3 SNOOZE mode function(p.666)(Recorrection of No.8)

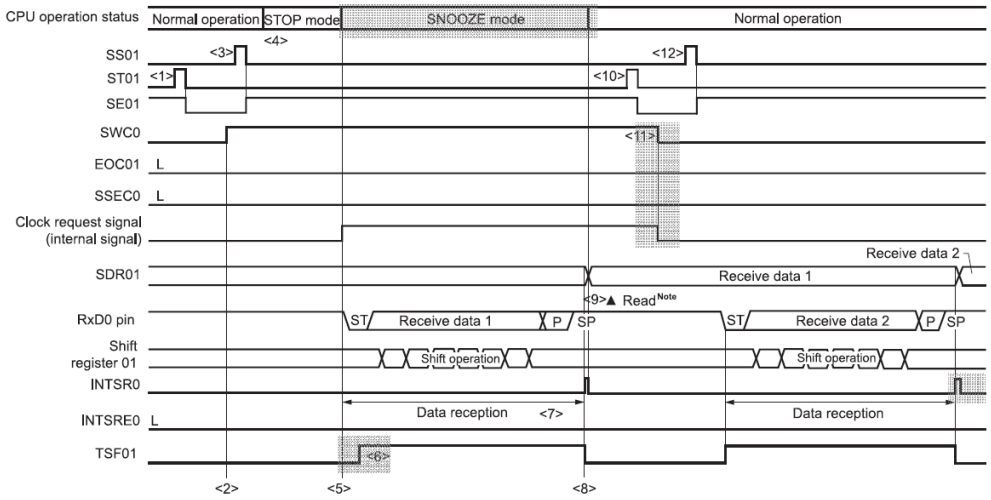
Old)

Figure 15-90. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 0, SSECm = 0/1)



New)

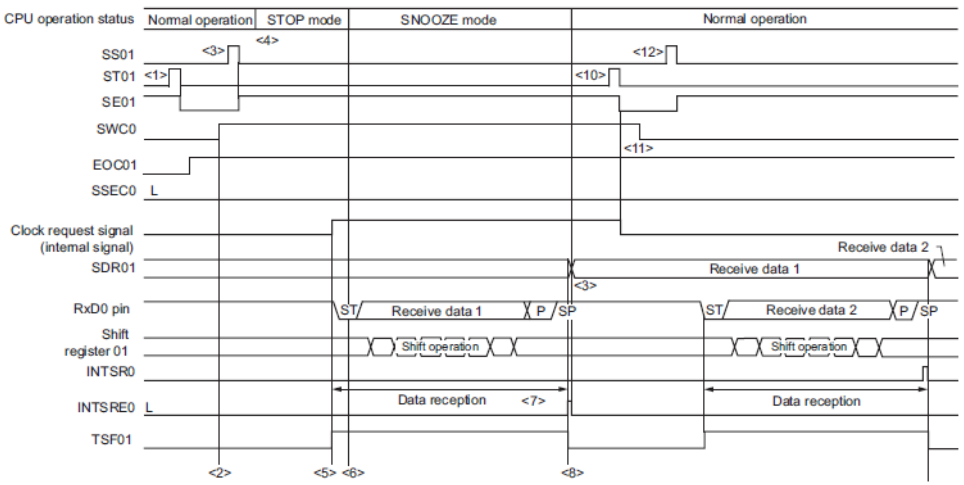
Figure 15-90. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 0, SSECm = 0/1)



70. 15.6.3 SNOOZE mode function(p.667)(Recorrection of No.8)

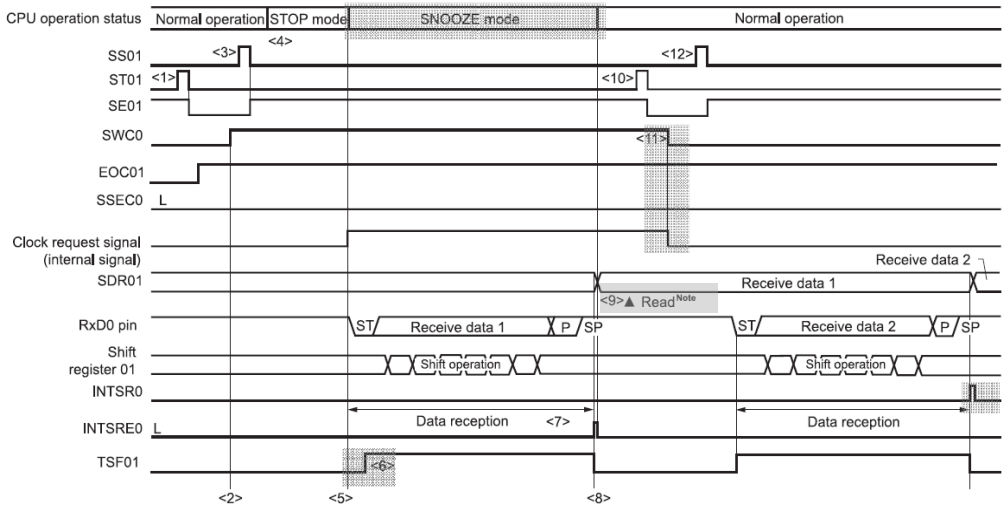
Old)

Figure 15-91. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 1, SSECm = 0)



New)

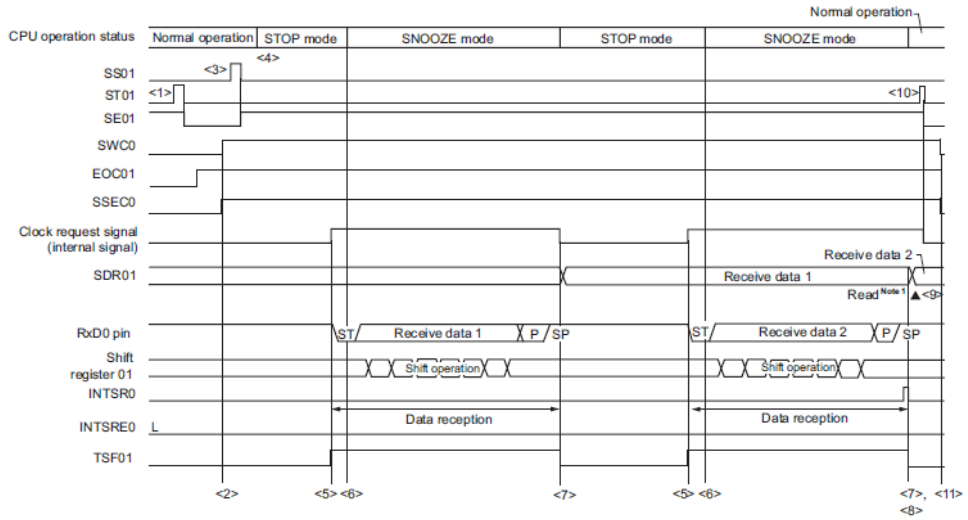
Figure 15-91. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 1, SSECm = 0)



71. 15.6.3 SNOOZE mode function(p.669)(Recorrection of No.8)

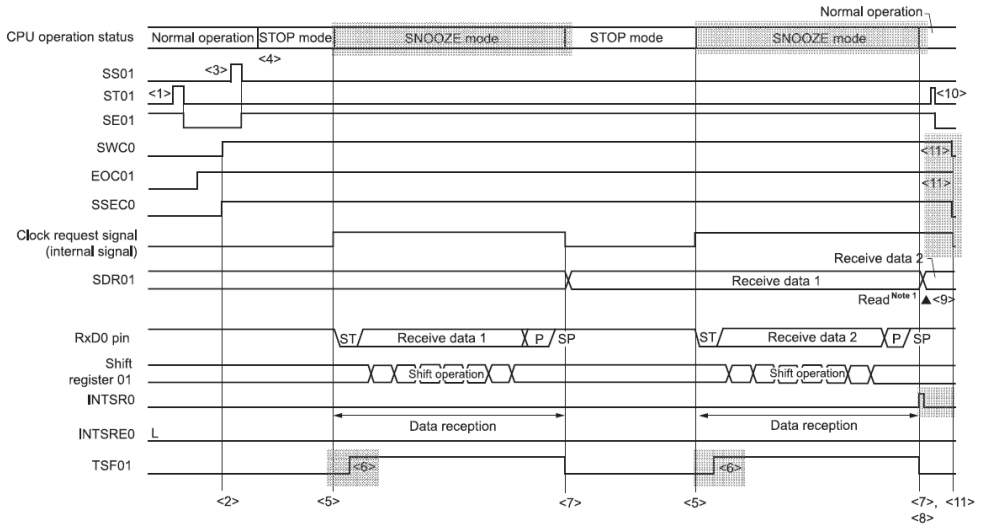
Old)

Figure 15-93. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 1, SSECm = 1)



New)

Figure 15-93. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 1, SSECm = 1)



72. 16.5.3 SNOOZE mode function(p.735)

Old)

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

Only UART0 can be set to the SNOOZE mode.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

Remark m = 0; n = 0; q = 0

New)

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.

Only UART0 can be set to the SNOOZE mode.

(omitted)

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (f_{IH}) is selected for f_{CLK}.

(omitted)

4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn, FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore, when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

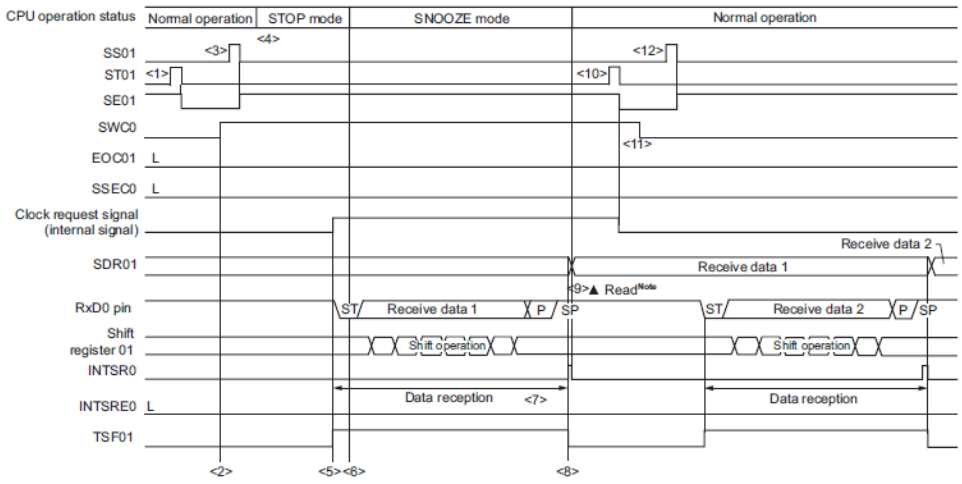
5. The CPU shifts from the STOP mode to the SNOOZE mode on detecting the valid edge of the RxDq signal. Note,however,that transfer through the UART channel may not start and the CPU may remain in the SNOOZE node if an input pulse on the RxDq pin is too short to be detected as a start bit. In such cases, data may note be received correctly, and this may lead to a framing error or parity error in the next UART transfer.

Remark m = 0; n = 0; q = 0

73. 16.5.3 SNOOZE mode function(p.737)

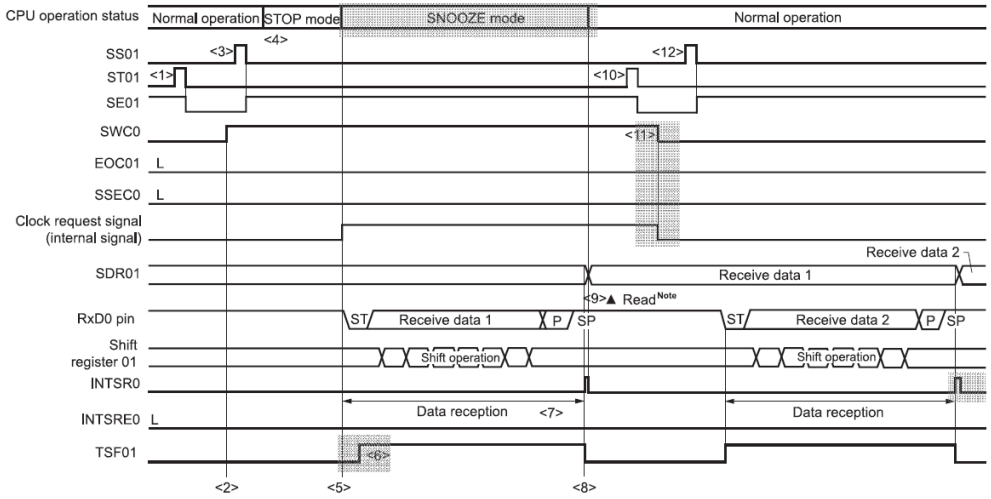
Old)

Figure 16-41. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 0, SSECm = 0/1)



New)

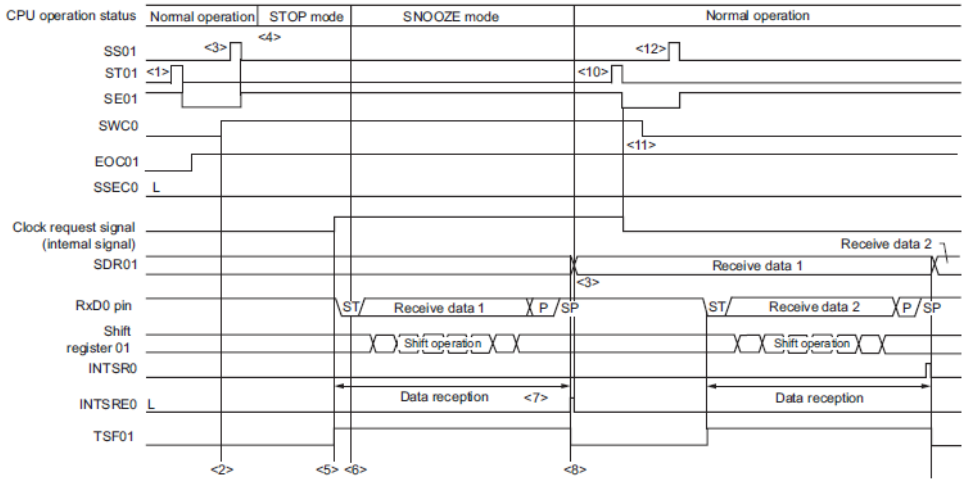
Figure 16-41. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 0, SSECm = 0/1)



74. 16.5.3 SNOOZE mode function(p.738)

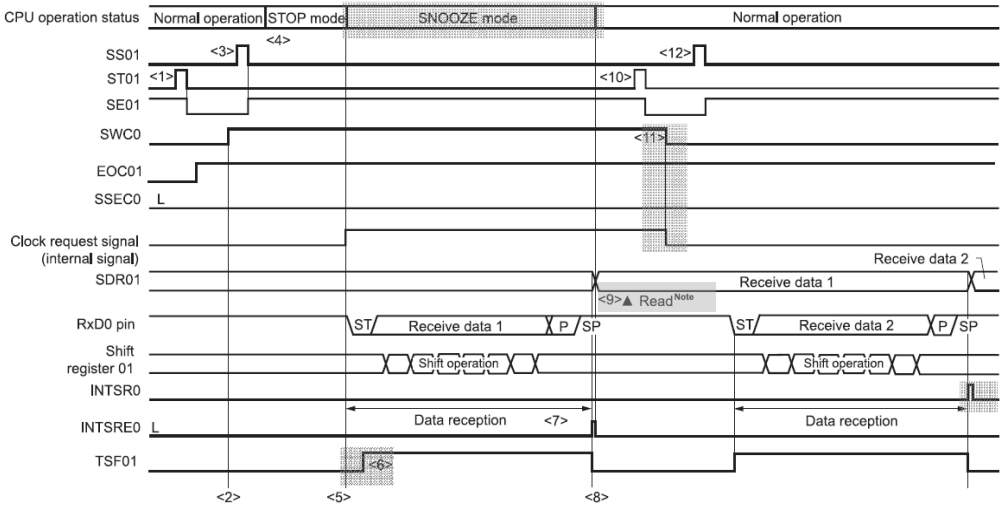
Old)

Figure 16-42. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 1, SSECm = 0)



New)

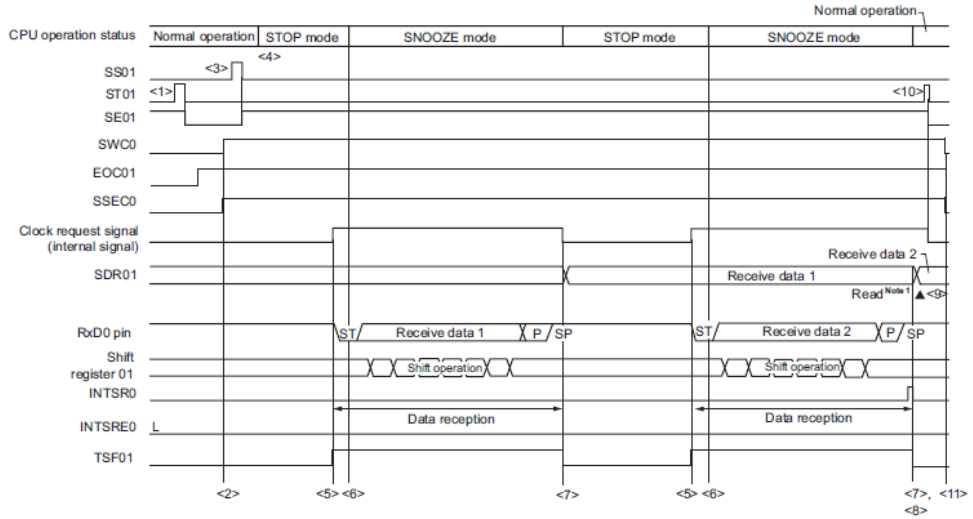
Figure 16-42. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 1, SSECm = 0)



75. 16.5.3 SNOOZE mode function(p.740)

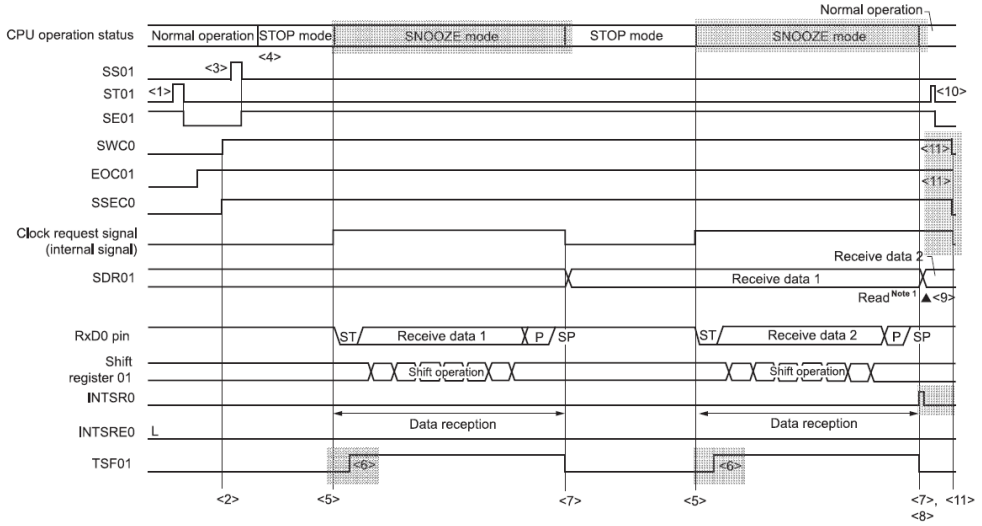
Old)

Figure 16-44. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 1, SSECm = 1)



New)

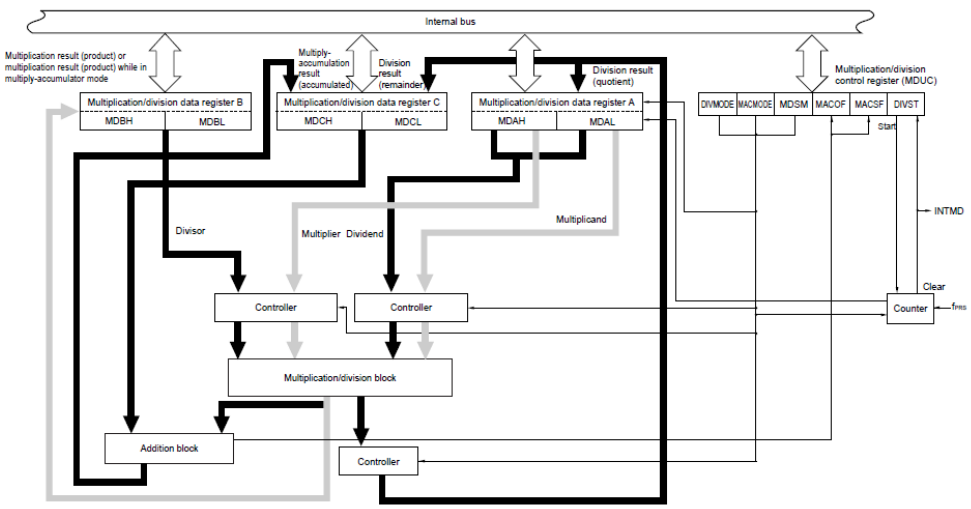
Figure 16-44. Timing Chart of SNOOZE Mode Operation
(EOCm1 = 1, SSECm = 1)



76. 18.2 Configuration of Multiplier and Divider/Multiply-Accumulator (p.860)

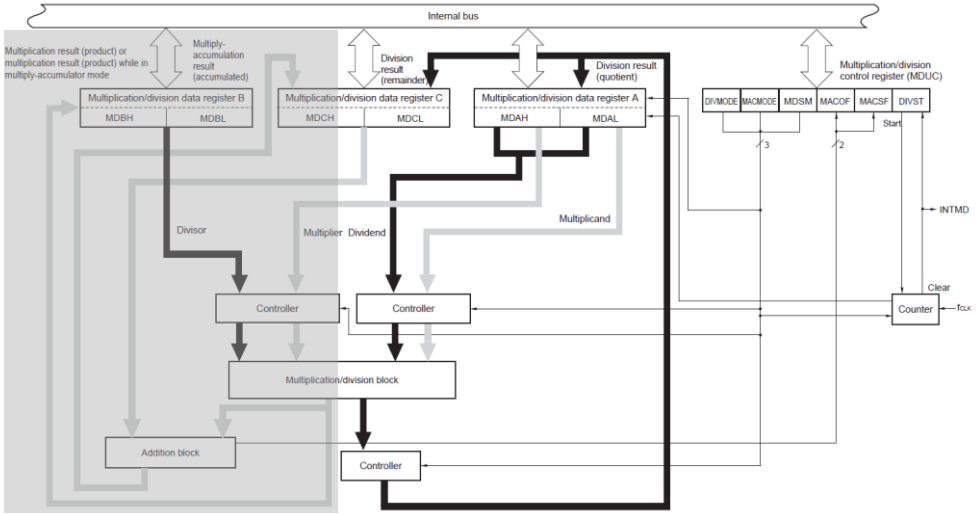
Old)

Figure18-1.Block Diagram of Multiplier and Divider/Multiply-Accumulator



New)

Figure18-1.Block Diagram of Multiplier and Divider/Multiply-Accumulator

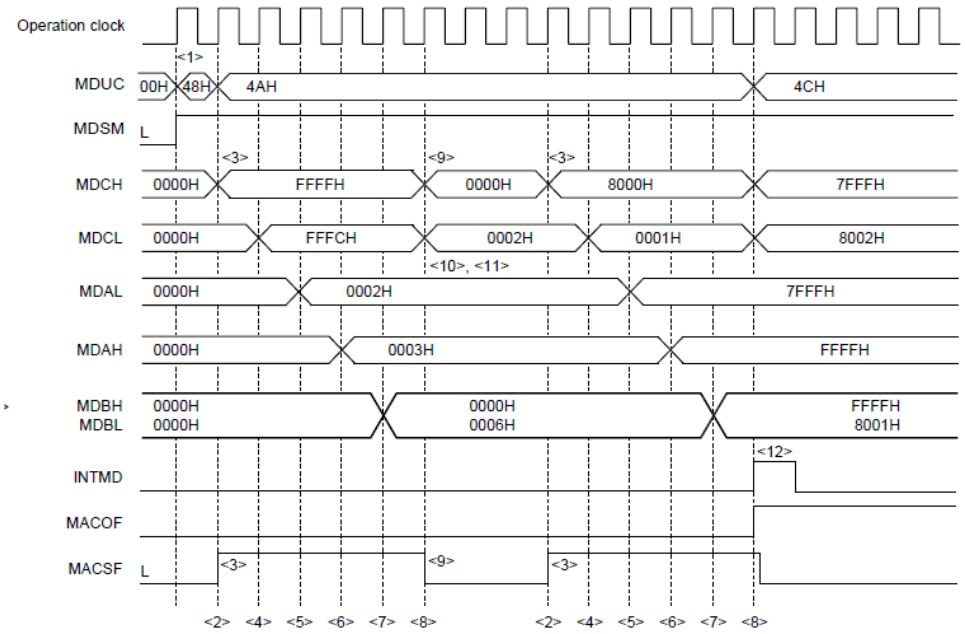


Remark fCLK:CPU/peripheral hardware clock frequency

77. 18.4.4 Multiply-accumulation (signed) operation(p.872)

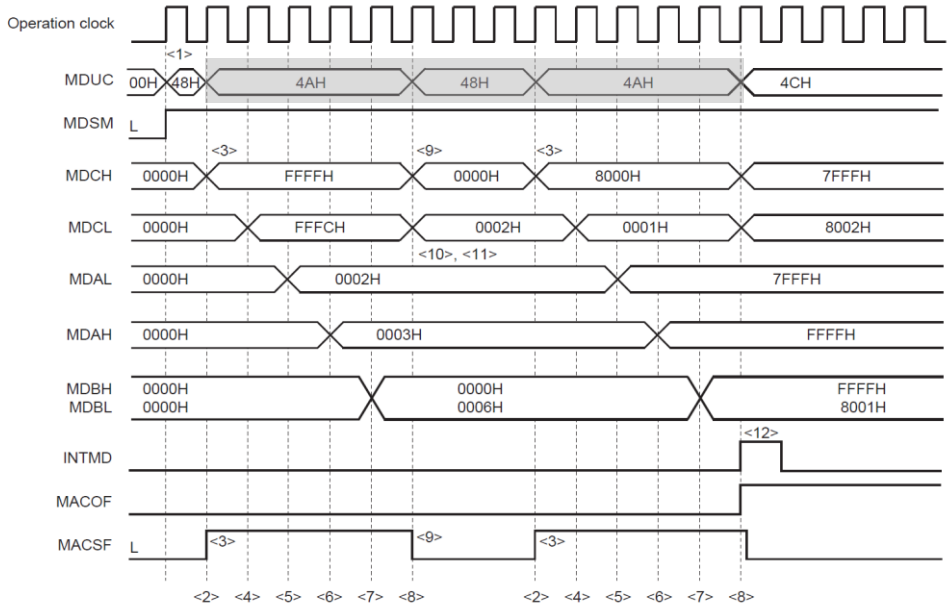
Old)

Figure 18-9. Timing Diagram of Multiply-Accumulation (signed) Operation
(2 × 3 + (–4) = 2 → 32767 × (–1) + (–2147483647) = –2147450882 (Overflow Occurs.))



New)

Figure 18-9. Timing Diagram of Multiply-Accumulation (signed) Operation
(2 × 3 + (–4) = 2 → 32767 × (–1) + (–2147483647) = –2147450882 (Overflow Occurs.))



78. 19.6 Cautions on Using DMA Controller(p.895)

Old)

(4) DMA pending instruction

Even if a DMA request is generated, DMA transfer is held pending immediately after the following instructions.

- CALL !addr16
- CALL $!addr20
- CALL !!addr20
- CALL rp
- CALLT [addr5]
- BRK

- Bit manipulation instructions for registers IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, and PSW each.
- An instruction that accesses a register placed in the 2nd SFR address range from F0500H to F06FFH
- Instruction for accessing the data flash memory

New)

(4) DMA pending instruction

Even if a DMA request is generated, DMA transfer is held pending immediately after the following instructions.

- CALL !addr16
- CALL $!addr20
- CALL !!addr20
- CALL rp
- CALLT [addr5]
- BRK
- MOV PSW, #byte
- MOV PSW, A
- MOV1 PSW. bit, CY
- SET1 PSW. bit
- CLR1 PSW. bit
- POP PSW
- BTCLR PSW. bit, $addr20
- EI
- DI

- Write instructions for registers IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, and PR12H each.
- An instruction that accesses a register placed in the 2nd SFR address range from F0500H to F06FFH
- Instruction for accessing the data flash memory

79. 23.1 Functions of Power-on-reset Circuit(p.957)

Old)

The power-on-reset circuit (POR) has the following functions.

- Generates internal reset signal at power on.
  The reset signal is released when the supply voltage (V_{DD}) exceeds 1.51 V ±0.03 V.

- Compares supply voltage (V_{DD}) and detection voltage (V_{PDR} = 1.50 V ±0.03 V), generates internal reset signal when $V_{DD} < V_{PDR}$.

Caution **If an internal reset signal is generated in the POR circuit, TRAP, WDTRF, RPERF, IAWRF, and LVIRF flags of the reset control flag register (RESF) is cleared.**

Remark This product incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT), voltage-detector (LVD), illegal instruction execution, RAM parity error, or illegal-memory access. The RESF register is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by the watchdog timer (WDT), voltage-detector (LVD), illegal instruction execution, RAM parity error, or illegal-memory access.For details of the RESF register, see **CHAPTER 22 RESET FUNCTION**.

New)

The power-on-reset circuit (POR) has the following functions.

- Generates internal reset signal at power on.
  The reset signal is released when the supply voltage (V_{DD}) exceeds the detection voltage (V_{POR}).
  Note that the reset state must be retained until the operating voltage becomes in the range defined in **32.4** or **33.4 AC Characteristics**. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal.

- Compares supply voltage (V_{DD}) and detection voltage (V_{PDR}), generates internal reset signal when $V_{DD} < V_{PDR}$. Note that, after power is supplied, this LSI should be placed in the STOP mode, or in the reset state by utilizing the voltage detection circuit or externally input reset signal, before the operation voltage falls below the range defined in **32.4** or **33.4 AC Characteristics**. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

Caution **If an internal reset signal is generated in the power-on-reset circuit, the reset control flag register (RESF) is cleared to 00H.**

Remark 1. The RL78 microcontroller incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT), voltage-detector (LVD), illegal instruction execution, RAM parity error, or illegal-memory access. The RESF register is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by the watchdog timer (WDT), voltage-detector (LVD), illegal instruction execution, RAM parity error, or illegal-memory access.For details of the RESF register, see **CHAPTER 22 RESET FUNCTION**.

2. V_{POR}: POR power supply rise detection voltage
V_{PDR}: POR power supply fall detection voltage
For details, see **32.6.5** or **33.6.5 POR circuit characteristics**.

80. 24.1 Functions of Voltage Detector(p.964)

Old)

The voltage detector (LVD) has the following functions.

- The LVD circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVDH}, V_{LVDL}), and generates an internal reset or internal interrupt signal.
- The detection level for the power supply detection voltage (V_{LVDH}, V_{LVDL}) can be selected by using the option byte as one of 6 levels (For details, see **CHAPTER 27 OPTION BYTE**).
- Operable in STOP mode.
- The following three operation modes can be selected by using the option byte.

New)

The operation mode and detection voltages (V_{LVDH}, V_{LVDL}, V_{LVD}) for the voltage detector is set by using the option byte (000C1H). The voltage detector (LVD) has the following functions.

- The LVD circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}), and generates an internal reset or internal interrupt signal.
- The detection level for the power supply detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected by using the option byte as one of 6 levels (for details, see **CHAPTER 27 OPTION BYTE**).
- Operable in STOP mode.
- After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in **32.4** or **33.4 AC Characteristics**. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal before the voltage falls below the operating range.
  The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).