Date: Aug. 6, 2013

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A008A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/I1A Descriptions in the Hardware User's Manual Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/I1A R5F107xxx	Lot No. All lots	Reference Document	RL78/I1A User's Manual: Hardware Rev.1.00 R01UH0169EJ0100 (Jul. 2013)		

This document describes misstatements found in the RL78/I1A User's Manual: Hardware Rev.1.00 (R01UH0169EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
Internal data memory space	Page 42	Specifications extended
Table 3-6. Extended SFR (2nd SFR) List	Pages 58 to 69	Specifications added
High-speed on-chip oscillator frequency select register (HOCODIV)	-	Specifications added
16-bit timer KC output pin control register	-	Specifications added
(16) Peripheral function switch register 0 (PFSEL0)	Page 301	Incorrect descriptions revised
Figure 8-16. Timer KC operation setting example	Page 410	Incorrect descriptions revised
A/D converter mode register 0 (ADM0)	Page 463	Incorrect descriptions revised
(5)Comparator rising edge enable register 0 (CMPEGP0), comparator falling edge enable register 0 (CMPEGN0)	Page 532	Incorrect descriptions revised
Figure 14-15. Operation Setting Flow Chart 1 of Comparator	Page 541	Incorrect descriptions revised
Figure 14-16. Operation Setting Flow Chart 2 of Comparator	Page 542	Incorrect descriptions revised
15. 6. 3 SNOOZE mode function	Page 663	Specifications changed
16.6 DALI Mode	Page 732	Specifications extended
16.6.1 DALI transmission	Page 735	Specifications extended
Figure 16-46. Example of Contents of Registers for DALI Transmission	Pages 736 to 737	Specifications extended
16.6.2 DALI reception	Page 743	Specifications extended
Figure 16-52. Example of Contents of Registers for DALI Reception	Pages 744 to 745	Specifications extended
16.7 SNOOZE Mode Function(OnlyDALI/UART4 Reception)	Pages 750 to 755	Specifications extended
Figure 20-5. Format of Priority Specification Flag Registers	Page 903	Incorrect descriptions revised
21.2.2 STOP mode	Page 931	Incorrect descriptions revised
21.2.3 SNOOZE mode	Page 934	Incorrect descriptions revised
Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector	Pages 952 to 953	Incorrect descriptions revised
25.3.6 Invalid memory access detection function	Page 984	Incorrect descriptions revised
27.3 Format of On-chip Debug Option Byte	Page 998	Specifications extended
28.3.1 Data flash overview	Page 1008	Caution added
28.6 Flash Memory Programming by Self-Programming	Page 1017	Caution added
32.3.2 Supply current characteristics	Pages 1059 to 1062	Incorrect descriptions revised
32.5 Peripheral Functions Characteristics	Pages 1067 to 1080	Specifications changed
32.6.1 A/D converter characteristics	Pages 1082 to 1085	Incorrect descriptions revised
32.6.2 Temperature sensor characteristics	Page 1085	Specifications added
Supply Voltage Rise Time	-	Specifications added
32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	Page 1089	Specifications extended
32.8 Flash Memory Programming Characteristics	Page 1089	Incorrect descriptions revised
32.9 Timing Specs for Switching Flash Memory Programming Modes	Page 1090	Incorrect descriptions revised
Chapter 33 ELECTRICAL SPECIFICATIONS (for T_A = −40 to +125°C product)	-	Specifications added

Document Improvement
The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
		Document No.	English	R01UH0169EJ0100
1	Internal data memory space			Page 42	Page 3
2	Table 3-6. Extended SFR (2nd SFR) List			Pages 58 to 69	Page 4
3	High-speed on-chip oscillator frequency select register (HOCODIV)			-	Page 5
4	16-bit timer KC output pin control register			-	Page 6
5	(16) Peripheral function switch register 0 (PFSEL0)			Page 301	Pages 7 to 8
6	Figure 8-16. Timer KC operation setting example			Page 410	Page 9
7	A/D converter mode register 0 (ADM0)			Page 463	Page 10
8	(5)Comparator rising edge enable register 0 (CMPEGP0), comparator falling edge enable register 0 (CMPEGN0)			Page 532	Page 11
9	Figure 14-15. Operation Setting Flow Chart 1 of Comparator			Page 541	Pages 12 to 13
10	Figure 14-16. Operation Setting Flow Chart 2 of Comparator			Page 542	Pages 14 to 15
11	15. 6. 3 SNOOZE mode function			Page 663	Pages 16 to 17
12	16.6 DALI Mode			Page 732	Page 18
13	16.6.1 DALI transmission			Page 735	Page 19
14	Figure 16-46. Example of Contents of Registers for DALI Transmission			Pages 736 to 737	Page 20
15	16.6.2 DALI reception			Page 743	Page 21
16	Figure 16-52. Example of Contents of Registers for DALI Reception			Pages 744 to 745	Page 21
17	16.7 SNOOZE Mode Function(OnlyDALI/UART4 Reception)			Pages 750 to 755	Pages 22 to 23
18	Figure 20-5. Format of Priority Specification Flag Registers			Page 903	Page 24
19	21.2.2 STOP mode			Page 928	Page 25
20	21.2.3 SNOOZE mode			Page 934	Page 26
21	Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector			Pages 952 to 953	Pages 27 to 31
22	25.3.6 Invalid memory access detection function			Page 984	Pages 32 to 33
23	27.3 Format of On-chip Debug Option Byte			Page 998	Pages 34 to 35
24	28.3.1 Data flash overview			Page 1008	Page 36
25	28.6 Flash Memory Programming by Self-Programming			Page 1017	Page 37
26	32.3.2 Supply current characteristics			Pages 1059 to 1062	Page 38
27	32.5 Peripheral Functions Characteristics			Pages 1067 to 1080	Page 38
28	32.6.1 A/D converter characteristics			Pages 1082 to 1085	Page 39
29	32.6.2 Temperature sensor characteristics			Page 1085	Page 39
30	Supply Voltage Rise Time			-	Page 39
31	32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics			Page 1089	Page 39
32	32.8 Flash Memory Programming Characteristics			Page 1089	Page 40
33	32.9 Timing Specs for Switching Flash Memory Programming Modes			Page 1090	Page 40
34	Chapter 33 ELECTRICAL SPECIFICATIONS (for T_A = −40 to +125°C product)			-	Page 40

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/I1A User's Manual: Hardware Rev.1.00 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A008A/E	Aug. 6, 2013	First edition issued No.1 to 34 in corrections (This notice)

Internal data memory space

Incorrect:

The internal RAM can be used as a data area and a program area where instructions are written and executed. Four general-purpose register banks consisting of eight 8-bit registers per bank are assigned to the 32-byte area of FFEE0H to FFEFFH of the internal RAM area. However, instructions cannot be executed by using the general-purpose registers.
The internal RAM is used as a stack memory.

Cautions 1. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetchinginstructions or as a stack area.
2. While using the self-programming function and data flash function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FEF00H to FF309H also cannot beused with the R5F107AE and R5F107DE.

Correct:

The internal RAM can be used as a data area and a program area where instructions are fetchod (it is prohibited to use the general-purpose register area for fetching instructions). Four general-purpose register banks consisting of eight 8-bit registers per bank are assigned to the 32-byte area of FFEE0H to FFEFFH of the internal RAM area.
The internal RAM is used as stack memory.

Cautions 1. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space for fetching instructions or as a stack area.

2. Do not allocate RAM addresses which are used as a stack area, a data buffer, a branch destination of vector interrupt processing, and a DMA transfer destination/transfer source to the area FFE20H to FFEDFH when performing self-programming and rewriting the data flash memory.

3. Use of the RAM areas of the following products is prohibited when performing self-programming and rewriting the data flash memory, because these areas are used for each library.
R5F107AE, R5F107DE: FEF00H to FF309H

Table 3-6. Extended SFR (2nd SFR) List

TKBCNT0,1,2 and TKCCNT0 registers added in "Extended SFR(2nd SFR).

Old:

—

New:

The following registers are added.

F0620H	16-bit timer counter KB0	TKBCNT0	R	—	—	√	FFFFH
F0621H							
F0660H	16-bit timer counter KB1	TKBCNT1	R	—	—	√	FFFFH
F0661H							
F06A0H	16-bit timer counter KB2	TKBCNT2	R	—	—	√	FFFFH
F06A1H							
F06F0H	16-bit timer counter KC0	TKCCNT0	R	—	—	√	FFFFH

High-speed on-chip oscillator frequency select register (HOCODIV)

High-speed on-chip oscillator frequency select register (HOCODIV) is added.

Old:

—

New:

High-speed on-chip oscillator frequency select register (HOCODIV)

The frequency of the high-speed on-chip oscillator which is set by an option byte (000C2H) can be changed by using high-speed on-chip oscillator frequency select register (HOCODIV). However, the selectable frequency depends on the FRQSEL3 bit of the option byte (000C2H).

The HOCODIV register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to the value set by FRQSEL2 to FRQSEL0 of the option byte (000C2H).

Figure 5-12. Format of High-speed On-chip Oscillator Frequency Select Register (HOCODIV)

Address: F00A8H After reset: the value set by FRQSEL2 to FRQSEL0 of the option byte (000C2H) R/W

Symbol	7	6	5	4	3	2	1	0
HOCODIV	0	0	0	0	0	HOCODIV2	HOCODIV1	HOCODIV0

HOCODIV2	HOCODIV1	HOCODIV0	High-Speed On-Chip Oscillator Clock Frequency	
			FRQSEL3 Bit is 0	FRQSEL3 Bit of is 1
0	0	0	24 MHz	32 MHz
0	0	1	12 MHz	16 MHz
0	1	0	6 MHz	8 MHz
0	1	1	3 MHz	4 MHz
1	0	0	Setting prohibited	2 MHz
1	0	1	Setting prohibited	1 MHz
Other than above			Setting prohibited	

Caution 1. Set the HOCODIV register within the operable voltage range of the flash operation mode set in the option byte (000C2H) before and after the frequency change.

Option Byte (000C2H) Value		Flash Operation Mode	Operating Frequency Range	Operating Voltage Range
CMODE1	CMODE2			
1	0	LS (low-speed main) mode	1 MHz to 8 MHz	2.7V to 5.5V
1	1	HS (high-speed main) mode	1 MHz to 16 MHz	
			1 MHz to 32 MHz	

2. Set the HOCODIV register with the high-speed on-chip oscillator clock (f_{IH}) selected as the CPU/peripheral hardware clock (f_{CLK}).

3. After the frequency is changed with the HOCODIV register, the frequency is switched after the following transition time has elapsed.

- **Operation for up to three clocks at the pre-change frequency**
- **CPU/peripheral hardware clock wait at the post-change frequency for up to three clocks**

16-bit timer KC output pin control register

16-bit timer KC output pin control register is added.

Old:

—

New:

16-bit timer KC output pin contorol register (TOETKC0)

It is the register that controls output enable/disable toward pins for the timer output generated from 16-bit timer KC.

The output control of TKCOn is possible regardless of the setting of the timer output gate function which is coupled with 16-bit timer KB.

TOETKC0 can be read by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 8-9. Format of 16-bit timer KC output pin contorol register (TOETKC0)

Address: F05C8H After reset: 00H R/W

Symbol	7	6	<5>	<4>	<3>	<2>	<1>	<0>
TOETKC0	0	0	TOETKC05	TOETKC04	TOETKC03	TOETKC02	TOETKC01	TOETKC00

TOETKC0m	Pin of timer output TKCO0m output enable/disable
0	Disables pin output of TKCO0m.
1	Enables pin output of TKCO0m.

Remark m = 0 to 5

(16) Peripheral function switch register 0 (PFSEL0)

Bit explanation is incorrect and Remark added

Incorrect:

(16) Peripheral function switch register 0 (PFSEL0)

PFSEL0 selects function setting I/O in peripheral function and 16-bit timers KB0, KB1, and KB2.

:

(omitted)

Address: F05C6H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0

CMP2STEN	CMP0STEN	Comparator interrupt selection
See CHAPTER 14 COMPARATOR.		

PNFEN	Use/Do not use external interrupt INTP20 noise filter
0	Use noise filter
1	Do not use noise filter

ADTRG11	ADTRG10	Timer trigger selection for A/D conversion
0	0	Timer KB0 trigger source
0	1	Timer KB1 trigger source
1	0	Timer KB2 trigger source
1	1	Setting prohibited

TMRSTEN1	Use selection for external interrupt INTP21
0	Can be used to clear STOP mode (cannot be used for timer restart function)
1	Can be used for timer restart function (cannot be used to clear STOP mode)

TMRSTEN0	Use selection for external interrupt INTP20
0	Can be used to clear STOP mode (cannot be used for timer restart function)
1	Can be used for timer restart function (cannot be used to clear STOP mode)

Correct:

(16) Peripheral function switch register 0 (PFSEL0)

PFSEL0 selects function setting I/O in peripheral function and 16-bit timers KB0, KB1, and KB2.

:

(omitted)

Address: F05C6H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0

CMP2STEN	CMP0STEN	Comparator interrupt selection
See CHAPTER 14 COMPARATOR.		

PNFEN	Use/Do not use external interrupt INTP20 noise filter
0	Use noise filter
1	Do not use noise filter

ADTRG11	ADTRG10	Timer trigger selection for A/D conversion
0	0	Timer KB0 trigger source
0	1	Timer KB1 trigger source
1	0	Timer KB2 trigger source
1	1	Setting prohibited

TMRSTEN1	Function selection for external interrupt INTP21
0	External interrupt function (external interrupt generation enabled, timer restart disabled)
1	Timer restart function (external interrupt generation disabled, standby release disabled)

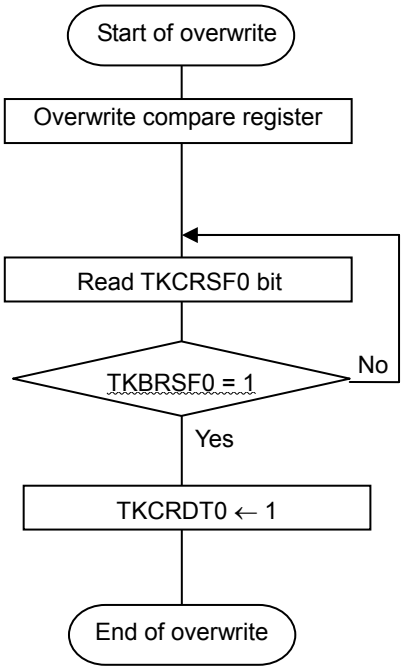
TMRSTEN0	Function selection for external interrupt INTP20
0	External interrupt function (external interrupt generation enabled, timer restart disabled)
1	Timer restart function (external interrupt generation disabled, standby release disabled)

Remark See Block Diagram of Comparator.

Figure 8-16. Timer KC operation setting example

Correction of errors in the flowchart

Incorrect:



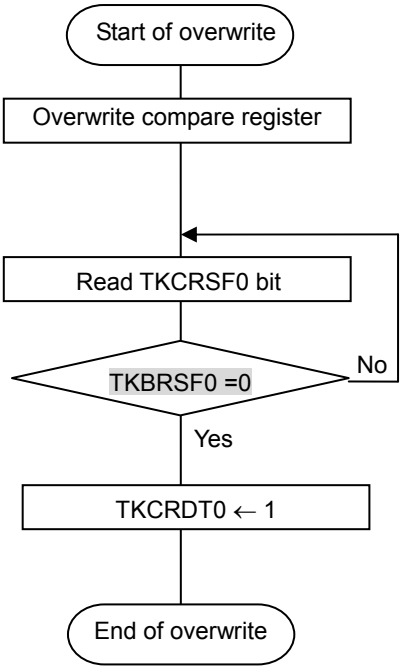
TKBCNTn, TKBCRn0-TKBCRn3, TKBTGCRn (n = 0, 1, 2)
Overwrite TKBDNRn0, TKBDNRn1, TKBCRLDn0, and TKBCRLDn1 register.

Read TKCRSF0 of TKCFLG0 register.
Accept batch overwrite request when TKCRSF0 =1.

Compare register batch overwrite request

After accepting overwrite request, TKCRSF0 bit remains "0" until setting is actually changed.

Correct:



TKBCNTn, TKBCRn0-TKBCRn3, TKBTGCRn (n = 0, 1, 2)
Overwrite TKBDNRn0, TKBDNRn1, TKBCRLDn0, and TKBCRLDn1 register.

Read TKCRSF0 of TKCFLG0 register.
Accept batch overwrite request when TKCRSF0 = 0.

Compare register batch overwrite request

After accepting overwrite request, TKCRSF0 bit remains "1" until setting is actually changed.

A/D converter mode register 0 (ADM0)

Incorrect:

A/D converter mode register 0 (ADM0)

:

(omitted)

:

Caution 1. Change the ADMD, FR2 to FR0, LV1, LV0, and ADCE bits while conversion is stopped or on standby (ADCS = 0).

2. Do not change the ADCE and ADCS bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to set these bits in the order described in 12.7 A/D Converter Setup Flowchart.

Correct:

A/D converter mode register 0 (ADM0)

:

(omitted)

:

Cautions 1. Change the ADMD, FR2 to FR0, LV1, and LV0 bits while conversion is stopped (ADCS = 0, ADCE = 0).

2. Do not set the ADCS bit to 1 and the ADCE bit to 0 at the same time.

3. Do not change the ADCS and ADCE bits from 0 to 1 at the same time by using an 8-bit manipulation instruction. Be sure to set these bits in the order described in 12.7 A/D Converter Setup Flowchart.

(5)Comparator rising edge enable register 0 (CMPEGP0), comparator falling edge enable register 0 (CMPEGN0)

Incorrect:

Figure 14-6. Format of Comparator Rising Edge Enable Register 0 (CMPEGP0) and Comparator Falling Edge Enable Register 0 (CMPEGN0)

CEGP7	CEGN7	INTP21 pin valid edge selection
0	0	Edge detection disabled (disables output of timer forced output stop signal (output signal = fixed to low level))
0	1	Falling edge (enables output of timer forced output stop signal)
1	0	Rising edge (enables output of timer forced output stop signal)
1	1	Both rising and falling edges (enables output of timer forced output stop signal)

CEGP6	CEGN6	INTP20 pin valid edge selection
0	0	Edge detection disabled (disables output of timer forced output stop signal (output signal = fixed to low level))
0	1	Falling edge (enables output of timer forced output stop signal)
1	0	Rising edge (enables output of timer forced output stop signal)
1	1	Both rising and falling edges (enables output of timer forced output stop signal)

Correct:

Figure 14-6.Format of Comparator Rising Edge Enable Register 0 (CMPEGP0) and Comparator Falling Edge Enable Register 0 (CMPEGN0)

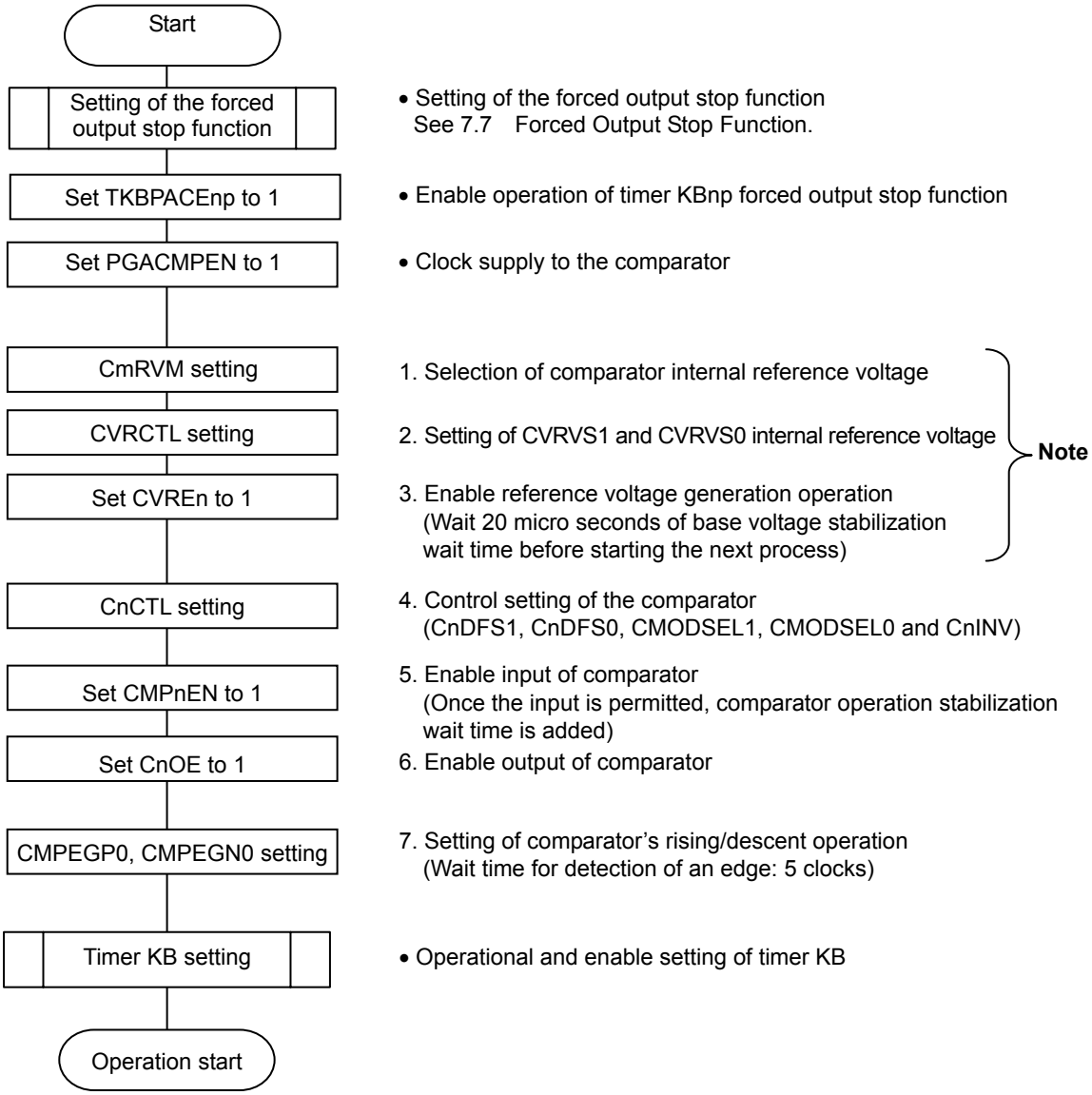
CEGP7	CEGN7	INTP21 pin valid edge selection
0	0	Edge detection disabled (disables output of timer restart signal (output signal = fixed to low level))
0	1	Falling edge (enables output of timer restart signal)
1	0	Rising edge (enables output of timer restart signal)
1	1	Both rising and falling edges (enables output of timer restart signal)

CEGP6	CEGN6	INTP20 pin valid edge selection
0	0	Edge detection disabled (disables output of timer restart signal (output signal = fixed to low level))
0	1	Falling edge (enables output of timer restart signal)
1	0	Rising edge (enables output of timer restart signal)
1	1	Both rising and falling edges (enables output of timer restart signal)

Figure 14-15. Operation Setting Flow Chart 1 of Comparator

Incorrect:

Figure 14-15. Operation Setting Flow Chart 1 of Comparator (CMP)
(Using INTCMPn, CMPnHZO output)

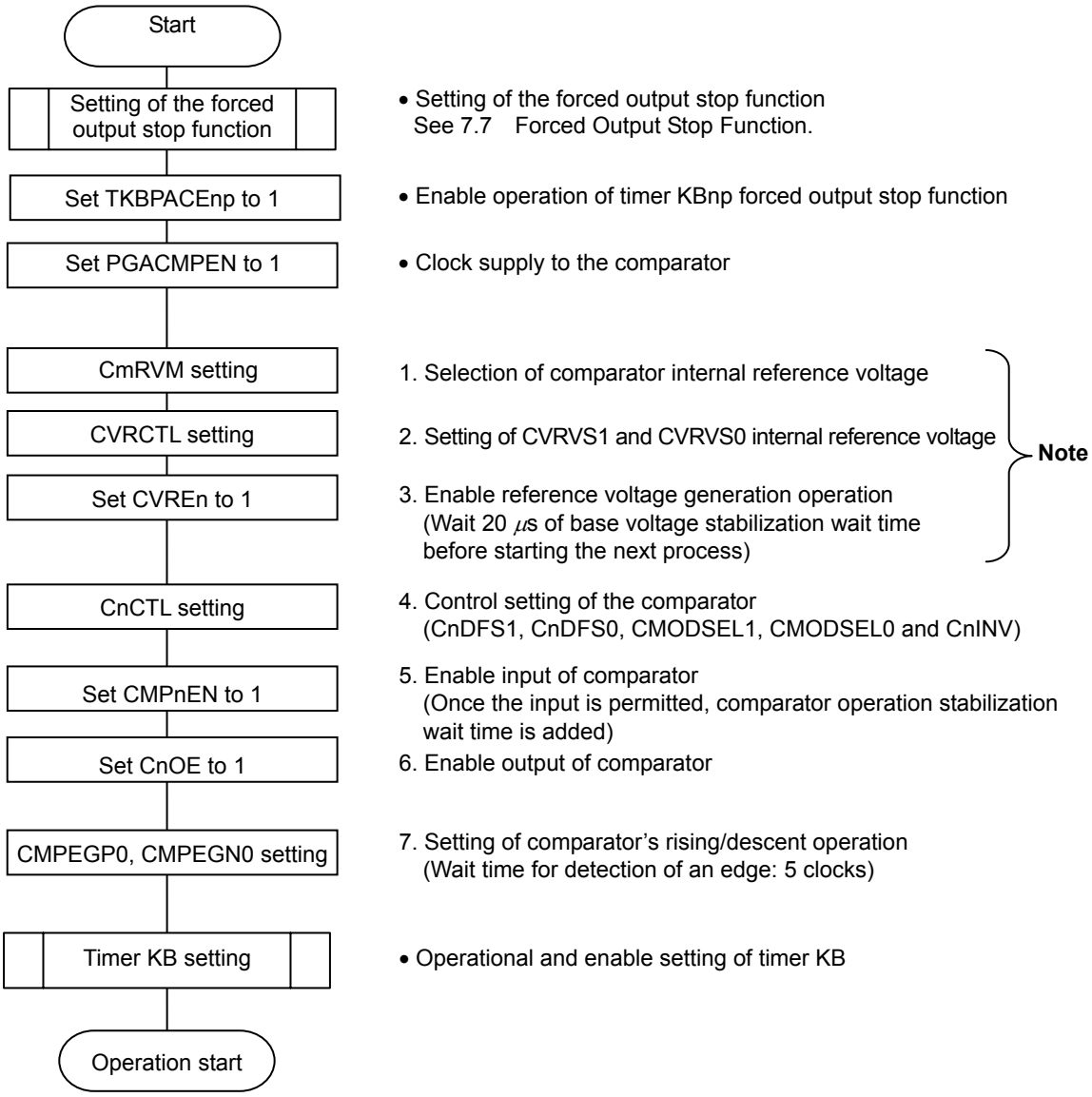


Note It is not required, when the external pin CMPCOM is used for base voltage.

Caution Above 1. to 7. should be set under INTCMP process prohibition state.

Correct:

Figure 14-15. Operation Setting Flow Chart 1 of Comparator (CMP)
(Using Timer Forced Output Stop Request Signal by INTCMPn, CMPn)



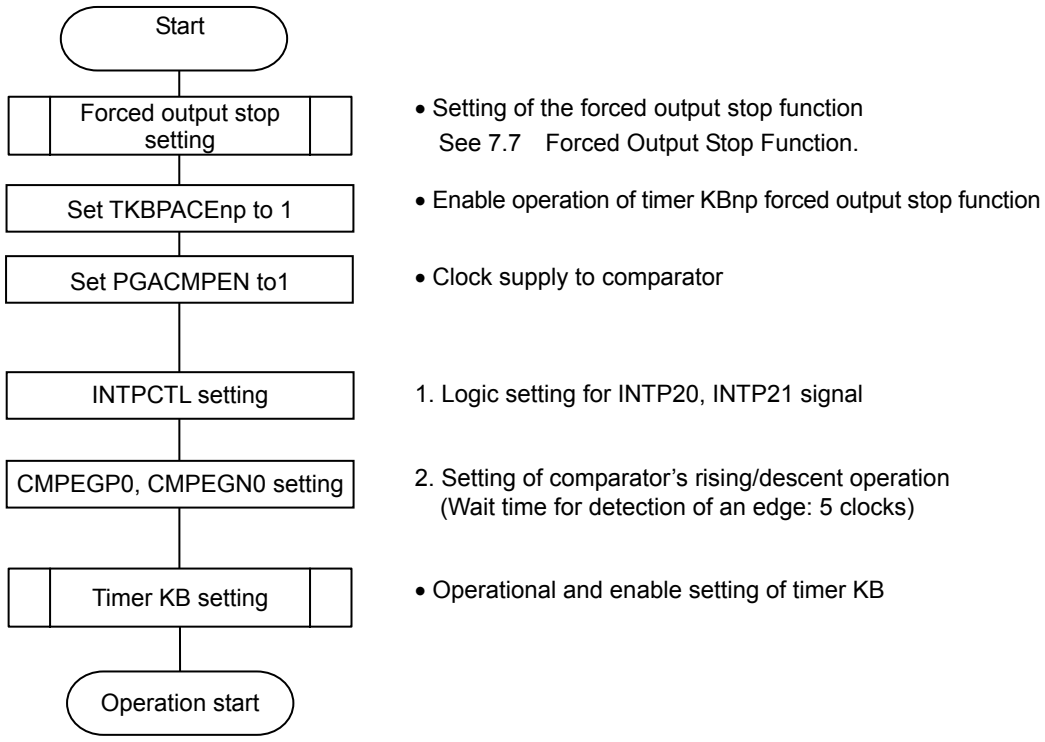
Note It is not required, when the external pin CMPCOM is used for base voltage.

Caution Above 1. to 7. should be set under INTCMP process prohibition state.

Figure 14-16. Operation Setting Flow Chart 2 of Comparator

Incorrect:

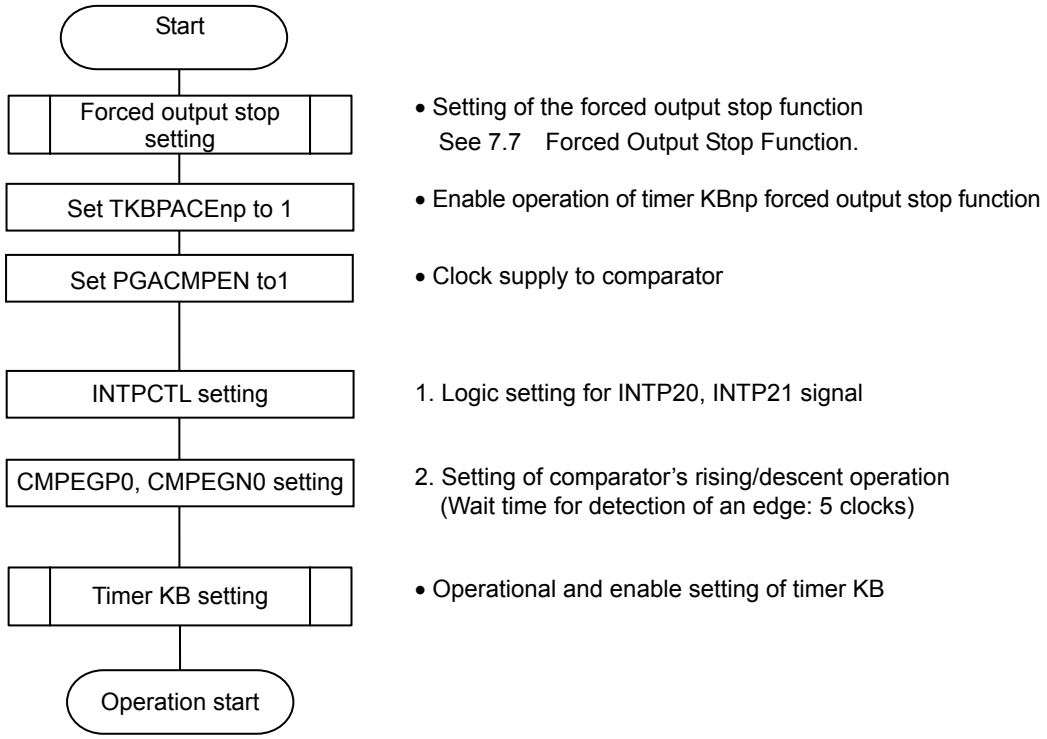
Figure 14-16. Operation Setting Flow Chart 2 of Comparator (CMP)
(Using INTPm, INTPmHZO output (Using Edge circuit only))



Caution Above 1. to 2. should be set under INTCMP process prohibition state.

Correct:

Figure 14-16. Operation Setting Flow Chart 2 of Comparator (CMP)
(Using Timer Forced Output Stop Request Signal by INTPm, INTPm(Using Edge Circuit only))



Caution Above 1. to 2. should be set under INTCMP process prohibition state.

15. 6. 3 SNOOZE mode function

Incorrect:

SNOOZE mode makes UART operate reception by RxD0 pin input detection while the STOP mode. Normally UART stops communication in the STOP mode. But, using the SNOOZE mode makes reception UART operate unless the CPU operation by detecting RxD0 pin input. Only UART0 can be set to the SNOOZE mode.
When using the SNOOZE mode function, set the SWC0 bit of serial standby control register 0 (SSC0) to 1 just before switching to the STOP mode.

Cautions 1. The SNOOZE mode can only be specified when the high-speed on-chip oscillator clock is selected for fCLK.

2. The maximum transfer rate when using UART0 in the SNOOZE mode is 9600 bps.

Correct:

The SNOOZE mode makes the UART perform reception operations upon RxDq pin input detection while in the STOP mode. Normally the UART stops communication in the STOP mode. However, using the SNOOZE mode enables the UART to perform reception operations without CPU operation.
UART0 channel can be set to the SNOOZE mode.

When using UARTq in the SNOOZE mode, make the following settings before entering the STOP mode. (See Figure 12-92 Flowchart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1 or EOCm1 = 1, SSECm = 0) and Figure 12-94 Flowchart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1).)

- In the SNOOZE mode, the baud rate setting for UART reception needs to be changed to a value different from that in normal operation. Set the SPSm register and bits 15 to 9 of the SDRmn register with reference to Table 12-3.
- Set the EOCmn and SSECmn bits. This is for enabling or stopping generation of an error interrupt (INTSRE0) when a communication error occurs.
- When using the SNOOZE mode function, set the SWCm bit of serial standby control register m (SSCm) to 1 just before switching to the STOP mode. After the initial setting has completed, set the SSm1 bit of serial channel start register m (SSm) to 1.
  Upon detecting the edge of RxDq (start bit input) after a transition was made to the STOP mode, UART reception is started.

Cautions 1. The SNOOZE mode can only be used when the high-speed on-chip oscillator clock (fIH) is selected for fCLK.
2. The transfer rate in the SNOOZE mode is only 4800 bps.
3. When SWCm = 1, UARTq can be used only when the reception operation is started in the STOPmode. When used simultaneously with another SNOOZE mode function or interrupt, if the reception operation is started in a state other than the STOP mode, such as those given below,data may not be received correctly and a framing error or parity error may be generated.
   - When after the SWCm bit has been set to 1, the reception operation is started before the STOP mode is entered
   - When the reception operation is started while another function is in the SNOOZE mode
   - When after returning from the STOP mode to normal operation due to an interrupt or other cause, the reception operation is started before the SWCm bit is returned to 0
4. If a parity error, framing error, or overrun error occurs while the SSECm bit is set to 1, the PEFmn,FEFmn, or OVFmn flag is not set and an error interrupt (INTSREq) is not generated. Therefore,when the setting of SSECm = 1 is made, clear the PEFmn, FEFmn, or OVFmn flag before setting the SWC0 bit to 1 and read the value in bits 7 to 0 (RxDq register) of the SDRm1 register.

Table 15-3. Baud Rate Setting for UART Reception in SNOOZE Mode

High-speed on-chip oscillator (f_{IH})	UART reception baud rate in SNOOZE mode			
	Baud rate: 4800 bps			
	Operating clock (f_{MCK})	SDRmn [15:9]	Maximum acceptable value	Minimum acceptable value
32 MHz ± 1.0% (note)	$f_{CLK}/2^5$	105	2.27%	−1.53%
24 MHz ± 1.0% (note)	$f_{CLK}/2^5$	79	1.60%	−2.18%
16 MHz ± 1.0% (note)	$f_{CLK}/2^4$	105	2.27%	−1.53%
12 MHz ± 1.0% (note)	$f_{CLK}/2^4$	79	1.60%	−2.19%
8 MHz ± 1.0% (note)	$f_{CLK}/2^3$	105	2.27%	−1.53%
6 MHz ± 1.0% (note)	$f_{CLK}/2^3$	79	1.60%	−2.19%
4 MHz ± 1.0% (note)	$f_{CLK}/2^2$	105	2.27%	−1.53%
3 MHz ± 1.0% (note)	$f_{CLK}/2^2$	79	1.60%	−2.19%
2 MHz ± 1.0% (note)	$f_{CLK}/2^1$	105	2.27%	−1.54%
1 MHz ± 1.0% (note)	$f_{CLK}/2^0$	105	2.27%	−1.57%

Note: When the high-speed on-chip oscillator clock accuracy is at ± 1.5% or 2.0%, the acceptable range is limited as follows:
• f_{IH} ± 1.5%: Subtract 0.5% from the maximum acceptable value of f_{IH} ± 1.0%, and add 0.5% to the minimum acceptable value of f_{IH} ± 1.0%.
• f_{IH} ± 2.0%: Subtract 1.0% from the maximum acceptable value of f_{IH} ± 1.0%, and add 1.0% to the minimum acceptable value of f_{IH} ± 1.0%.

Remarks: Maximum and minimum acceptable values in the above table are the baud rate acceptable values in UART reception. Make sure to set the baud rate for transmission within this range.

16.6 DALI Mode

Master mode of DALI communication is added.

Old:

This mode is used to perform slave transmission/reception of DALI (Digital Addressable Lighting Interface).
DALI performs communication using the following protocol.

New:

This mode is used to perform data transmission/reception as master and slave of DALI (Digital Addressable Lighting Interface).
DALI performs communication using the following protocol.

16.6.1 DALI transmission

DALI transmission functions are extended.

Old)

P.735 Figure

DALI transmission	
Transfer data length	8, 16, or 24 bits
Data phase	Forward output(default: high level)

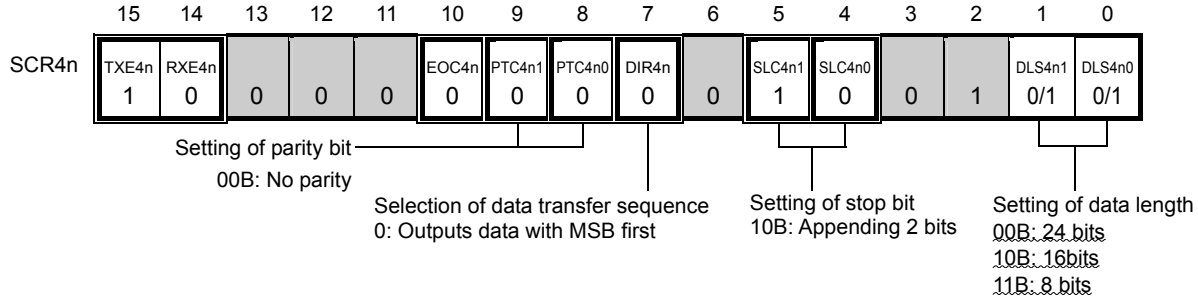
New)

DALI transmission	
Transfer data length	8, 16, 17, or 24 bits
Data phase	Non-reverse output (default: high level), reverse output (default: low level)

Figure 16-46. Example of Contents of Registers for DALI Transmission

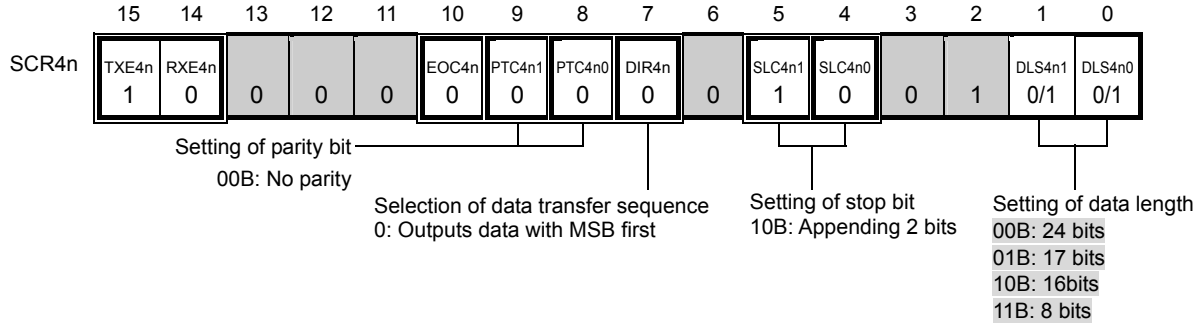
Old)

(c) Serial communication operation setting register 4n (SCR4n)



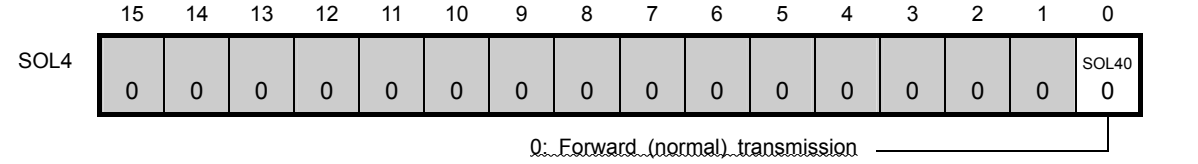
New)

(c) Serial communication operation setting register 4n (SCR4n)



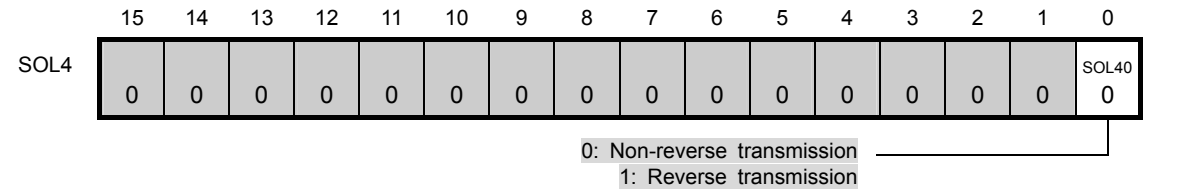
Old)

(f) Serial output level register 4 (SOL4) … Sets only the bits of the target channel.



New)

(f) Serial output level register 4 (SOL4) … Sets only the bits of the target channel.



16.6.2 DALI reception

DALI reception functions are extended.

Old)

DALI Reception	
Transfer data length	16, 17, or 24 bits
Data phase	Forward output (default: high level)

New)

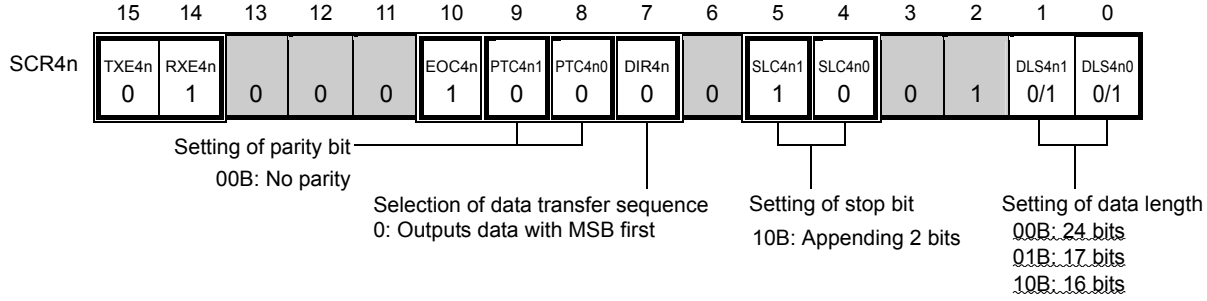
DALI Reception	
Transfer data length	8, 16, 17, or 24 bits
Data phase	Non-reverse output (default: high level), reverse output (default: low level)

Figure 16-52. Example of Contents of Registers for DALI Reception

Old)

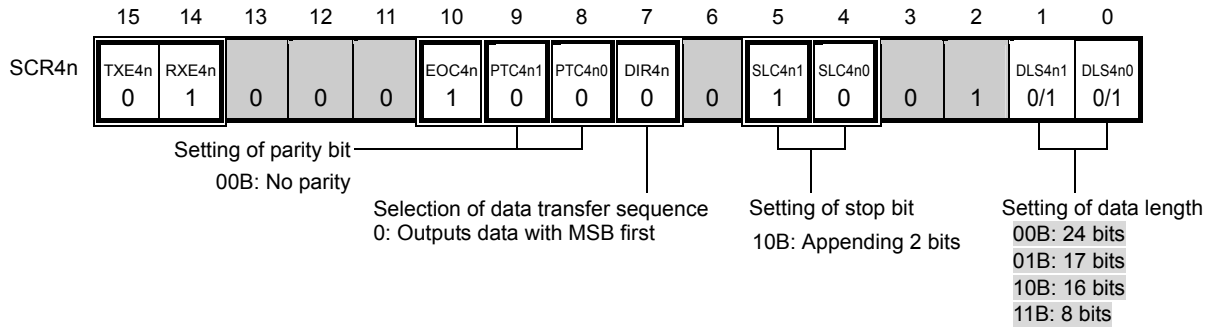
P.744 Register setting

(d) Serial communication operation setting register 4n (SCR4n)



New)

(d) Serial communication operation setting register 4n (SCR4n)



16.7 SNOOZE Mode Function (Only DALI/UART4 Reception)

Use of SNOOZE mode

During the SNOOZE mode function of DALI mode, the manchester framing error may occur depending on the baud rate and the start bit waveform even if the data is correct. In this case, the data is received but it is impossible to distinguish the error. To avoid this problem, please use "STOP & HALT Mode Function (Only DALI/UART4 Reception)" described

Old)

16.7 SNOOZE Mode Function (Only DALI/UART4 Reception)

DALI reception and UART reception (channel 1) support the SNOOZE mode. When DALIRxD4 pin input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible.
When using the SNOOZE mode function, set the SWC bit of serial standby control register 4 (SSC4) to 1 before switching to the STOP mode.

:
(omitted)
:

Remark <1> to <11> in the figure correspond to <1> to <11> in Figure 16-60. Flowchart of SNOOZE Mode Operation (Normal Operation/Abnormal Operation <1>)**)**.

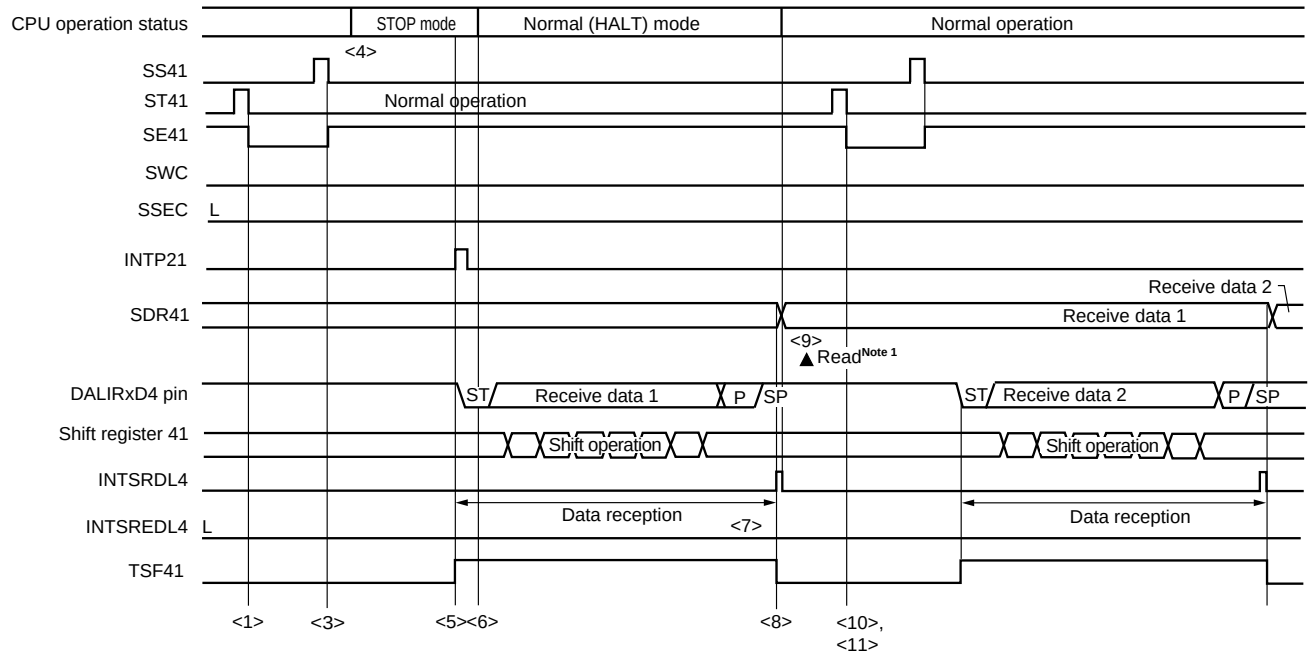
New)

16.7 STOP & HALT Mode Function (Only DALI/UART4 Reception)

(1) Returning from STOP & HALT modes (when DALI is received)

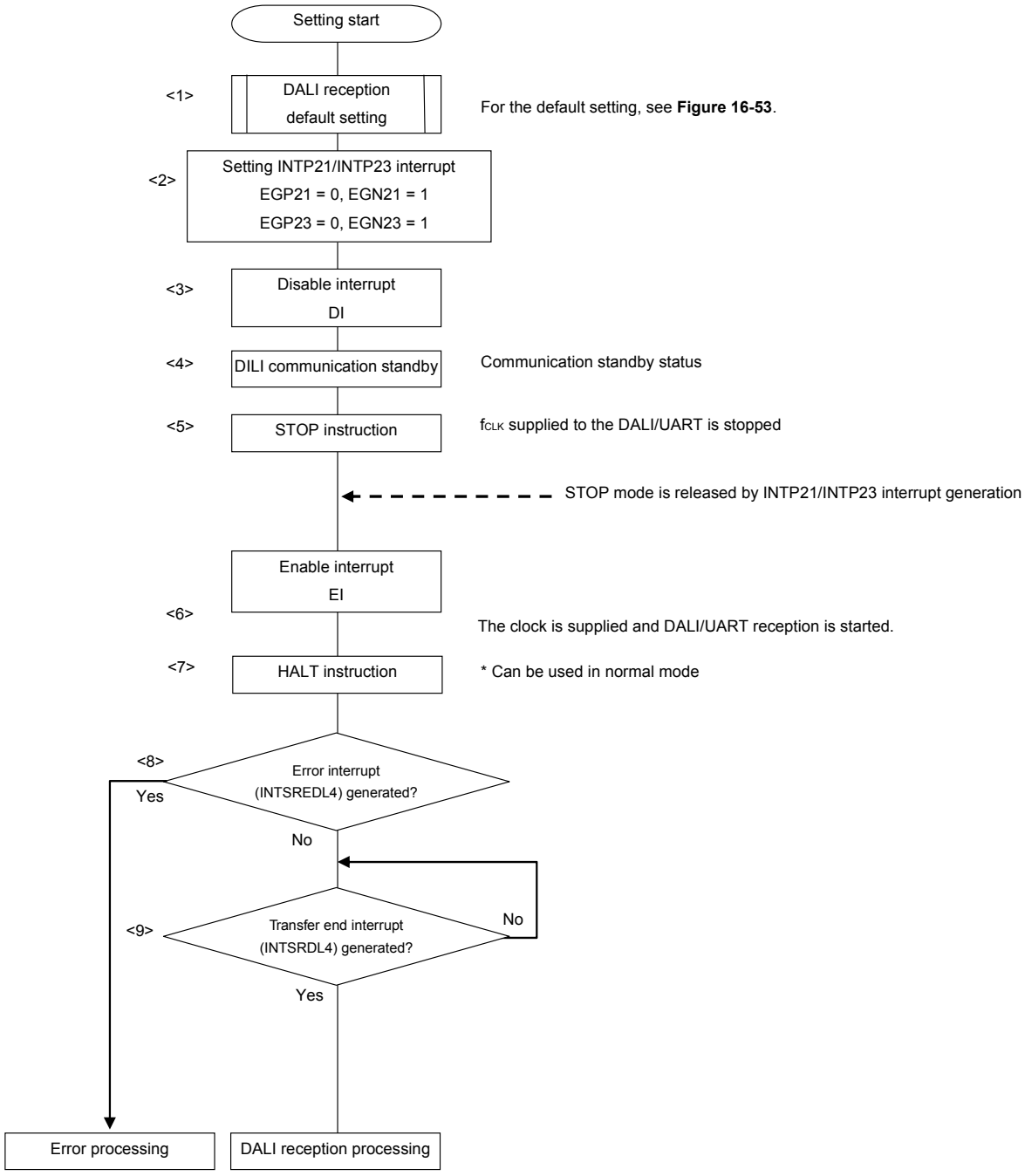
DALI cannot be received in the SNOOZE mode but it can be receive wait at a STOP mode by using the RxD4 pin input with the interrupt function of INTP21 or INTP23. As a result, power-saving communication can be realized in the same manner as in the SNOOZE mode.

Figure 16-1. Timing Chart of Returning from STOP Mode



Remark <1> to <9> in the figure correspond to <1> to <9> in **Figure 16-59. Flowchart of Returning from STOP Mode for Reception**.

Figure 16-2. Flowchart of Returning from STOP Mode for Reception



Remarks 1. <1> to <9> in the figure correspond to <1> to <9> in **Figure 16-58. Timing Chart of Returning from STOP Mode**.

2. Keep SWC4 bit at 0 during use.

Figure 20-5. Format of Priority Specification Flag Registers

Incorrect:

Figure 20-5. Format of Priority Specification Flag Registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H) (38-pin) (2/2)

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR01H	TMPR004	PPR020 PPR120	SRDLPR04 SREDLPR04	STDLPR04	1	ITPR0	RTCPR0	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR11H	TMPR104	PPR022 PPR122	SRDLPR14 SREDLPR14	STDLPR14	1	ITPR1	RTCPR1	ADPR1

Correct:

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR01H	TMPR004	PPR020 PPR022	SRDLPR04 SREDLPR04	STDLPR04	1	ITPR0	RTCPR0	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR11H	TMPR104	PPR022 PPR120	SRDLPR14 SREDLPR14	STDLPR14	1	ITPR1	RTCPR1	ADPR1

21.2.2 STOP mode

Incorrect:

Figure 21-5. STOP Mode Release by Interrupt Request Generation

(1) When high-speed system clock (X1 oscillation) is used as CPU clock
Note 2. STOP mode release time
Supply of the clock is stopped: 18.96 μ s to "whichever is longer 28.95 μ s and the oscillation stabilization time (set by OSTS)"
Wait
・When vectored interrupt servicing is carried out: 10 to 11 clocks
・When vectored interrupt servicing is not carried out: 4 to 5 clocks

(2) When high-speed system clock (external clock input) is used as CPU clock
(3) When high-speed on-chip oscillator clock is used as CPU clock
:
(omitted)
:

Note 2. STOP mode release time
Supply of the clock is stopped: 19.08 to 32.99 μs
Wait
・ When vectored interrupt servicing is carried out: 7 clocks
・ When vectored interrupt servicing is not carried out: 1 clock

Correct:

Figure 21-5. STOP Mode Release by Interrupt Request Generation

(1) When high-speed on-chip oscillator clock is used as CPU clock

Note 2. STOP mode release time
Supply of the clock is stopped:18 μs to "whichever is longer 65 μs and the oscillation stabilization time (set by OSTS)"
Wait
•When vectored interrupt servicing is carried out: 10 to 11 clocks
•When vectored interrupt servicing is not carried out: 4 to 5 clocks

(2) When high-speed system clock (X1 oscillation) is used as CPU clock
(3) When high-speed system clock (external clock input) is used as CPU clock
:
(omitted)
:

Note 2. STOP mode release time
Supply of the clock is stopped: 18 to 65 μs
Wait
• When vectored interrupt servicing is carried out: 7 clocks
• When vectored interrupt servicing is not carried out: 1 clock

21.2.3 SNOOZE mode

Incorrect:

In SNOOZE mode transition, wait status to be only following time.
From STOP to SNOOZE
HS (High-speed main) mode : 18.96 to 28.95 µs
LS (Low-speed main) mode : 20.24 to 28.95 µs

From SNOOZE to normal operation
• When vectored interrupt servicing is carried out
HS (High-speed main) mode : 6.79 to 12.4 µs + 7 clocks
LS (Low-speed main) mode : 2.58 to 7.8 µs + 7 clocks
• When vectored interrupt servicing is not carried out:
HS (High-speed main) mode : 6.79 to 12.4 µs + 1 clock
LS (Low-speed main) mode : 2.58 to 7.8 µs + 1 clock

Correct:

In SNOOZE mode transition, wait status to be only following time.
Transition time from STOP mode to SNOOZE mode: 18 to 65 µs

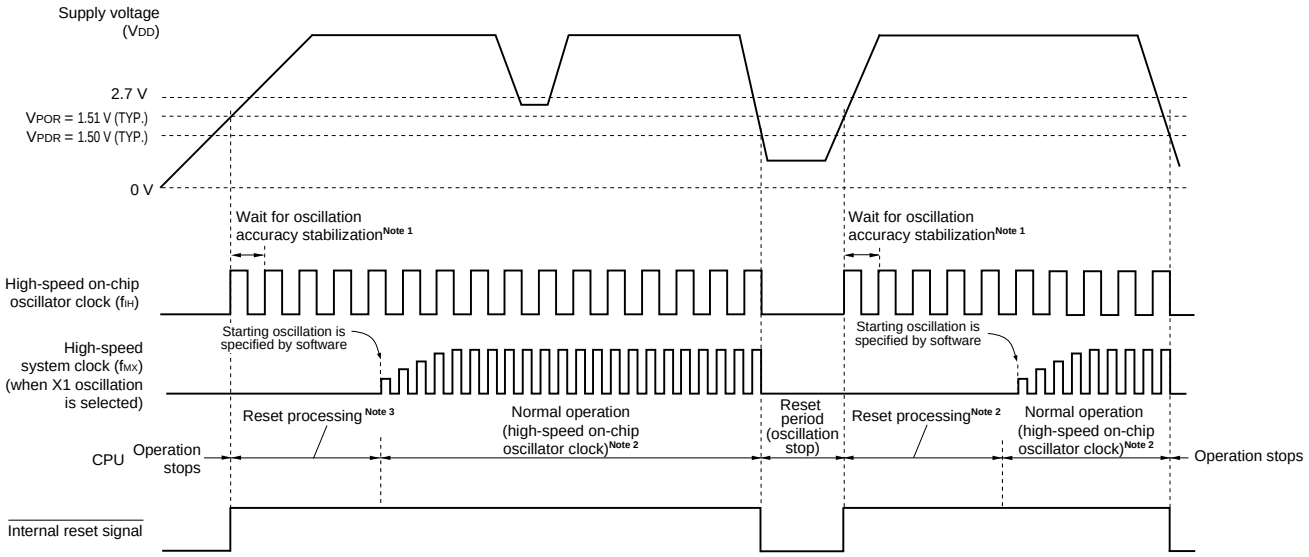
Transition time from SNOOZE mode to normal operation:
• When vectored interrupt servicing is carried out:
HS (High-speed main) mode: 4.99 to 9.44 µs + 7 clocks
LS (Low-speed main) mode: 1.10 to 5.08 µs + 7 clocks
• When vectored interrupt servicing is not carried out:
HS (High-speed main) mode: 4.99 to 9.44 µs + 1 clock
LS (Low-speed main) mode: 1.10 to 5.08 µs + 1 clock

Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector

Timing diagrams and Notes are revised.

Incorrect:

(1) When LVD is OFF (option byte 000C1H: VPOC2 = 1)



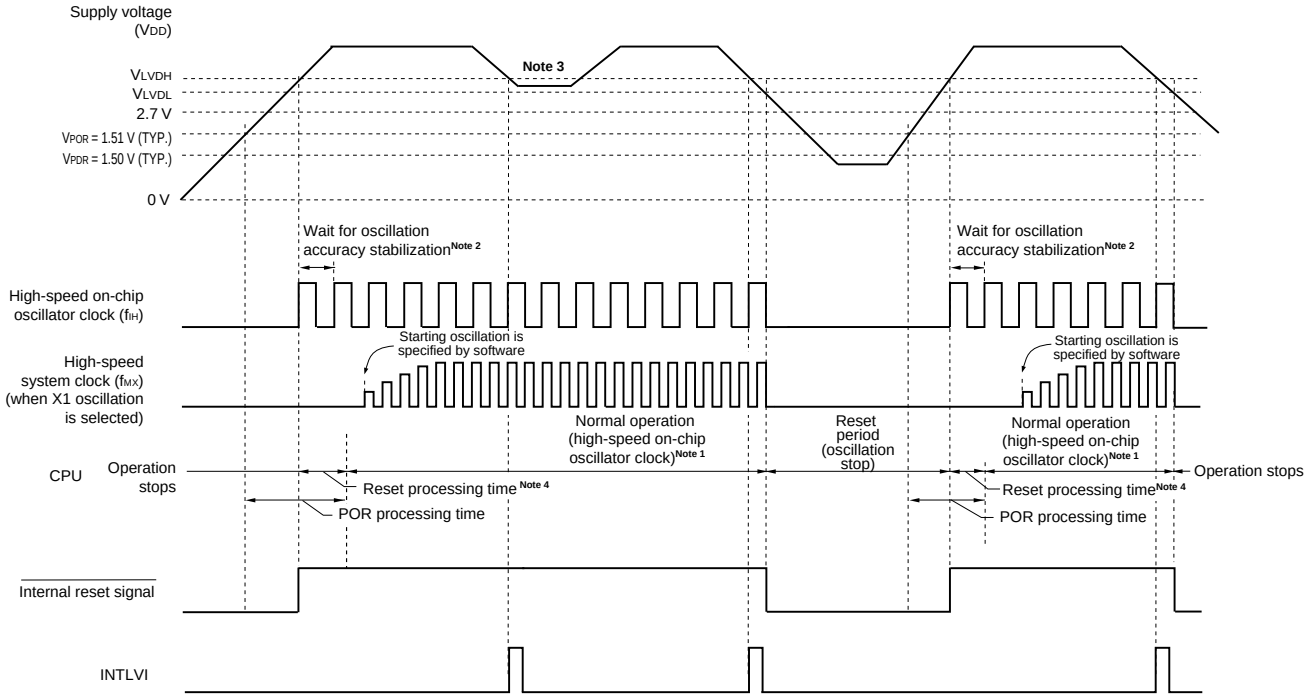
Notes 1. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

2. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

3. Reset processing time: 265 to 407 μs

Remark VPOR: POR power supply rise detection voltage
VPDR: POR power supply fall detection voltage

(2) When LVD is interrupt & reset mode (option byte 000C1: LVIMDS1, LVIMDS0 = 1, 0)



Notes 1. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

2. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

3. After the first interrupt request signal (INTLVI) is generated, the LVIL and LVIMD bits of the voltage detection level register (LVIS) are automatically set to 1. If the operating voltage returns to 2.7 V or higher without falling below the voltage detection level (VLVDL), after INTLVI is generated, perform the required backup processing, and then use software to specify the initial settings in order (see **Figure 24-8. Initial Setting of Interrupt and Reset Mode**).

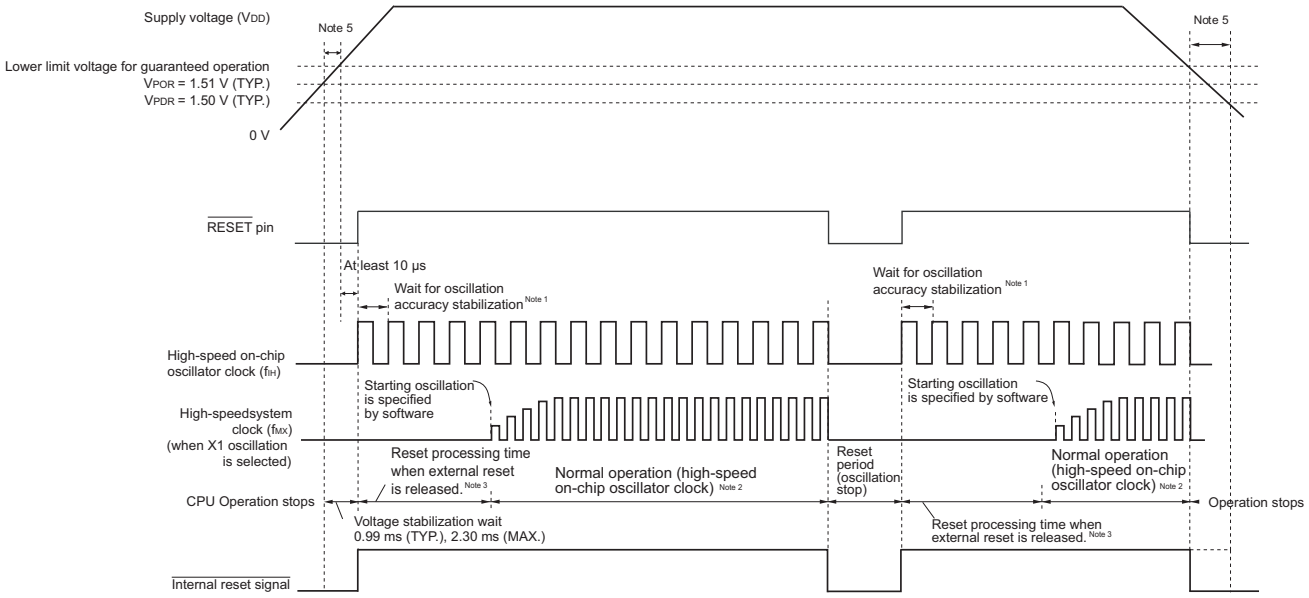
4. Reset processing time: 497 to 720 μs

Remark VLVDH, VLVDL: LVD detection voltage
VPOR: POR power supply rise detection voltage
VPDR: POR power supply fall detection voltage

Correct:

Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (1/3)

(1) When the externally input reset signal on the RESET pin is used



Notes 1. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

2. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

3. The time until normal operation starts includes the following reset processing time when the external reset is released (after the first release of POR) after the RESET signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.51 V, typ.) is reached.
   Reset processing time when the external reset is released is shown below.
   After the first release of POR: 0.672 ms (typ.), 0.832 ms (max.) (When the LVD is in use)
   0.399 ms (typ.), 0.519 ms (max.) (When the LVD is off)

4. Reset processing time when the external reset is released after the second release of POR is shown below.
   After the second release of POR: 0.531 ms (typ.), 0.675 ms (max.) (when the LVD is in use)
   0.259 ms (typ.), 0.362 ms (max.) (when the LVD is off)

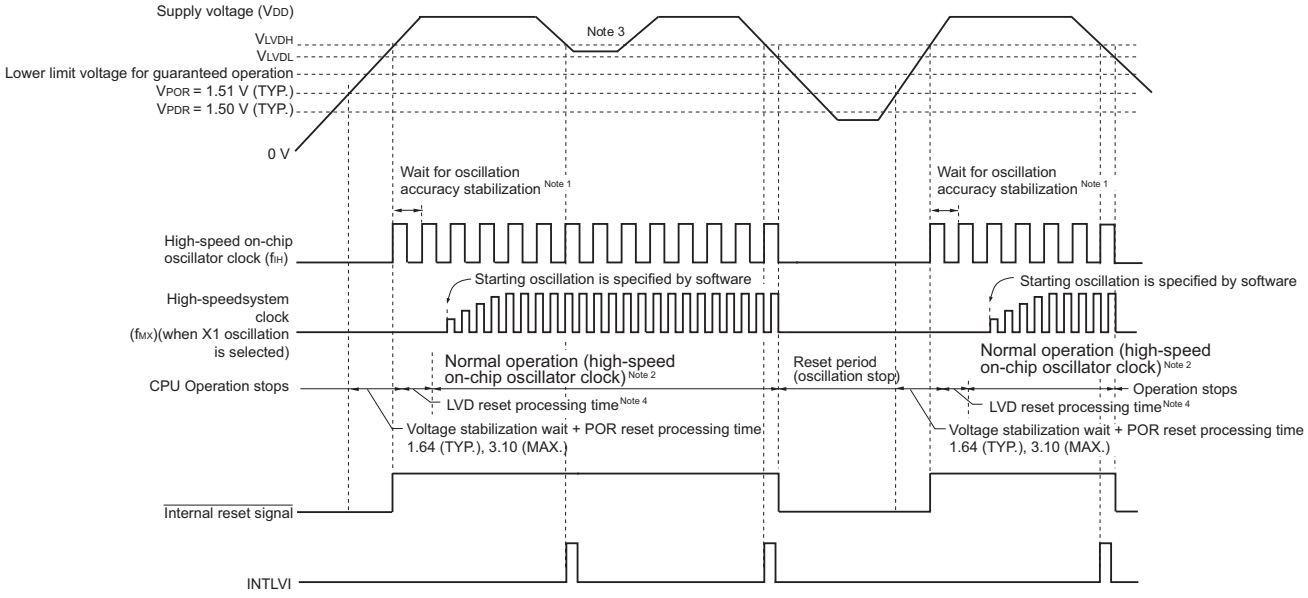
5. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 32.4 or 33.4 AC Characteristics. This is done by controlling the externally input reset signal. After power supply is turned off, this LSI should be placed in the STOP mode, or in the reset state by utilizing the voltage detection circuit or externally input reset signal, before the voltage falls below the operating range. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

Remark VPOR: POR power supply rise detection voltage
VPDR: POR power supply fall detection voltage

Caution For power-on reset, be sure to use the externally input reset signal on the RESET pin when the LVD is off. For details, see CHAPTER 21 VOLTAGE DETECTOR.

Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (2/3)

(2) LVD interrupt & reset mode (option byte 000C1: LVIMDS1, LVIMDS0 = 1, 0)



Notes 1. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

2. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

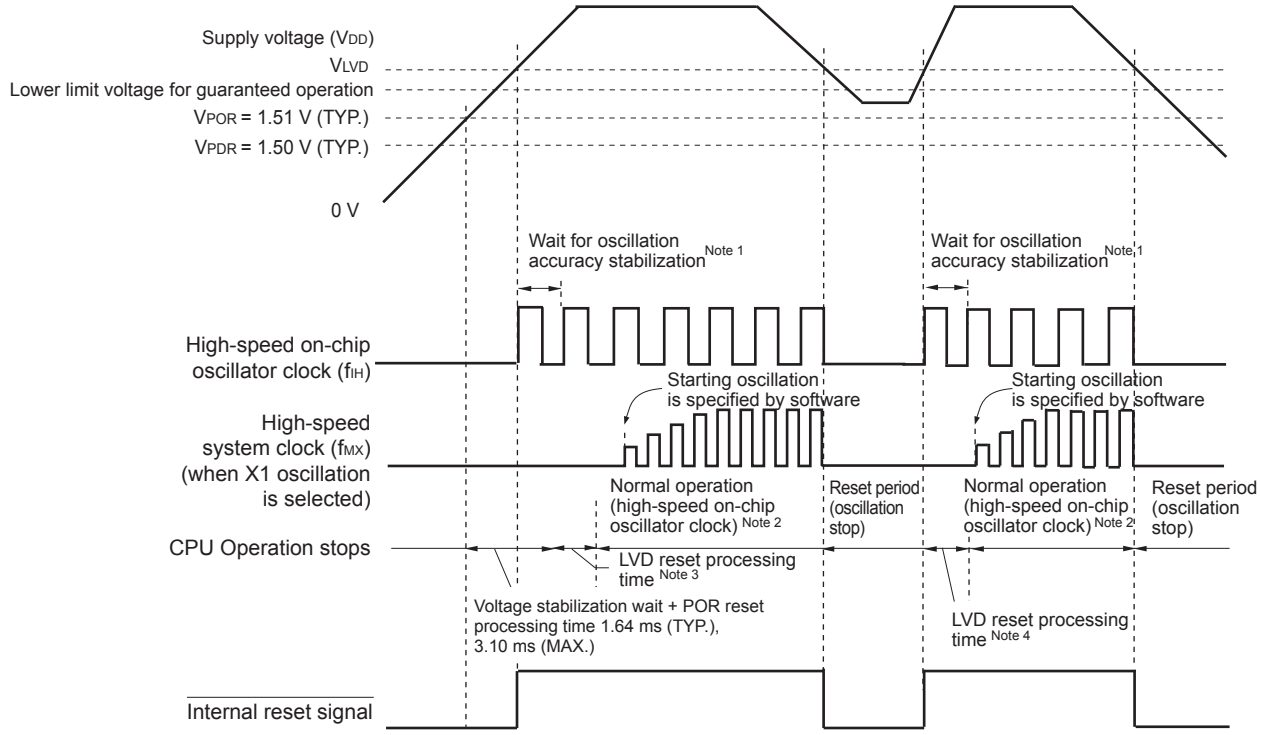
3. After the interrupt request signal (INTLVI) is generated, the LVIL and LVIMD bits of the voltage detection level register (LVIS) are automatically set to 1. After INTLVI is generated, appropriate settings should be made according to Figure 21-8 Processing Procedure After an Interrupt Is Generated and Figure 21-9 Initial Setting of Interrupt and Reset Mode, taking into consideration that the supply voltage might return to the high voltage detection level (VLVDH) or higher without falling below the low voltage detection level (VLVDL).

4. The time until normal operation starts includes the following LVD reset processing time after the LVD detection level (VLVDH) is reached as well as the voltage stabilization wait + POR reset processing time after the VPOR (1.51 V, typ.) is reached.
LVD reset processing time: 0 ms to 0.0701 ms (max.)

Remark VLVDH, VLVDL: LVD detection voltage
VPOR: POR power supply rise detection voltage
VPDR: POR power supply fall detection voltage

Figure 23-2. Timing of Generation of Internal Reset Signal by Power-on-reset Circuit and Voltage Detector (3/3)

(3) LVD reset mode (option byte 000C1H: LVIMDS1 = 1, LVIMDS0 = 1)



Notes 1. The internal reset processing time includes the oscillation accuracy stabilization time of the high-speed on-chip oscillator clock.

2. The high-speed on-chip oscillator clock and a high-speed system clock or subsystem clock can be selected as the CPU clock. To use the X1 clock, use the oscillation stabilization time counter status register (OSTC) to confirm the lapse of the oscillation stabilization time. To use the XT1 clock, use the timer function for confirmation of the lapse of the stabilization time.

3. The time until normal operation starts includes the following LVD reset processing time after the LVD detection level (VLVD) is reached as well as the voltage stabilization wait + POR reset processing time after the VPOR (1.51 V, typ.) is reached.
   LVD reset processing time: 0 ms to 0.0701 ms (max.)

4. When the power supply voltage is below the lower limit for operation and the power supply voltage is then restored after an internal reset is generated only by the voltage detector (LVD), the following LVD reset processing time is required after the LVD detection level (VLVD) is reached.
   LVD reset processing time: 0.0511 ms (typ.), 0.0701 ms (max.)

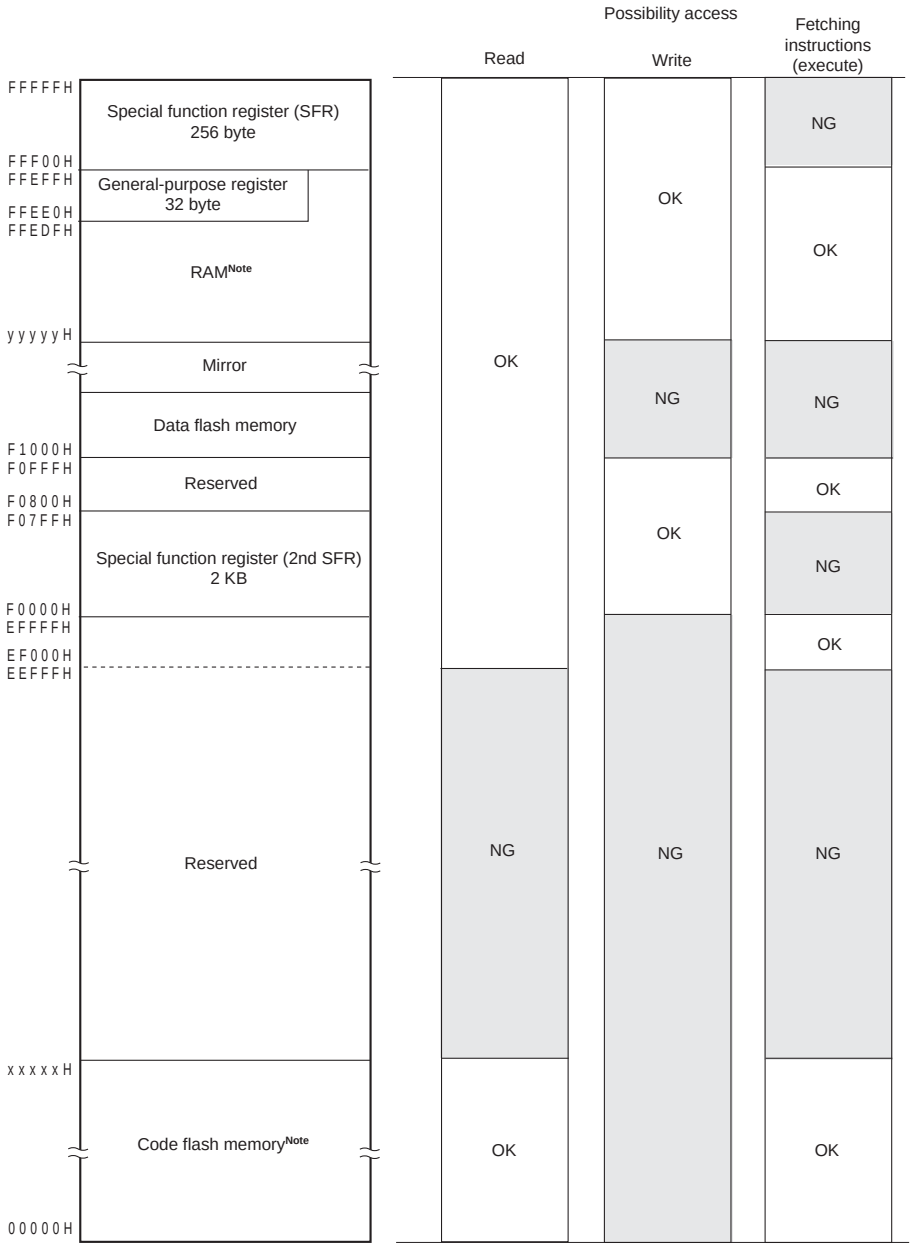
Remarks 1. VLVDH, VLVDL: LVD detection voltage
   VPOR: POR power supply rise detection voltage
   VPDR: POR power supply fall detection voltage

2. When the LVD interrupt mode is selected (option byte 000C1H: LVIMD1 = 0, LVIMD0 = 1), the time until normal operation starts after power is turned on is the same as the time specified in Note 3 of Figure 23-2 (3).

25.3.6 Invalid memory access detection function

Incorrect:

Figure 25-11. Invalid Access Detection Area

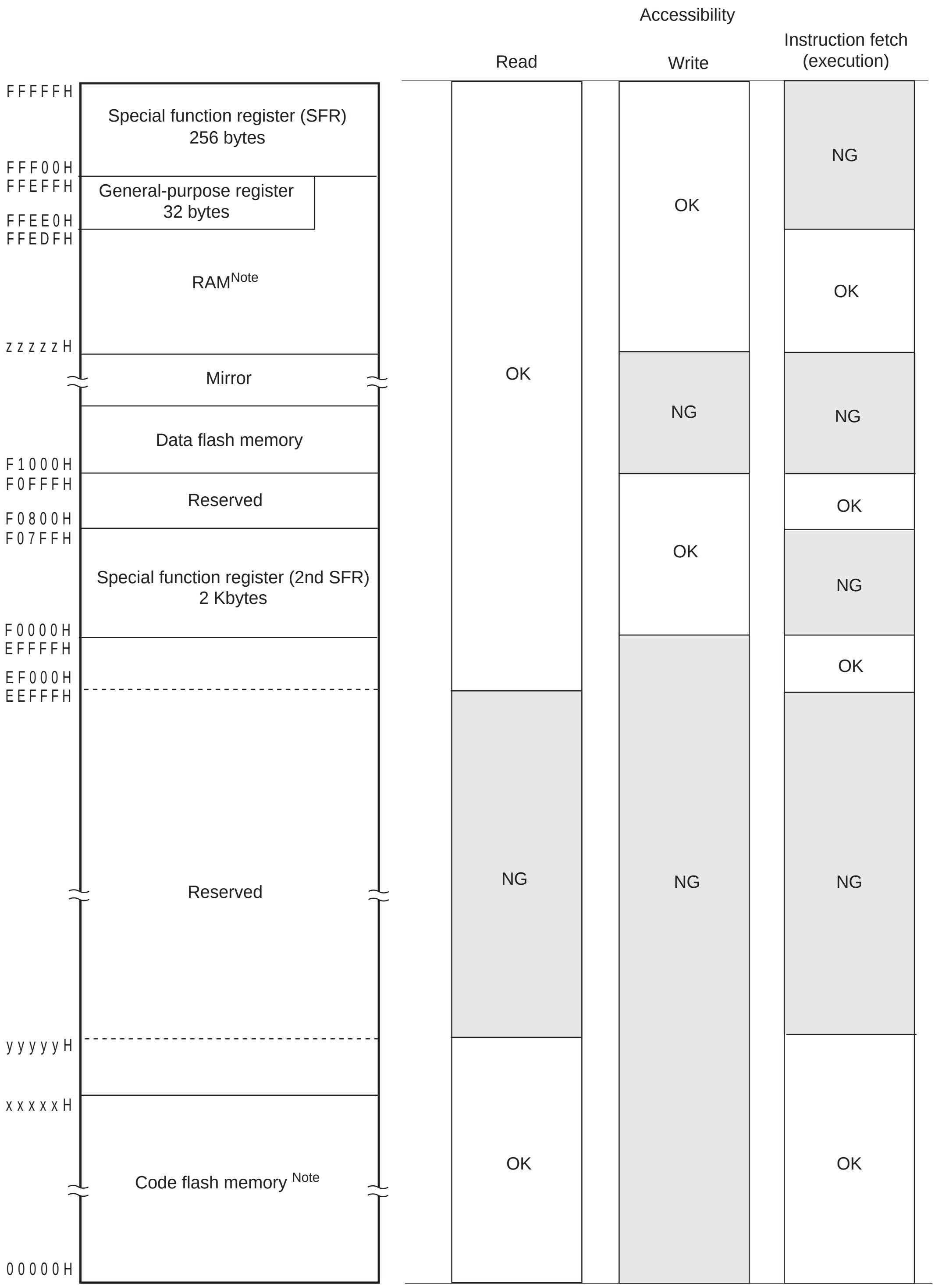


Note Code flash memory and RAM address of each product are as follows.

Products	Code Fash Memory (00000H to xxxxxH)	RAM (yyyyyH to FFEFFH)
R5F1076C, R5F107AC	32768 × 8 bit (00000H to 07FFFH)	2048 × 8 bit (FF700H to FFEFFH)
R5F107AE, R5F107DE	65536 × 8 bit (00000H to 0FFFFH)	4096 × 8 bit (FEF00H to FFEFFH)

Correct:

Figure 25-11. Invalid access detection area



Note The following table lists the code flash memory, RAM, and lowest detection address for each product:

Products	Code flash memory (00000H to xxxxxH)	RAM (zzzzzH to FFEFFH)	Detected lowest address for read/instruction fetch (execution) (yyyyyH)
R5F1076C, R5F107AC	32768 × 8 bit (00000H to 07FFFH)	2048 × 8 bit (FF700H to FFEFFH)	10000H
R5F107AE, R5F107DE	65536 × 8 bit (00000H to 0FFFFH)	4096 × 8 bit (FEF00H to FFEFFH)	10000H

27.3 Format of On-chip Debug Option Byte

Old:

Figure 27-3. Format of Option Byte (000C2H/010C2H)

Address: 000C2H/010C2H[Note]

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

CMODE1	CMODE0	Setting of flash operation mode		
			Operating frequency range	Operating voltage range
1	0	LS (low speed main) mode	1 to 8 MHz	2.7 to 5.5 V
1	1	HS (high speed main) mode	1 to 32 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

CMODE1	CMODE0	Setting of flash operation mode
1	0	LS (low speed main) mode
1	1	HS (high speed main) mode
Other than above		Setting prohibited

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator
1	0	0	0	32 MHz
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
1	0	1	1	4 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

Note Set the same value as 000C2H to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

New:

Address: 000C2H/010C2H[Note]

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

CMODE1	CMODE0	Setting of flash operation mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low voltage main) mode	1 to 4 MHz	1.6 to 5.5 V
1	0	LS (low speed main) mode	1 to 8 MHz	1.8 to 5.5 V
1	1	HS (high speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 32 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator
1	0	0	0	32 MHz
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
0	0	1	0	6 MHz
1	0	1	1	4 MHz
0	0	1	1	3 MHz
1	1	0	0	2 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

Note Set the same value as 000C2H to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

Cautions 1. Be sure to set bit 5 to “1" and bit 4 to “0”

2. The ranges of operation frequency and operation voltage vary depending on the flash operation mode. For details, see 32.4 and 33.4 AC Characteristics.

28.3.1 Data flash overview

Caution added

Old:

An overview of the data flash memory is provided below.

:
(omitted)
:

New:

An overview of the data flash memory is provided below.

・The user program can rewrite the data flash memory by using the flash data library. For details, refer to RL78 Family Flash Data Library User's Manual.

28.6 Flash Memory Programming by Self-Programming

Incorrect:

28.6 Flash Memory Programming by Self-Programming

The RL78/I1A supports a self-programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the RL78/I1A self-programming library, it can be used to upgrade the program in the field.

Cautions 1. The self-programming function cannot be used when the CPU operates with the subsystem clock.

2. To prohibit an interrupt during self-programming, in the same way as in the normal operation mode, execute the self-programming library in the state where the IE flag is cleared (0) by the DI instruction. To enable an interrupt, clear (0) the interrupt mask flag to accept in the state where the IE flag is set (1) by the EI instruction, and then execute the self-programming library.

3. When enabling RAM parity error resets (RPERDIS = 0), be sure to initialize the RAM area to use +10 bytes before overwriting.

Correct:

28.6 Flash Memory Programming by Self-Programming

The RL78/I1A supports a self-programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the RL78/I1A self-programming library, it can be used to upgrade the program in the field.

Cautions 1. The self-programming function cannot be used when the CPU operates with the subsystem clock.

2. To prohibit an interrupt during self-programming, in the same way as in the normal operation mode, execute the self-programming library in the state where the IE flag is cleared (0) by the DI instruction. To enable an interrupt, clear (0) the interrupt mask flag to accept in the state where the IE flag is set (1) by the EI instruction, and then execute the self-programming library.

3. The high-speed on-chip oscillator should be kept operating during self-programming. If it is kept stopping, the high-speed on-chip oscillator clock should be operated (HIOSTOP = 0). The flash self-programming library should be executed after 30 μs have elapsed.

32.3.2 Supply current characteristics

Incorrect:

Fixed typo in Note in pages 1059 to 1064.

Correct:

Refer to pages 12 and 17 in Technical Update Exhibit “Chapter 32 ELECTRICAL SPECIFICATIONS (T_A = −40 to + 105°C)” (MCYG-AB-13-0043).

32.5 Peripheral Functions Characteristics

Old:

Specifications changed and LS Mode spec extended in pages 1067 to 1081.

new:

Refer to pages 21 and 35 in Technical Update Exhibit “Chapter 32 ELECTRICAL SPECIFICATIONS (T_A = −40 to + 105°C)” (MCYG-AB-13-0043).

32.6.1 A/D converter characteristics

Incorrect:

The table and notes are changed in pages 1082 to 1085.

Correct:

Refer to pages 36 and 40 in Technical Update Exhibit “Chapter 32 ELECTRICAL SPECIFICATIONS (T_A = −40 to + 105°C)” (MCYG-AB-13-0043).

32.6.2 Temperature sensor characteristics

Incorrect:

Fixed typo and internal reference voltage characteristics added in page 1085

Correct:

Refer to page 41 in Technical Update Exhibit “Chapter 32 ELECTRICAL SPECIFICATIONS (T_A = −40 to + 105°C)” (MCYG-AB-13-0043).

Supply Voltage Rise Time

Old:

Power supply voltage rising slope characteristics added.

New:

Refer to page 44 in Technical Update Exhibit “Chapter 32 ELECTRICAL SPECIFICATIONS (T_A = −40 to + 105°C)” (MCYG-AB-13-0043).

32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

Old:

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics specifications extended.

New:

Refer to page 44 in Technical Update Exhibit “Chapter 32 ELECTRICAL SPECIFICATIONS (T_A = −40 to + 105°C)” (MCYG-AB-13-0043).

32.8 Flash Memory Programming Characteristics

Incorrect:

Fixed typo in 32.8 Flash Memory Programming Characteristics in page 1089.

Correct:

Refer to page 45 in Technical Update Exhibit “Chapter 32 ELECTRICAL SPECIFICATIONS (T_A = −40 to + 105°C)” (MCYG-AB-13-0043).

32.9 Timing Specs for Switching Flash Memory Programming Modes

Incorrect:

Fixed typo in 32.9 Timing Specs for Switching Flash Memory Programming Modes in page 1090.

Correct:

Refer to page 45 in Technical Update Exhibit “Chapter 32 ELECTRICAL SPECIFICATIONS (T_A = −40 to + 105°C)” (MCYG-AB-13-0043).

Chapter 33 ELECTRICAL SPECIFICATIONS (T_A = −40 to +125°C)

Old:

Specifications in Chapter 33 ELECTRICAL SPECIFICATIONS (T_A = −40 to +125°C) extended.

New:

Refer to Technical Update Exhibit “Chapter 32 ELECTRICAL SPECIFICATIONS (: T_A = −40 to + 125°C)” (MCYG-AB-13-0044).

To our valued customers:	RL78/I1A Technical Update Exhibit Chapter 32 ELECTRICAL SPECIFICATIONS (T_A = −40 to +105°C)	M C Y G - A B - 1 3 - 0 0 4 3 - 1
		Aug 6, 2013
		Isao Murakami Manager 1st Solution Business Unit General Purpose Solution Business Division Brand Strategy Department 2nd Renesas Electronics Corporation

(Rep. Takao Iwasaki)

Thank you for your continued support for Renesas Electronics products.

Please be advised that the misstatements found in the following User's Manual have been fixed.

The second and following pages in this document include "Chapter 32 ELECTRICAL SPECIFICATIONS (T_A = −40 to +105°C)" which has been updated by the Correction for incorrect description notice RL78/I1A Descriptions in the User's Manual: Hardware Rev.1.00 changed (TN-RL*-A008A/E).

1. Applicable products:

RL78/I1A

R5F1076CGSP, R5F107ACGSP,R5F107AEGSP,R5F107DEGSP

2. Reference documents:

Correction for incorrect description notice RL78/I1A Descriptions in the User's Manual: Hardware Rev.1.00 changed (TN-RL*-A008A/E)

RL78/I1A User's Manual: Hardware Rev.1.00 (R01UH0169EJ01.00)

CHAPTER 32 ELECTRICAL SPECIFICATIONS (T_A = –40 to +105°C)

Target products: T_A = –40 to +105°C

R5F1076CGSP#V0, R5F1076CGSP#X0, R5F107ACGSP#V0, R5F107ACGSP#X0,
R5F107AEGSP#V0, R5F107AEGSP#X0, R5F107DEGSP#V0, R5F107DEGSP#X0

Cautions 1. The RL78/I1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 With functions for each product.

32.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	−0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19	−0.3 to V_{DD} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	−40	mA
		Total of all pins −170 mA	P02, P03, P40, P120	−70	mA
			P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206	−100	mA
	I_{OH2}	Per pin	P20 to P22, P24 to P27	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	40	mA
		Total of all pins 170 mA	P02, P03, P40, P120	70	mA
			P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206	100	mA
	I_{OL2}	Per pin	P20 to P22, P24 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

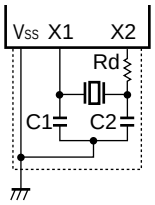
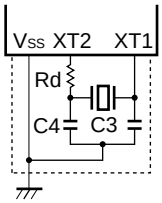
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

32.2 Oscillator Characteristics

32.2.1 X1, XT1 oscillator characteristics

(T_A = −40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Recommended Circuit	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator/ crystal resonator			1.0		20.0	MHz
XT1 clock oscillation frequency (f_{XT})Note	Crystal resonator			32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

32.2.2 On-chip oscillator characteristics

(T_A = −40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Note 1]	f_{IH}		1		32	MHz
High-speed on-chip oscillator clock frequency accuracy[Note 2]		T_A = −20 to 85°C	−1		+1	%
		T_A = −40 to 105°C	−1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			−15		+15	%

Notes 1. Frequency can be selected in a high-speed on-chip oscillator. Selected by bits 0 to 3 of option byte (000C2H/010C2H).

2. This indicates the oscillator characteristics only. See AC Characteristics for instruction execution time.

32.2.3 PLL characteristics

(T_A = −40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PLL input clock frequency[Note]	f_{PLLIN}	High-speed system clock is selected (f_{MX} = 4 MHz)	3.94	4.00	4.06	MHz
		High-speed on-chip oscillator clock is selected (f_{IH} = 4 MHz)	3.94	4.00	4.06	MHz
PLL output clock frequency[Note]	f_{PLL}		f_{PLLIN} × 16			MHz

Note This only indicates the oscillator characteristics. See AC Characteristics for instruction execution time.

32.3 DC Characteristics

32.3.1 Pin characteristics

(T_A = −40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	4.0 V ≤ V_{DD} ≤ 5.5 V			−3.0[Note 2]	mA
			2.7 V ≤ V_{DD} < 4.0 V			−1.0	mA
		Total of P02, P03, P40, P120 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			−12.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−4.0	mA
		Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			−30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			−30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−14.0	mA
	I_{OH2}	Per pin for P20 to P22, P24 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V			−0.1[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.7 V ≤ V_{DD} ≤ 5.5 V			−0.7	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = −10.0 mA

Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P02, P10 to P12 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5[Note 2]	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.5[Note 2]	mA
		Total of P02, P03, P40, P120 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			7.5	mA
		Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			17.5	mA
		Total of all pins (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			25.0	mA
	I_{OL2}	Per pin for P20 to P22, P24 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V			0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.7 V ≤ V_{DD} ≤ 5.5 V			2.8	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = −10.0 mA

Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ − 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, $\overline{\text{RESET}}$	Normal input buffer	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P03, P10, P11	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.1		V_{DD}	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 2.7 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
Input voltage, low	V_{IL1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, $\overline{\text{RESET}}$	Normal input buffer	0		0.2V_{DD}	V
	V_{IL2}	P03, P10, P11	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 2.7 V ≤ V_{DD} < 3.3 V	0		0.32	V

Caution The maximum value of V_{IH} of pins P02, P10 to P12 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = −3.0 mA	V_{DD} − 0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = −1.0 mA	V_{DD} − 0.5			V
	V_{OH2}	P20 to P22, P24 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = −100 μA	V_{DD} − 0.5			V
Output voltage, low	V_{OL1}	P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
	V_{OL2}	P20 to P22, P24 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V

Caution P02, P10 to P12 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P137, P147, P200 to P206, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P137, P147, P200 to P206, $\overline{\text{RESET}}$	$V_I = V_{SS}$				−1	μA
	I_{LIL2}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{SS}$	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
On-chip pll-up resistance	R_U	P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	$V_I = V_{SS}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

32.3.2 Supply current characteristics

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (high-speed main) mode[Note 5]	f_{IH} = 32 MHz[Note 3]	V_{DD} = 5.0 V		5.0	7.5	mA
					V_{DD} = 3.0 V		5.0	7.5	mA
				f_{IH} = 24 MHz[Note 3]	V_{DD} = 5.0 V		3.9	5.8	mA
					V_{DD} = 3.0 V		3.9	5.8	mA
				f_{IH} = 16 MHz[Note 3]	V_{DD} = 5.0 V		2.9	4.2	mA
					V_{DD} = 3.0 V		2.9	4.2	mA
			LS (low-speed main) mode[Note 5]	f_{IH} = 8 MHz[Note 3], T_A = –40 to + 85°C	V_{DD} = 3.0 V		1.3	2.0	mA
			HS (high-speed main) mode[Note 5]	f_{MX} = 20 MHz[Note 2], V_{DD} = 5.0 V	Square wave input		3.2	4.9	mA
					Resonator connection		3.3	5.0	mA
				f_{MX} = 20 MHz[Note 2], V_{DD} = 3.0 V	Square wave input		3.2	4.9	mA
					Resonator connection		3.3	5.0	mA
				f_{MX} = 10 MHz[Note 2], V_{DD} = 5.0 V	Square wave input		2.0	2.9	mA
					Resonator connection		2.0	2.9	mA
				f_{MX} = 10 MHz[Note 2], V_{DD} = 3.0 V	Square wave input		2.0	2.9	mA
					Resonator connection		2.0	2.9	mA
			LS (low-speed main) mode[Note 5]	f_{MX} = 8 MHz[Note 2], V_{DD} = 3.0 V, T_A = –40 to + 85°C	Square wave input		1.2	1.8	mA
					Resonator connection		1.2	1.8	mA
			HS (high-speed main) mode[Note 5]	f_{IH} = 4 MHz[Note 3] f_{PLL} = 64 MHz, f_{CLK} = 32 MHz	V_{DD} = 5.0 V		5.4	8.5	mA
					V_{DD} = 3.0 V		5.4	8.5	mA
				f_{IH} = 4 MHz[Note 3] f_{PLL} = 64 MHz, f_{CLK} = 16 MHz	V_{DD} = 5.0 V		3.3	5.7	mA
					V_{DD} = 3.0 V		3.3	5.7	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz[Note 4] T_A = –40°C	Square wave input		4.2	6.0	μA
					Resonator connection		4.4	6.2	μA
				f_{SUB} = 32.768 kHz[Note 4] T_A = +25°C	Square wave input		4.2	6.0	μA
					Resonator connection		4.4	6.2	μA
				f_{SUB} = 32.768 kHz[Note 4] T_A = +50°C	Square wave input		4.3	7.2	μA
					Resonator connection		4.5	7.4	μA
				f_{SUB} = 32.768 kHz[Note 4] T_A = +70°C	Square wave input		4.4	8.1	μA
					Resonator connection		4.6	8.3	μA
				f_{SUB} = 32.768 kHz[Note 4] T_A = +85°C	Square wave input		5.2	11.4	μA
					Resonator connection		5.4	11.6	μA
				f_{SUB} = 32.768 kHz[Note 4] T_A = +105°C	Square wave input		6.9	20.8	μA
					Resonator connection		7.1	21.0	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz

LS (low-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = −40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	HS (high-speed main) mode[Note 7]	f_{IH} = 32 MHz[Note 4]	V_{DD} = 5.0 V		0.72	2.9	mA
					V_{DD} = 3.0 V		0.72	2.9	mA
				f_{IH} = 24 MHz[Note 4]	V_{DD} = 5.0 V		0.57	2.3	mA
					V_{DD} = 3.0 V		0.57	2.3	mA
				f_{IH} = 16 MHz[Note 4]	V_{DD} = 5.0 V		0.50	1.7	mA
					V_{DD} = 3.0 V		0.50	1.7	mA
			LS (low-speed main) mode[Note 7]	f_{IH} = 8 MHz[Note 4], T_A = −40 to +85°C	V_{DD} = 3.0 V		320	910	μA
			HS (high-speed main) mode[Note 7]	f_{MX} = 20 MHz[Note 3], V_{DD} = 5.0 V	Square wave input		0.40	1.9	mA
					Resonator connection		0.50	2.0	mA
				f_{MX} = 20 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.40	1.9	mA
					Resonator connection		0.50	2.0	mA
				f_{MX} = 10 MHz[Note 3], V_{DD} = 5.0 V	Square wave input		0.24	1.02	mA
					Resonator connection		0.30	1.08	mA
				f_{MX} = 10 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.24	1.02	mA
					Resonator connection		0.30	1.08	mA
			LS (low-speed main) mode[Note 7]	f_{MX} = 8 MHz[Note 3], V_{DD} = 3.0 V, T_A = −40 to +85°C	Square wave input		130	720	μA
					Resonator connection		170	760	μA
			HS (high-speed main) mode[Note 7]	f_{IH} = 4 MHz[Note 4] f_{PLL} = 64 MHz, f_{CLK} = 32 MHz	V_{DD} = 5.0 V		1.15	4.0	mA
					V_{DD} = 3.0 V		1.15	4.0	mA
				f_{IH} = 4 MHz[Note 4] f_{PLL} = 64 MHz, f_{CLK} = 16 MHz	V_{DD} = 5.0 V		0.95	3.2	mA
					V_{DD} = 3.0 V		0.95	3.2	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz[Note 5] T_A = −40°C	Square wave input		0.28	0.70	μA
					Resonator connection		0.47	0.89	μA
				f_{SUB} = 32.768 kHz[Note 5] T_A = +25°C	Square wave input		0.33	0.70	μA
					Resonator connection		0.52	0.89	μA
				f_{SUB} = 32.768 kHz[Note 5] T_A = +50°C	Square wave input		0.41	1.90	μA
					Resonator connection		0.60	2.09	μA
				f_{SUB} = 32.768 kHz[Note 5] T_A = +70°C	Square wave input		0.54	2.80	μA
					Resonator connection		0.73	2.99	μA
				f_{SUB} = 32.768 kHz[Note 5] T_A = +85°C	Square wave input		1.27	6.10	μA
					Resonator connection		1.46	6.29	μA
				f_{SUB} = 32.768 kHz[Note 5] T_A = +105°C	Square wave input		3.04	15.5	μA
					Resonator connection		3.23	15.7	μA
	I_{DD3}[Note 6]	STOP mode[Note 8]	T_A = −40°C				0.18	0.50	μA
			T_A = +25°C				0.23	0.50	μA
			T_A = +50°C				0.27	1.70	μA
			T_A = +70°C				0.44	2.60	μA
			T_A = +85°C				1.17	5.90	μA
			T_A = +105°C				2.94	15.3	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz

LS (low-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = −40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1					0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3					0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4					0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz				0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V			1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V			0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1					75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1					75.0		μA
LVD operating current	I_{LVI} Notes 1, 7					0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 8					2.50	12.2	mA
Programmable gain amplifier operating current	I_{PGA} Note 9			AV_{REFP} = V_{DD} = 5.0 V		0.21	0.31	mA
				AV_{REFP} = V_{DD} = 3.0 V		0.18	0.29	mA
Comparator operating current	I_{CMP} Note 10	When one comparator channel is operating		AV_{REFP} = V_{DD} = 5.0 V		41.4	62	μA
				AV_{REFP} = V_{DD} = 3.0 V		37.2	59	μA
	I_{VREF}	When one internal reference voltage circuit is operating		AV_{REFP} = V_{DD} = 5.0 V		14.8	26	μA
				AV_{REFP} = V_{DD} = 3.0 V		8.9	20	μA
Programmable gain amplifier/ comparator reference current source	I_{IREF} Note 11			AV_{REFP} = V_{DD} = 5.0 V		3.2	5.1	μA
				AV_{REFP} = V_{DD} = 3.0 V		2.9	4.9	μA
BGO operating current	I_{BGO} Note 12					2.50	12.2	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 13			0.50	1.1	mA
			The A/D conversion operations are performed, Standard mode, AV_{REFP} = V_{DD} = 5.0 V			2.0	3.04	mA
		CSI/UART operation				0.70	1.54	mA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Current flowing to the V_{DD}.

2. When the high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the XT1 oscillator and f_{IL} operating current). The current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

8. Current flowing during self-programming operation.

9. Current flowing only to the programmable gain amplifier. The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{PGA}, when the programmable gain amplifier is operating in operating mode or in HALT mode.

10. Current flowing only to the comparator. The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{CMP}, when the comparator is operating.

11. This is the current required to flow to V_{DD} pin of the current circuit that is used as the programmable gain amplifier and the comparator.

12. Current flowing only during data flash rewrite.

13. Refer to **21.3.3 SNOOZE mode** for shift time to the SNOOZE mode.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

5. Example of calculating current value when using programmable gain amplifier and comparator.

Examples 1) TYP. operating current value when three comparator channels, one internal reference voltage generator, and PGA are operating (when AV_{REFP} = V_{DD} = 5.0 V)

I_{CMP} × 3 + I_{VREF} + I_{PGA} + I_{IREF}
= 41.4 [μA] × 3 + 14.8 [μA] × 1 + 210 [μA] + 3.2 [μA]
= 352.2 [μA]

Examples 2) TYP. operating current value when using two comparator channels, without using internal reference voltage generator (when AV_{REFP} = V_{DD} = 5.0 V)

I_{CMP} × 2 + I_{IREF}
= 41.4 [μA] × 2 + 3.2 [μA]
= 86.0 [μA]

32.4 AC Characteristics

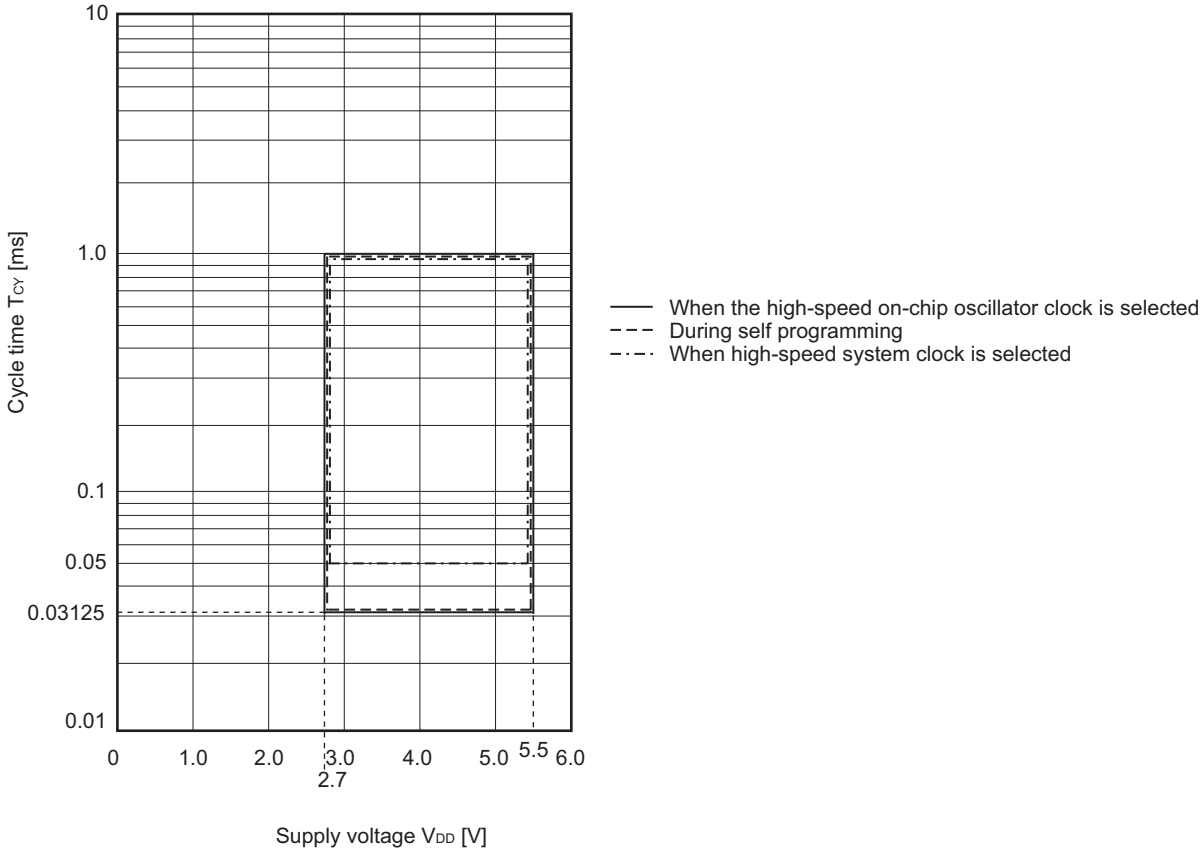
(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode		0.03125		1	μs
			LS (low-speed main) mode	T_A = –40 to +85°C	0.125		1	μs
		Subsystem clock (f_{SUB}) operation			28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode		0.03125		1	μs
			LS (low-speed main) mode	T_A = –40 to +85°C	0.125		1	μs
External system clock frequency	f_{EX}				1.0		20.0	MHz
	f_{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}				24			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI03, TI05, TI06, TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				2/f_{MCK}+10			ns
TO03, TO05, TO06, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TKCO00 to TKCO05 output frequency (When duty = 50%)	f_{TO}	HS (high-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			8	MHz
				2.7 V ≤ V_{DD} < 4.0 V			4	MHz
		LS (low-speed main) mode, T_A = –40 to +85°C		4.0 V ≤ V_{DD} ≤ 5.5 V			4	MHz
				2.7 V ≤ V_{DD} < 4.0 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP3, INTP4, INTP9 to INTP11, INTP20 to INTP23			1			μs
$\overline{RESET}$ low-level width	t_{RSL}				10			μs

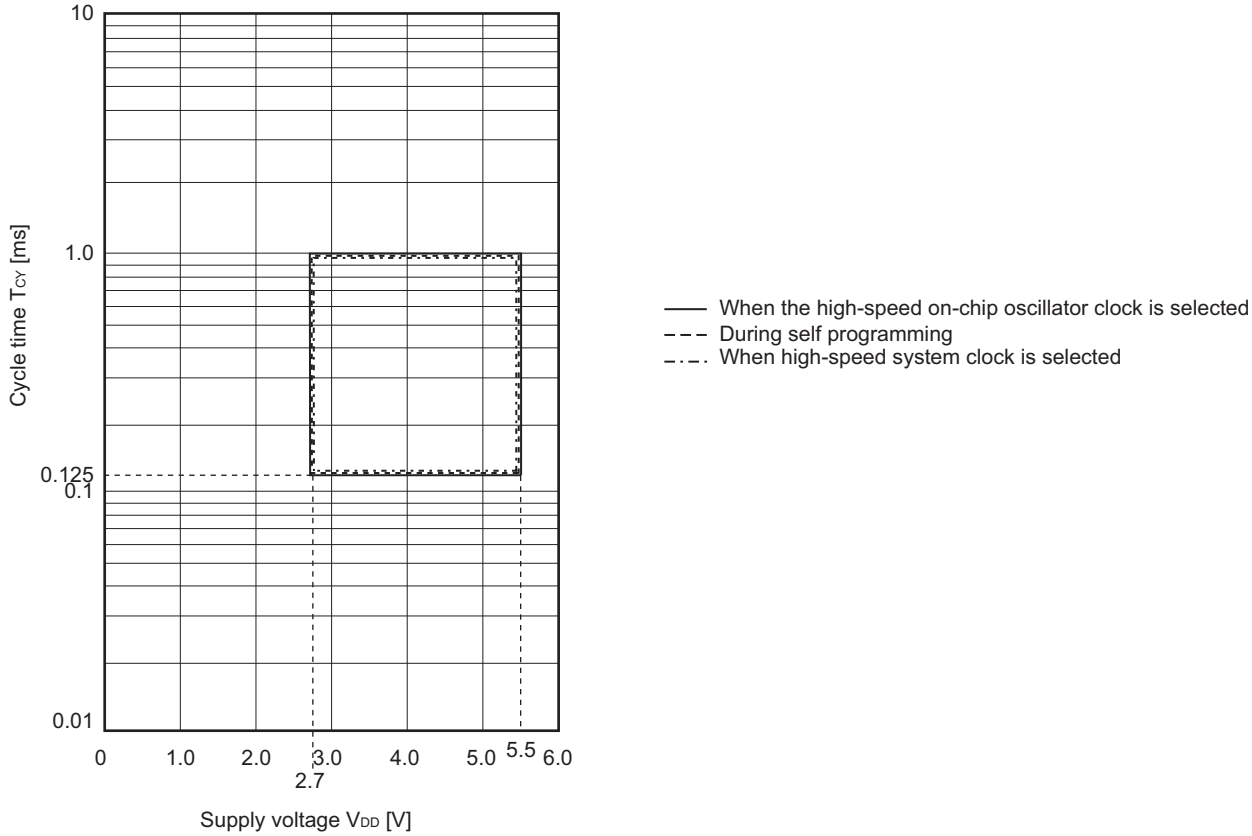
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation

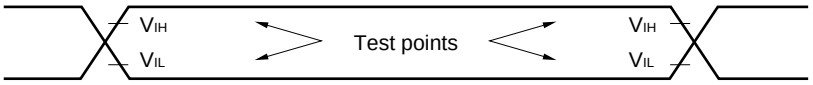
T_{CY} vs V_{DD} (HS (high-speed main) mode)



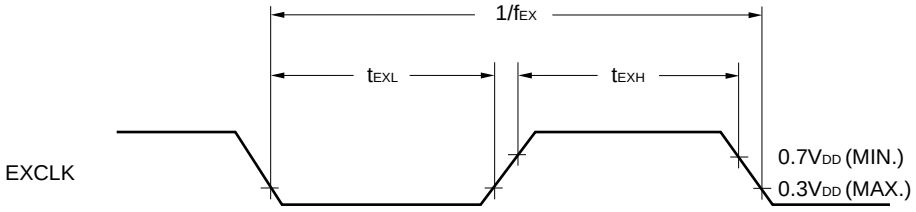
T_{CY} vs V_{DD} (LS (low-speed main) mode)



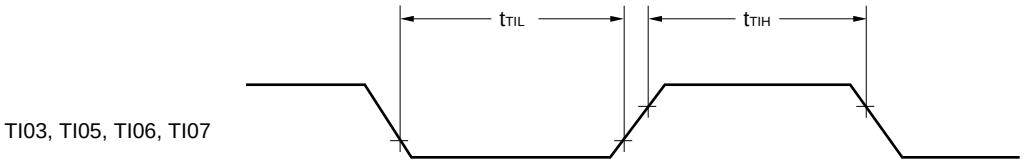
AC Timing Test Points

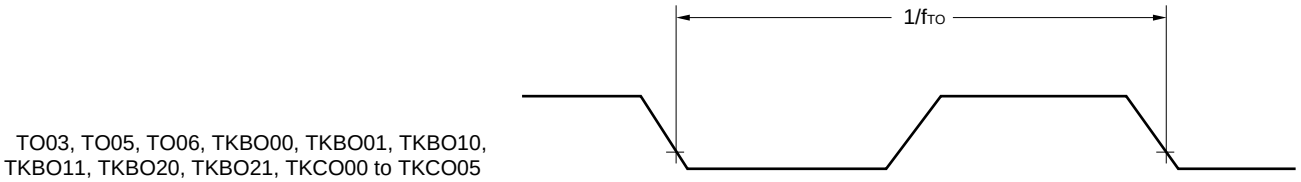


External System Clock Timing

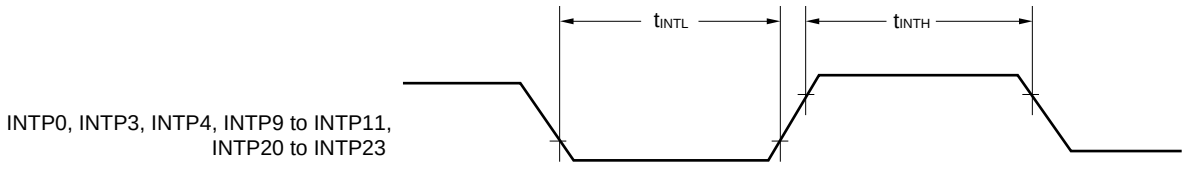


TI/TO Timing

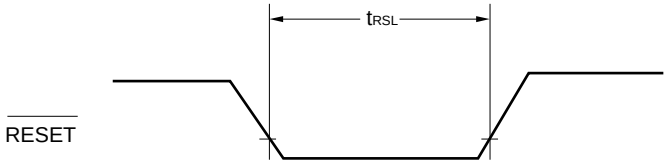




Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



32.5 Peripheral Functions Characteristics

32.5.1 Serial array unit 0, 4 (UART0, UART1, CSI00, DALI/UART4)

(1) During communication at same potential (UART mode)
(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

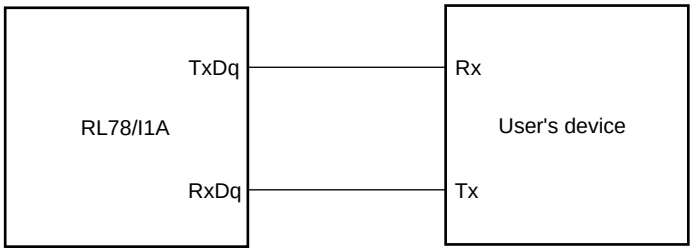
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1		2.7 V≤ V_{DD} ≤ 5.5 V			f_{MCK}/6		f_{MCK}/6	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		5.3		1.3	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

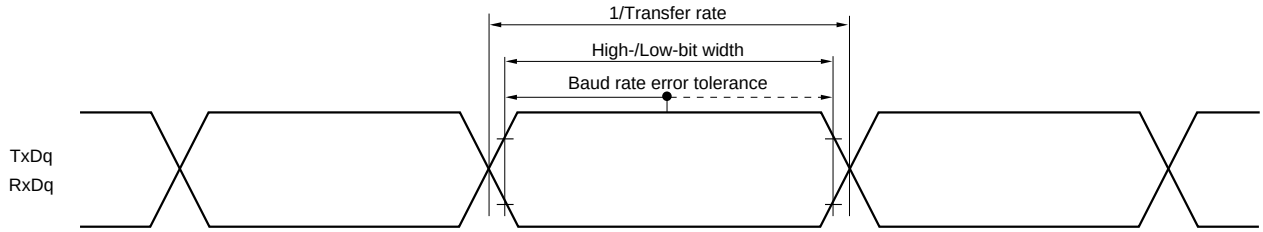
2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V), TA = –40 to +85°C

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	125		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY1}/2 - 12$		$t_{KCY1}/2 - 50$		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY1}/2 - 18$		$t_{KCY1}/2 - 50$		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	44		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	44		110		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}		19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4		25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

5. Operating condtions of LS (low-speed main) mode is T_A = -40 to +85 °C.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		—		ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	16 MHz < f_{MCK}	8/f_{MCK}		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2		t_{KCY2}/2		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}			1/f_{MCK}+20		1/f_{MCK}+30		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK}+31		1/f_{MCK}+31		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4			2/f_{MCK}+ 44		2/f_{MCK}+ 110	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

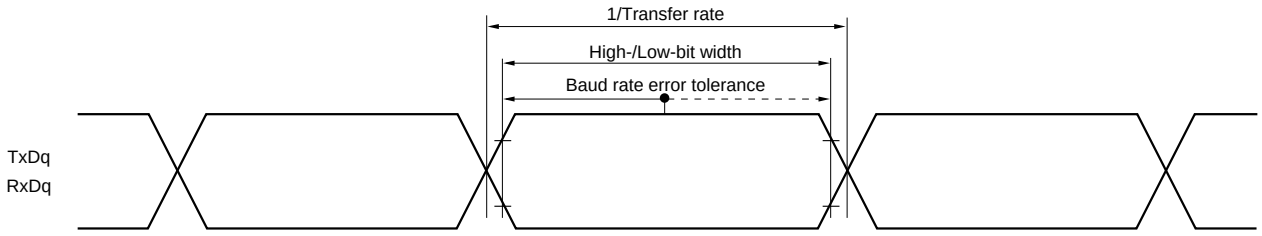
5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

6. Operating condtions of LS (low-speed main) mode is T_A = -40 to +85 °C.

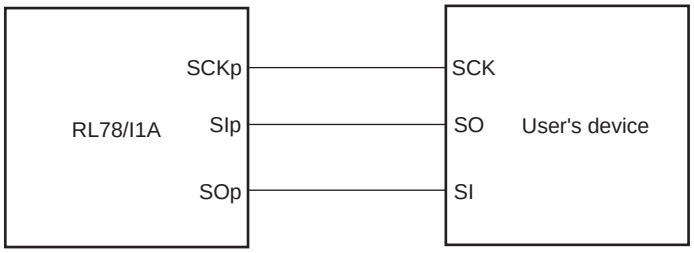
Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

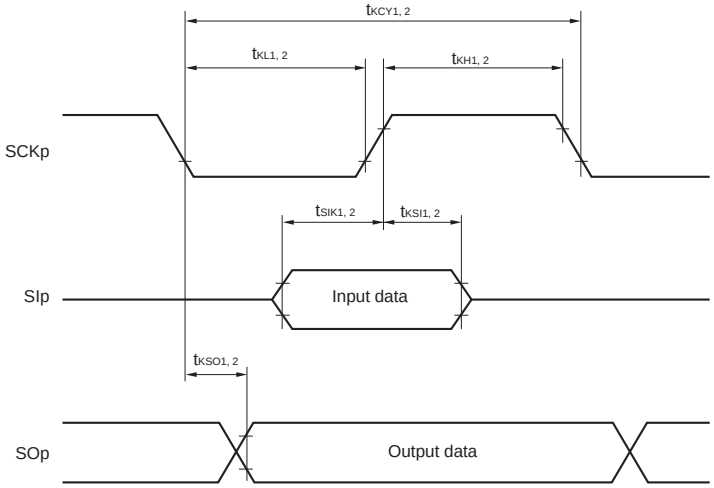
2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))



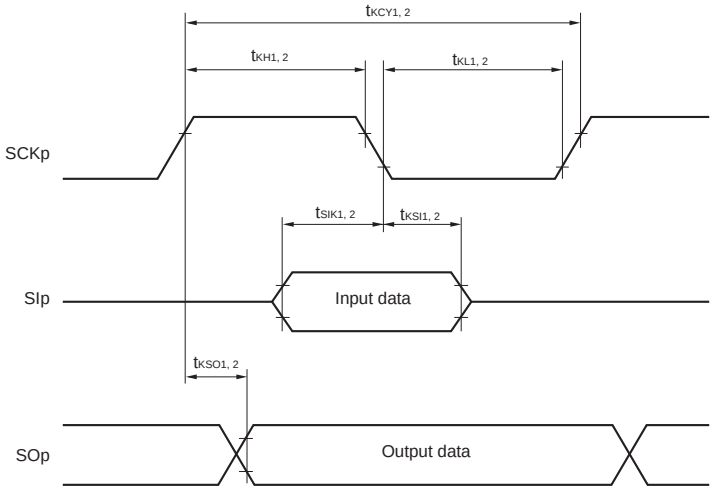
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00)

2. m: Unit number, n: Channel number (mn = 00)

(4) Communication at different potential (2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V,2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		5.3		1.3	Mbps
			2.7 V ≤ V_{DD} < 4.0 V,2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		5.3		1.3	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V), T_A = -40 to +85 °C.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03)

(4) Communication at different potential (2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		**Note 1**		**Note 1**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		**Note 3**		**Note 3**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4		1.2 Note 4	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. Operating condtions of LS (low-speed main) mode is T_A = -40 to +85 °C.

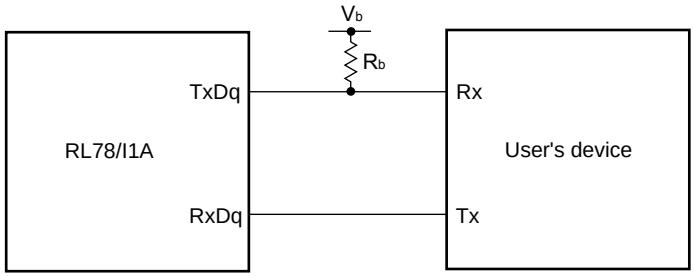
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]: Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

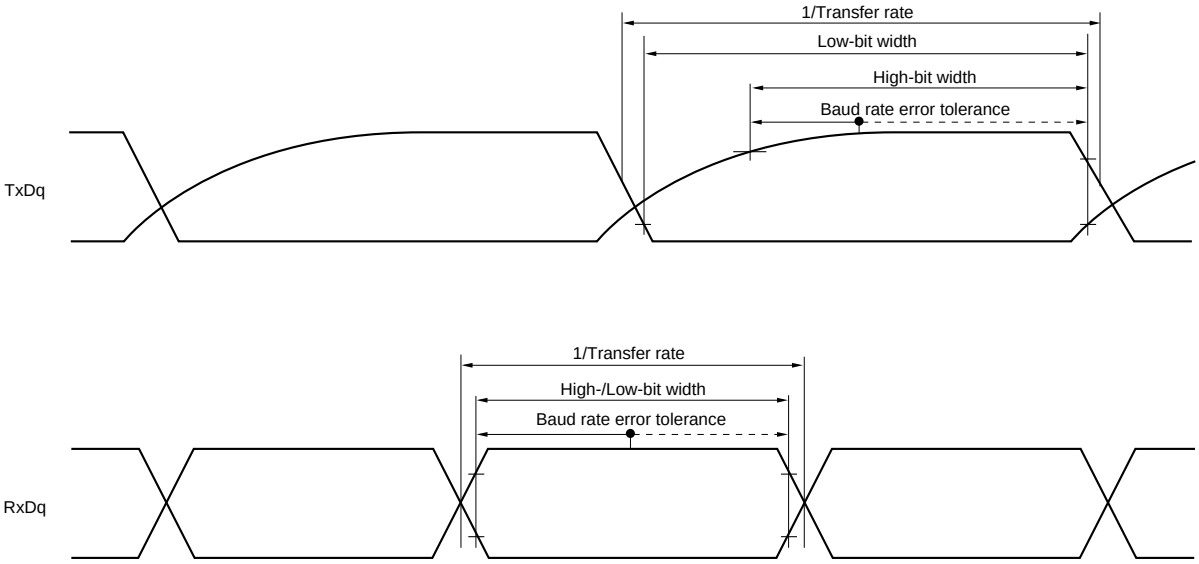
2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03))

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]: Communication line (TxDq) pull-up resistance, V_b[V]: Communication line voltage

2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

(5) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	200		1150		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	300		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 50		t_{KCY1}/2 – 75		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 120		t_{KCY1}/2 – 170		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 7		t_{KCY1}/2 – 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 10		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		81		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		177		479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		10		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		10		19		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			60		100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			130		195	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		44		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		44		110		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		10		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		10		19		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			10		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			10		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. Operating condtions of LS (low-speed main) mode is T_A = -40 to +85 °C.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

(6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

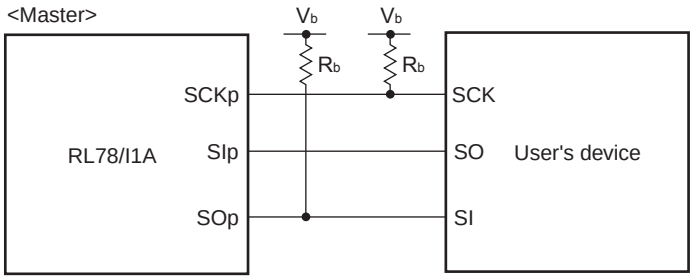
(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 75		t_{KCY1}/2 – 75		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 12		t_{KCY1}/2 – 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		81		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		177		479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			100		100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			195		195	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		44		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		44		110		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		19		19		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ			25		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ			25		25	ns

Notes
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. Operating condtions of LS (low-speed main) mode is T_A = -40 to +85 °C.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

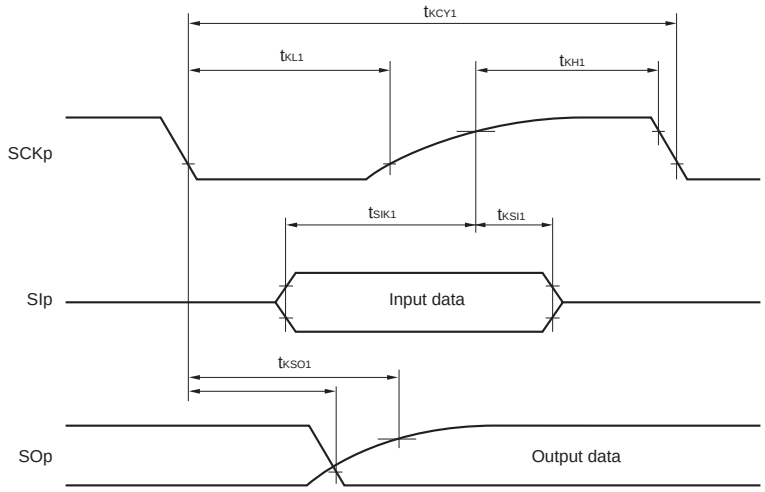
CSI mode connection diagram (during communication at different potential)



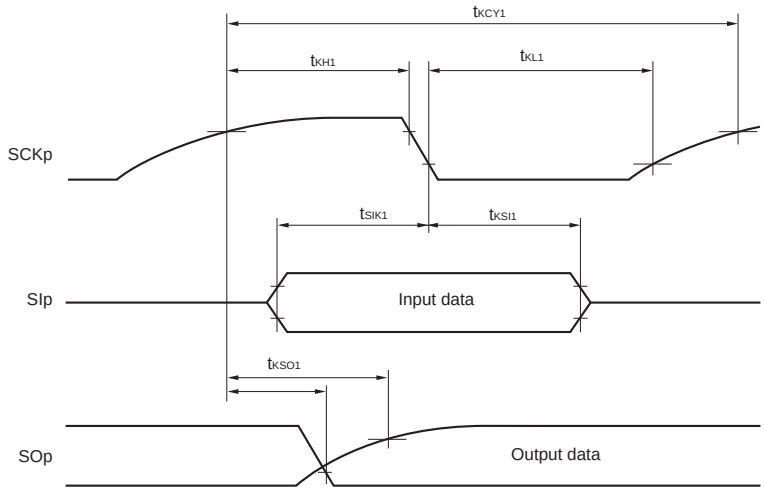
Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

(7) DALI/UART4 mode

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate				f_{MCK}/12		f_{MCK}/12	bps
		Maximum transfer rate theoretical value HS: f_{CLK} = 32 MHz, f_{MCK} = f_{CLK} LS: f_{CLK} = 8 MHz, f_{MCK} = f_{CLK}		2.6		0.6	Mbps

Note Operating condtions of LS (low-speed main) mode is T_A = -40 to +85 °C.

Remark f_{MCK}: Operation clock frequency of DALI/UART.
(Operation clock to be set by the serial clock select register mn (SPS4).)

32.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	0	100	0	100	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		4.7		μs
Hold time[Note 1]	$t_{HD:STA}$		4.0		4.0		μs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		4.7		μs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		4.0		μs
Data setup time (reception)	$t_{SU:DAT}$		250		250		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	3.45	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		4.0		μs
Bus-free time	t_{BUF}		4.7		4.7		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

3. Operating condtions of LS (low-speed main) mode is T_A = -40 to +85 °C.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I^2C fast mode

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	fast mode: f_{CLK} ≥ 3.5 MHz	0	400	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$		0.6		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$		0.6		0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}		1.3		1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}		0.6		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		100		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	0.9	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$		0.6		0.6		μs
Bus-free time	t_{BUF}		1.3		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

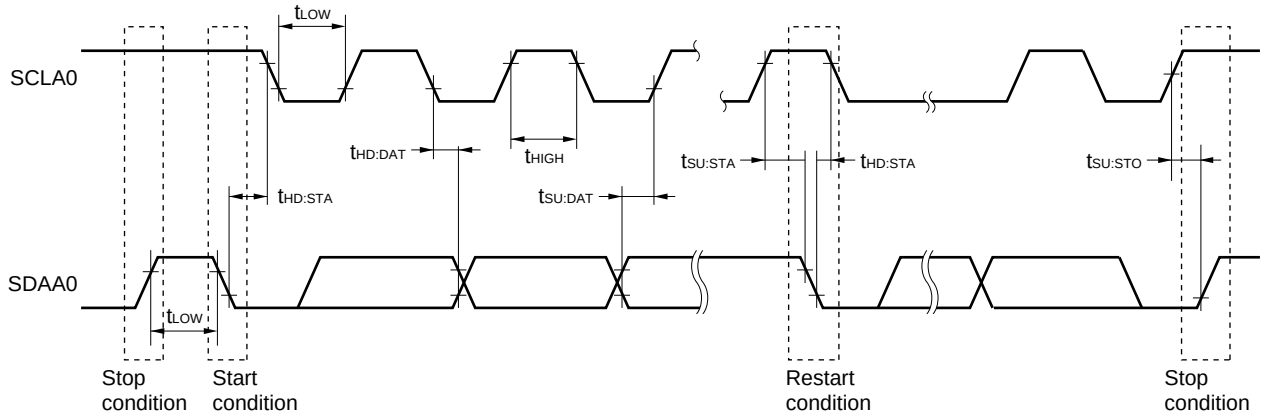
2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

3. Operating condtions of LS (low-speed main) mode is T_A = -40 to +85 °C.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



32.6 Analog Characteristics

32.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (–) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (–) = AV_{REFM}
ANI0 to ANI2, ANI4 to ANI7	Refer to **32.6.1 (1)**.	Refer to **32.6.1 (3)**.	Refer to **32.6.1 (3)**.
ANI16 to ANI19	Refer to **32.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **32.6.1 (1)**.		–

(1) When reference voltage (+)= AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI2, ANI4 to ANI7, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +105°C, 2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Note 3]			1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2, ANI4 to ANI7	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±2.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±1.5	LSB
Analog input voltage	V_{AIN}	ANI2, ANI4 to ANI7		0		AV_{REFP}	V
		Internal reference voltage (HS (high-speed main) mode)		V_{BGR} [Note 4]			V
		Temperature sensor output voltage (HS (high-speed main) mode)		V_{TMPS25} [Note 4]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

4. Refer to **32.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI16 to ANI19

(T_A = –40 to +105°C, 2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Notes 3]			1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin : ANI16 to ANI19	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD} [Notes 3]				±0.35	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution AV_{REFP} = V_{DD} [Notes 3]				±0.35	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD} [Notes 3]				±3.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD} [Notes 3]				±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI19		0		AV_{REFP} and V_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin : ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution			1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
Conversion time	t_{CONV}	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution				±0.60	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution				±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution				±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution				±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI2, ANI4 to ANI7		0		V_{DD}	V
		ANI16 to ANI19		0		V_{DD}	V
		Internal reference voltage (HS (high-speed main) mode)		V_{BGR}[Note 3]			V
		Temperature sensor output voltage (HS (high-speed main) mode)		V_{TMPS25}[Note 3]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **32.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0, ANI2, ANI4 to ANI7, ANI16 to ANI19

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} = 0 V Note 4, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8			bit
Conversion time	t_{CONV}	8-bit resolution	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution			±1.0	LSB
Analog input voltage	V_{AIN}		0		V_{BGR} Note 3	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **32.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS}, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV_{REFM}.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.

32.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGRT}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		−3.6		mV/C
Operation stabilization wait time	t_{AMP}		5			μs

32.6.3 Programmable gain amplifier

(T_A = –40 to +105°C, 2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOPGA}					±5	±10	mV
Input voltage range	V_{IPGA}				0		0.9V_{DD}/gain	V
Gain error Note 1		4, 8 times					±1	%
		16 times					±1.5	%
		32 times					±2	%
Slew rate Note 1	SR_{RPGA}	Rising edge	4.0 V ≤ V_{DD} ≤ 5.5 V	4, 8 times	4			V/μs
				16, 32 times	1.4			V/μs
			2.7 V ≤ V_{DD} < 4.0 V	4, 8 times	1.8			V/μs
				16, 32 times	0.5			V/μs
	SR_{FPGA}	Falling edge	4.0 V ≤ V_{DD} ≤ 5.5 V	4, 8 times	3.2			V/μs
				16, 32 times	1.4			V/μs
			2.7 V ≤ V_{DD} < 4.0 V	4, 8 times	1.2			V/μs
				16, 32 times	0.5			V/μs
Operation stabilization wait time Note 2	t_{PGA}	4, 8 times			5			μs
		16, 32 times			10			μs

Notes 1. When V_{IPGA} = 0.1V_{DD}/gain to 0.9V_{DD}/gain.

2. Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

Remark These characteristics apply when AV_{REFM} is selected as GND of the PGA by using the CVRVS1 bit.

32.6.4 Comparator

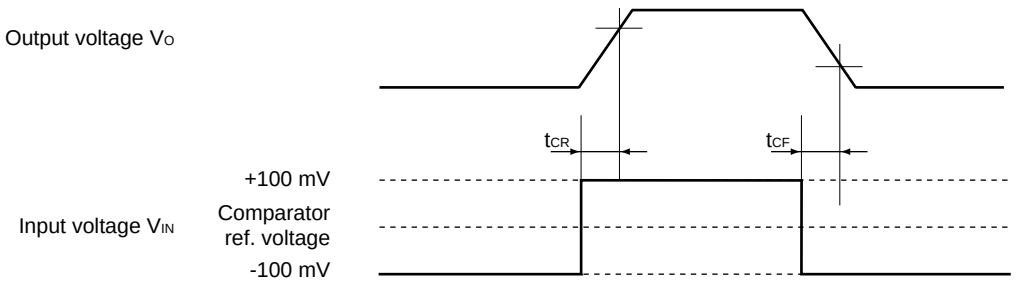
(T_A = −40 to +105°C, 2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOCMP}			±5	±40	mV
Input voltage range	V_{ICMP}	CMP0P to CMP5P	0		V_{DD}	V
		CMPCOM	0.045		0.9V_{DD}	V
Internal reference voltage deviation	ΔV_{IREF}	CmRVM register values: 7FH to 80H (m = 0 to 2)			±2	LSB
		Other than above			±1	LSB
Response time	t_{CR}, t_{CF}	Input amplitude = ±100 mV		70	150	ns
Operation stabilization wait time[Note 1]	t_{CMP}	3.3 V ≤ V_{DD} ≤ 5.5 V	1			μs
		2.7 V ≤ V_{DD} < 3.3 V	3			μs
Reference voltage stabilization wait time	t_{VR}	CVRE: 0 to 1 [Note 2]	10			μs

Notes 1. Time required until a state is entered where the DC and AC specifications of the comparator are satisfied after the operation of the comparator has been enabled (CMPnEN bit = 1: n = 0 to 5)

2. Enable comparator output (CnOE bit = 1; n = 0 to 5) after enabling operation of the internal reference voltage generator (by setting the CVREm bit to 1; m = 0 to 2) and waiting for the operation stabilization time to elapse.

Remark These characteristics apply when AV_{REFP} is selected as the power supply source of the internal reference voltage by using the CVRVS0 bit, and when AV_{REFM} is selected as GND of the internal reference voltage by using the CVRVS1 bit.

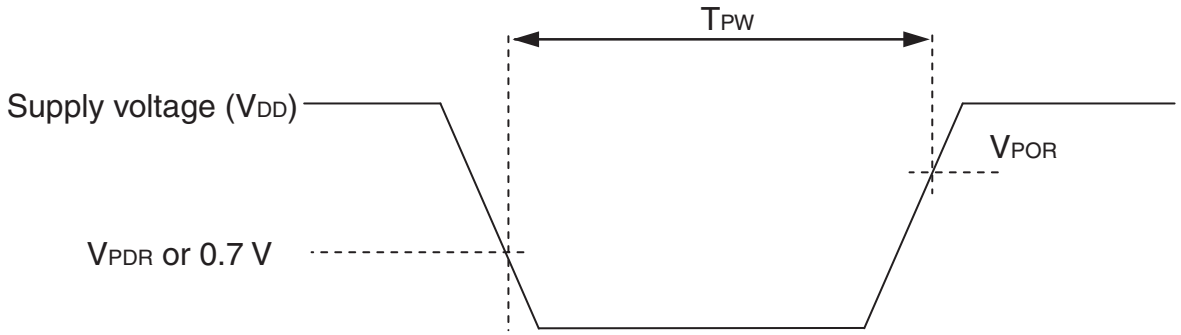


32.6.5 POR circuit characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



32.6.6 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interruput Mode

(T_A = –40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.97	4.06	4.14	V
			Power supply fall time	3.89	3.98	4.06	V
		V_{LVD1}	Power supply rise time	3.67	3.75	3.82	V
			Power supply fall time	3.59	3.67	3.74	V
		V_{LVD2}	Power supply rise time	3.06	3.13	3.19	V
			Power supply fall time	2.99	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.95	3.02	3.08	V
			Power supply fall time	2.89	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.85	2.92	2.97	V
			Power supply fall time	2.79	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.75	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage: 2.7 V			2.70	2.75	2.81	V
	V_{LVDD1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.85	2.92	2.97	V
				Falling interrupt voltage	2.79	2.86	2.91	V
	V_{LVDD2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.95	3.02	3.08	V
				Falling interrupt voltage	2.89	2.96	3.02	V
	V_{LVDD3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.97	4.06	4.14	V
				Falling interrupt voltage	3.89	3.98	4.06	V

32.6.7 Supply voltage rise inclination characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage rise	SV_{DD}				54	V/ms

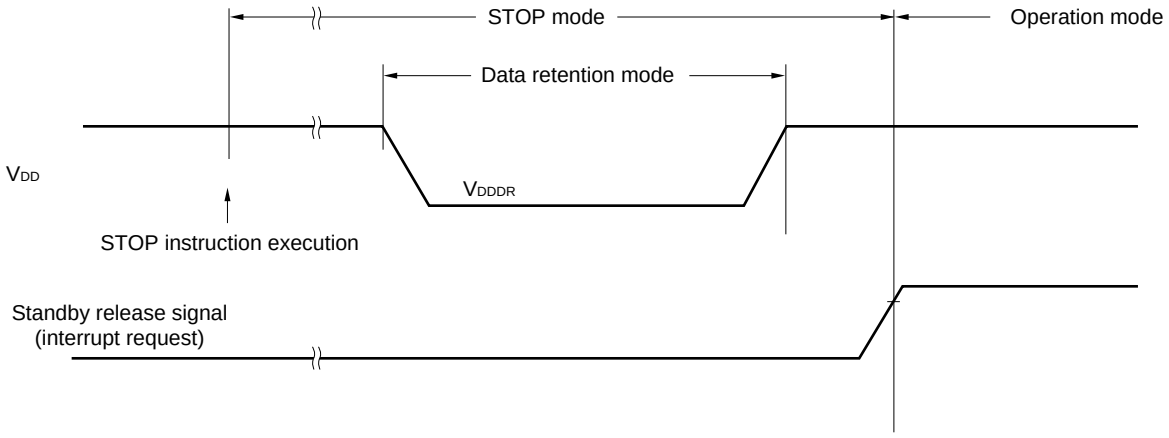
Caution Keep the internal reset status by using the LVD circuit or an external reset signal until V_{DD} rises to within the operating voltage range shown in 32.4 AC Characteristics.

32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



32.8 Flash Memory Programming Characteristics

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		32	MHz
Number of code flash rewrites[Notes 1, 2, 3]	C_{erwr}	Retained for 20 years	T_A = 85°C[Note 3]	1,000			Times
Number of data flash rewrites[Notes 1, 2, 3]		Retained for 1 year	T_A = 25°C[Note 3]		1,000,000		
		Retained for 5 years	T_A = 85°C[Note 3]	100,000			
		Retained for 20 years	T_A = 85°C[Note 3]	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

32.9 Dedicated Flash Memory Programmer Communication (UART)

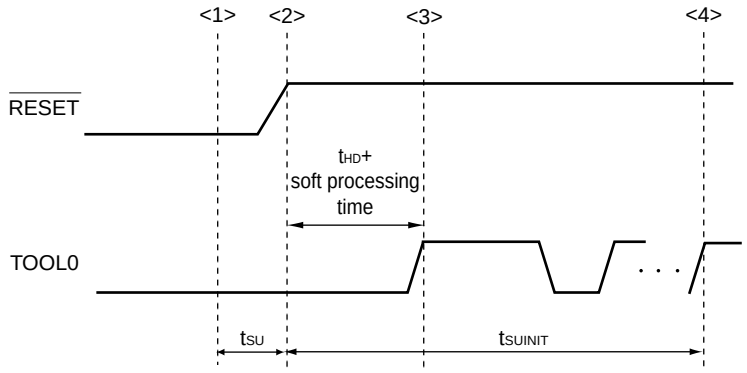
(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115.2 k		1 M	bps

32.10 Timing Specs for Switching Flash Memory Programming Modes

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the pin reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)

To our valued customers:	RL78/I1A Technical Update Exhibit Chapter 33 ELECTRICAL SPECIFICATIONS (T_A = −40 to +125°C)	M C Y G - A B - 1 3 - 0 0 4 4 - 1
		Aug 6, 2013
		Isao Murakami Manager 1st Solution Business Unit General Purpose Solution Business Division Brand Strategy Department 2nd Renesas Electronics Corporation

(Rep. Takao Iwasaki)

Thank you for your continued support for Renesas Electronics products.

Please be advised that the misstatements found in the following User's Manual have been fixed.

The second and following pages in this document include "Chapter 33 ELECTRICAL SPECIFICATIONS (T_A = −40 to +125°C)" which has been updated by the Correction for incorrect description notice RL78/I1A Descriptions in the User's Manual: Hardware Rev.1.00 changed (TN-RL*-A008A/E).

1. Applicable products:

RL78/I1A

R5F1076CMSP, R5F107ACMSP,R5F107AEMSP,R5F107DEMSP

2. Reference documents:

Correction for incorrect description notice RL78/I1A Descriptions in the User's Manual: Hardware Rev.1.00 changed (TN-RL*-A008A/E)

RL78/I1A User's Manual: Hardware Rev.1.00 (R01UH0169EJ01.00)

CHAPTER 33 ELECTRICAL SPECIFICATIONS (T_A = –40 to +125°C)

Target products: T_A = –40 to +125°C

R5F1076CMSP#V0, R5F1076CMSP#X0, R5F107ACMSP#V0,R5F107ACMSP#X0,
R5F107AEMSP#V0, R5F107AEMSP#X0, R5F107DEMSP#V0, R5F107DEMSP#X0

Cautions 1. The RL78/I1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 With functions for each product.

3. When any of these products are used at 105°C or lower, refer to CHAPTER 32 ELECTRICAL SPECIFICATIONS (T_A = –40 to +105°C).

33.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	−0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19	−0.3 to V_{DD} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	−40	mA
		Total of all pins −170 mA	P02, P03, P40, P120	−70	mA
			P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206	−100	mA
	I_{OH2}	Per pin	P20 to P22, P24 to P27	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	40	mA
		Total of all pins 170 mA	P02, P03, P40, P120	70	mA
			P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206	100	mA
	I_{OL2}	Per pin	P20 to P22, P24 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +125	°C
		In flash memory programming mode		−40 to +105	
Storage temperature	T_{stg}			−65 to +150	°C

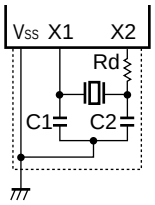
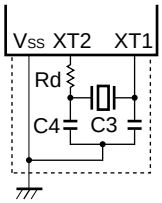
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

33.2 Oscillator Characteristics

33.2.1 X1, XT1 oscillator characteristics

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Recommended Circuit	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock frequency (f_X)Note	Ceramic resonator/ crystal resonator			1.0		20.0	MHz
XT1 clock frequency (f_{XT})Note	Crystal resonator			32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to 5.4 System Clock Oscillator.

33.2.2 On-chip oscillator characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Note 1]	f_{IH}		1		32	MHz
High-speed on-chip oscillator clock frequency accuracy[Note 2]		T_A = –20 to 85°C	–1		+1	%
		T_A = –40 to 105°C	–1.5		+1.5	%
		T_A = –40 to 125°C When 16 MHz selected	–2		+2	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			–15		+15	%

Notes 1. Frequency can be selected in a high-speed on-chip oscillator. Selected by bits 0 to 3 of option byte (000C2H/010C2H).

2. This indicates the oscillator characteristics only. See AC Characteristics for instruction execution time.

Remark When using the device at an ambient temperature that exceeds T_A = 105°C, the selectable oscillation frequency is 16 MHz max.X.

33.2.3 PLL characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PLL input clock frequency[Note]	f_{PLLIN}	High-speed system clock is selected (f_{MX} = 4 MHz)	3.92	4.00	4.08	MHz
		High-speed on-chip oscillator clock is selected (f_{IH} = 4 MHz)	3.92	4.00	4.08	MHz
PLL output clock frequency[Note]	f_{PLL}		f_{PLLIN} × 16			MHz

Note This only indicates the oscillator characteristics. See AC Characteristics for instruction execution time.

Remark When using the device at an ambient temperature that exceeds T_A = 105°C, only 16 MHz (f_{PLL} x 1/4) can be selected as the CPU operating frequency.

33.3 DC Characteristics

33.3.1 Pin characteristics

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	4.0 V ≤ V_{DD} ≤ 5.5 V			−3.0[Note 2]	mA
			2.7 V ≤ V_{DD} < 4.0 V			−1.0	mA
		Total of P02, P03, P40, P120 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			−9.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−3.0	mA
		Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			−21.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−6.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			−21.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−9.0	mA
	I_{OH2}	Per pin for P20 to P22, P24 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V			−0.1[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.7 V ≤ V_{DD} ≤ 5.5 V			−0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = −10.0 mA

Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P02, P10 to P12 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5[Note 2]	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.5[Note 2]	mA
		Total of P02, P03, P40, P120 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			5.0	mA
		Total of P05, P06, P10 to P12, P30, P31, P75 to P77, P147, P200 to P206 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
	I_{OL2}	Per pin for P20 to P22, P24 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V			0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.7 V ≤ V_{DD} ≤ 5.5 V			1.6	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = −10.0 mA

Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, $\overline{\text{RESET}}$	Normal input buffer	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P03, P10, P11	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.1		V_{DD}	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 2.7 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
Input voltage, low	V_{IL1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120 to P124, P137, P147, P200 to P206, EXCLK, EXCLKS, $\overline{\text{RESET}}$	Normal input buffer	0		0.2V_{DD}	V
	V_{IL2}	P03, P10, P11	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 2.7 V ≤ V_{DD} < 3.3 V	0		0.32	V

Caution The maximum value of V_{IH} of pins P02, P10 to P12 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD} – 0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –1.0 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P22, P24 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
	V_{OL2}	P20 to P22, P24 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V

Caution P02, P10 to P12 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P137, P147, P200 to P206, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P02, P03, P05, P06, P10 to P12, P20 to P22, P24 to P27, P30, P31, P40, P75 to P77, P120, P137, P147, P200 to P206, $\overline{\text{RESET}}$	$V_I = V_{SS}$				−1	μA
	I_{LIL2}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{SS}$	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
On-chip pll-up resistance	R_U	P02, P03, P05, P06, P10 to P12, P30, P31, P40, P75 to P77, P120, P147, P200 to P206	$V_I = V_{SS}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

33.3.2 Supply current characteristics

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (high-speed main) mode[Note 5]	f_{IH} = 16 MHz[Note 3]	V_{DD} = 5.0 V		2.9	4.8	mA
					V_{DD} = 3.0 V		2.9	4.8	mA
			HS (high-speed main) mode[Note 5]	f_{MX} = 20 MHz[Note 2], V_{DD} = 5.0 V	Square wave input		3.2	5.6	mA
					Resonator connection		3.3	5.7	mA
				f_{MX} = 20 MHz[Note 2], V_{DD} = 3.0 V	Square wave input		3.2	5.6	mA
					Resonator connection		3.3	5.7	mA
				f_{MX} = 10 MHz[Note 2], V_{DD} = 5.0 V	Square wave input		2.0	3.3	mA
					Resonator connection		2.0	3.3	mA
				f_{MX} = 10 MHz[Note 2], V_{DD} = 3.0 V	Square wave input		2.0	3.3	mA
					Resonator connection		2.0	3.3	mA
			HS (high-speed main) mode[Note 5]	f_{IH} = 4 MHz[Note 3] f_{PLL} = 64 MHz, f_{CLK} = 16 MHz	V_{DD} = 5.0 V		3.3	6.5	mA
					V_{DD} = 3.0 V		3.3	6.5	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz[Note 4] T_A = −40°C	Square wave input		4.2	6.0	μA
					Resonator connection		4.4	6.2	μA
				f_{SUB} = 32.768 kHz[Note 4] T_A = +25°C	Square wave input		4.2	6.0	μA
					Resonator connection		4.4	6.2	μA
				f_{SUB} = 32.768 kHz[Note 4] T_A = +50°C	Square wave input		4.3	7.2	μA
					Resonator connection		4.5	7.4	μA
				f_{SUB} = 32.768 kHz[Note 4] T_A = +70°C	Square wave input		4.4	8.1	μA
					Resonator connection		4.6	8.3	μA
				f_{SUB} = 32.768 kHz[Note 4] T_A = +85°C	Square wave input		5.2	11.4	μA
					Resonator connection		5.4	11.6	μA
				f_{SUB} = 32.768 kHz[Note 4] T_A = +105°C	Square wave input		6.9	20.8	μA
					Resonator connection		7.1	21.0	μA
				f_{SUB} = 32.768 kHz[Note 4] T_A = +125°C	Square wave input		11.1	51.2	μA
					Resonator connection		11.3	51.4	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 20 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.50	2.0	mA
					V_{DD} = 3.0 V		0.50	2.0	mA
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.40	2.2	mA
					Resonator connection		0.50	2.3	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.40	2.2	mA
					Resonator connection		0.50	2.3	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.24	1.22	mA
					Resonator connection		0.30	1.28	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.24	1.22	mA
					Resonator connection		0.30	1.28	mA
			HS (high-speed main) mode Note 7	f_{IH} = 4 MHz Note 4 f_{PLL} = 64 MHz, f_{CLK} = 16 MHz	V_{DD} = 5.0 V		0.95	3.7	mA
					V_{DD} = 3.0 V		0.95	3.7	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = −40°C	Square wave input		0.28	0.70	μA
					Resonator connection		0.47	0.89	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.33	0.70	μA
					Resonator connection		0.52	0.89	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.41	1.90	μA
					Resonator connection		0.60	2.09	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.54	2.80	μA
					Resonator connection		0.73	2.99	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		1.27	6.10	μA
					Resonator connection		1.46	6.29	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +105°C	Square wave input		3.04	15.5	μA
					Resonator connection		3.23	15.7	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +125°C	Square wave input		7.20	45.2	μA
					Resonator connection		7.53	45.5	μA
	I_{DD3} Note 6	STOP mode Note 8	T_A = −40°C				0.18	0.50	μA
			T_A = +25°C				0.23	0.50	μA
			T_A = +50°C				0.27	1.70	μA
			T_A = +70°C				0.44	2.60	μA
			T_A = +85°C				1.17	5.90	μA
			T_A = +105°C				2.94	15.3	μA
			T_A = +125°C				7.14	45.1	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 20 MHz

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVI} Notes 1, 7				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 8				2.5	12.2	mA
Programmable gain amplifier operating current	I_{PGA} Note 9		AV_{REFP} = V_{DD} = 5.0 V		0.21	0.37	mA
			AV_{REFP} = V_{DD} = 3.0 V		0.18	0.35	mA
Comparator operating current	I_{CMP} Note 10	When one comparator channel is operating	AV_{REFP} = V_{DD} = 5.0 V		41.4	74	μA
			AV_{REFP} = V_{DD} = 3.0 V		37.2	71	μA
	I_{VREF}	When one internal reference voltage circuit is operating	AV_{REFP} = V_{DD} = 5.0 V		14.8	31	μA
			AV_{REFP} = V_{DD} = 3.0 V		8.9	24	μA
Programmable gain amplifier/ comparator reference current source	I_{IREF} Note 11		AV_{REFP} = V_{DD} = 5.0 V		3.2	6.1	μA
			AV_{REFP} = V_{DD} = 3.0 V		2.9	5.9	μA
BGO operating current	I_{BGO} Note 12				2.50	12.2	mA
SNOOZE operating current	I_{SNOZ} Note 1	A/D converter operation	The mode is performed Note 13		0.50	1.10	mA
			The A/D conversion operations are performed, Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.20	2.17	mA
		CSI/UART operation			0.70	1.27	mA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Current flowing to the V_{DD}.

2. When the high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip ocsillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock is operating in operating mode or in HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the XT1 oscillator and f_{IL} operating current). The current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{WDT}, when $f_{CLK} = f_{SUB}$ when the watchdog timer is operating.

6. Current flowing only to the A/D converter. The supply current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC}, when the A/D converter is operating in operating mode or in HALT mode.

7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

8. Current flowing during self-programming operation.

9. Current flowing only to the programmable gain amplifier. The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{PGA}, when the programmable gain amplifier is operating in operating mode or in HALT mode.

10. Current flowing only to the comparator. The supply current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3}, and I_{CMP}, when the comparator is operating.

11. This is the current required to flow to V_{DD} pin of the current circuit that is used as the programmable gain amplifier and the comparator.

12. Current flowing only during data flash rewrite.

13. Refer to **21.3.3 SNOOZE mode** for shift time to the SNOOZE mode.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

5. Example of calculating current value when using programmable gain amplifier and comparator.

Examples 1) TYP. operating current value when three comparator channels, one internal reference voltage generator, and PGA are operating (when $AV_{REFP} = V_{DD}$ = 5.0 V)

$I_{CMP} \times 3 + I_{VREF} + I_{PGA} + I_{IREF}$
= 41.4 [μA] × 3 + 14.8 [μA] × 1 + 210 [μA] + 3.2 [μA]
= 352.2 [μ A]

Examples 2) TYP. operating current value when using two comparator channels, without using internal reference voltage generator (when $AV_{REFP} = V_{DD}$ = 5.0 V)

$I_{CMP} \times 2 + I_{IREF}$
= 41.4 [μA] × 2 + 3.2 [μA]
= 86.0 [μA]

33.4 AC Characteristics

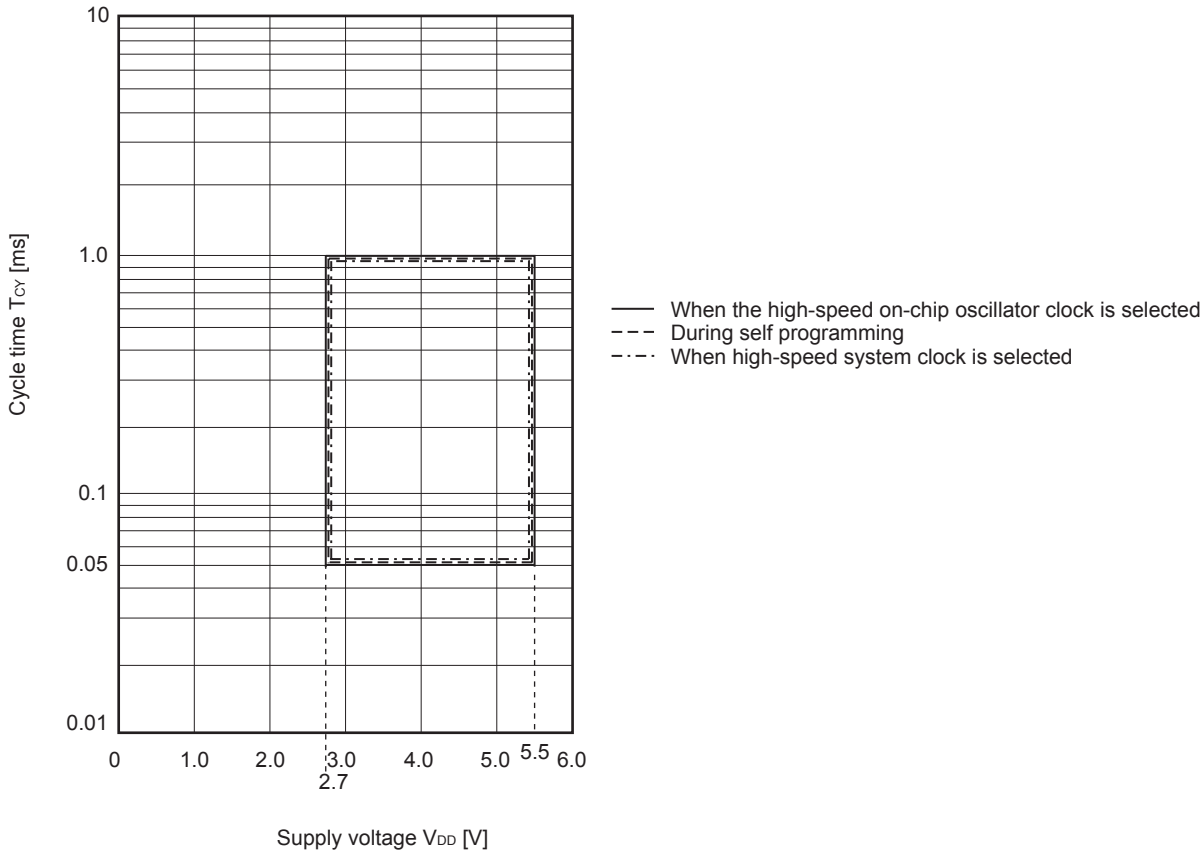
(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode		0.05		1	μs
		Subsystem clock (f_{SUB}) operation			28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	T_A = −40 to +105°C	0.05		1	μs
External system clock frequency	f_{EX}				1.0		20.0	MHz
	f_{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}				24			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI03, TI05, TI06, TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				2/f_{MCK}+10			ns
TO03, TO05, TO06, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TKCO00 to TKCO05 output frequency (When duty = 50%)	f_{TO}	HS (high-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			5	MHz
				2.7 V ≤ V_{DD} < 4.0 V			4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP3, INTP4, INTP9 to INTP11, INTP20 to INTP23		2.7 V ≤ V_{DD} ≤ 5.5 V	1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

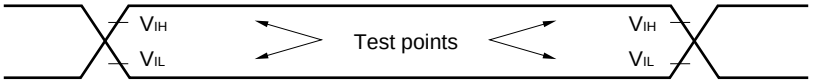
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation

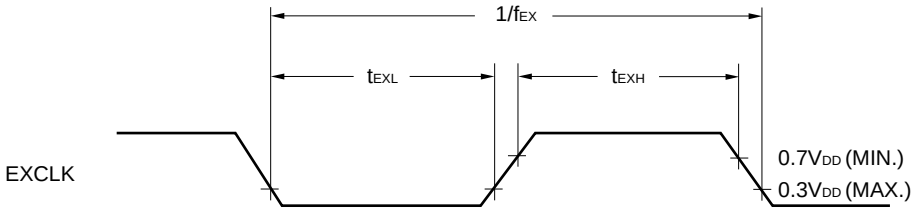
T_{CY} vs V_{DD} (HS (high-speed main) mode)



AC Timing Test Points

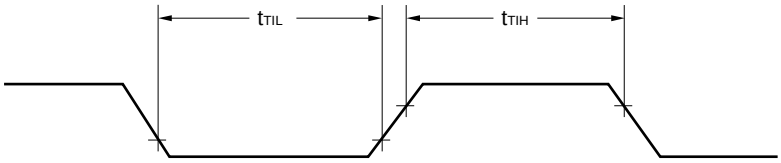


External System Clock Timing

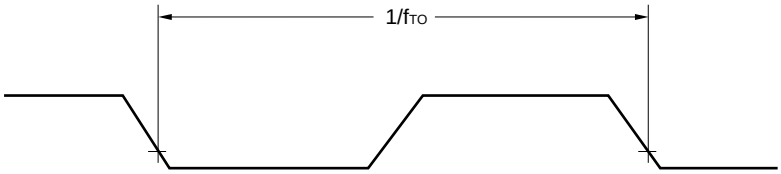


TI/TO Timing

TI03, TI05, TI06, TI07

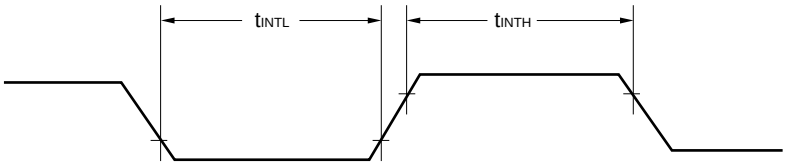


TO03, TO05, TO06, TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TKCO00 to TKCO05



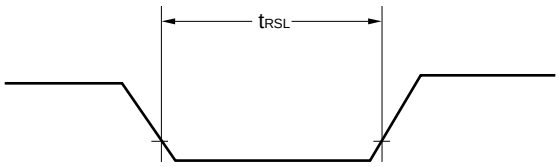
Interrupt Request Input Timing

INTP0, INTP3, INTP4, INTP9 to INTP11, INTP20 to INTP23



$\overline{\text{RESET}}$ Input Timing

$\overline{\text{RESET}}$



33.5 Peripheral Functions Characteristics

33.5.1 Serial array unit 0, 4 (UART0, UART1, CSI00, DALI/UART4)

(1) During communication at same potential (UART mode)

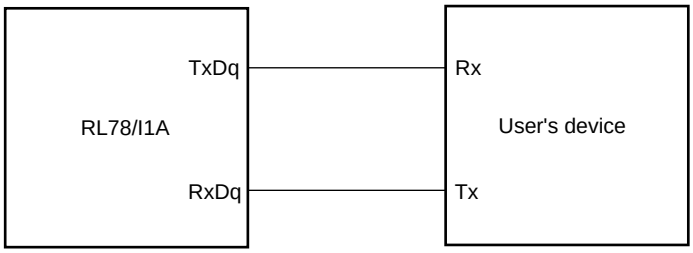
(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1				f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 2		3.3	Mbps

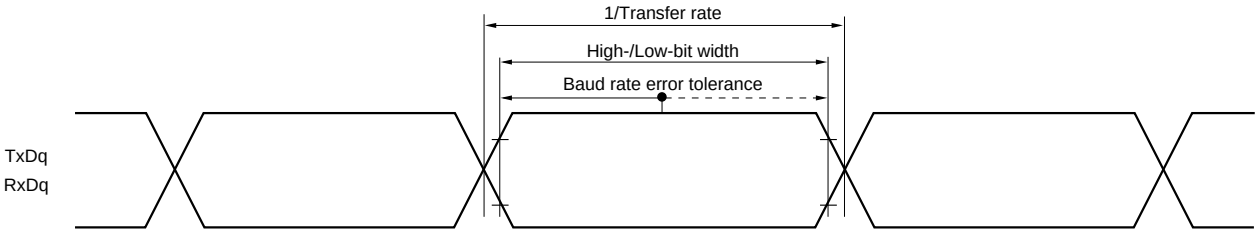
Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 20 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V	250		ns
			2.7 V ≤ V_{DD} ≤ 5.5 V	500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 20$		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 40$		ns
SIp setup time (to SCKp↑)[Note 1]	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		80		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		80		ns
SIp hold time (from SCKp↑)[Note 2]	t_{KSI1}			40		ns
Delay time from $\overline{SCKp}$↓ to SOp output[Note 3]	t_{KSO1}	C = 30 pF[Note 4]			80	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time[Note 5]	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} ≤ 20 MHz	6/f_{MCK}		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	16 MHz < f_{MCK}	8/f_{MCK}		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2		ns
SIp setup time (to SCKp↑)[Note 1]	t_{SIK2}			1/f_{MCK}+40		ns
SIp hold time (from SCKp↑)[Note 2]	t_{KSI2}			1/f_{MCK}+60		ns
Delay time from SCKp↓ to SOp output[Note 3]	t_{KSO2}	C = 30 pF[Note 4]			2/f_{MCK}+80	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

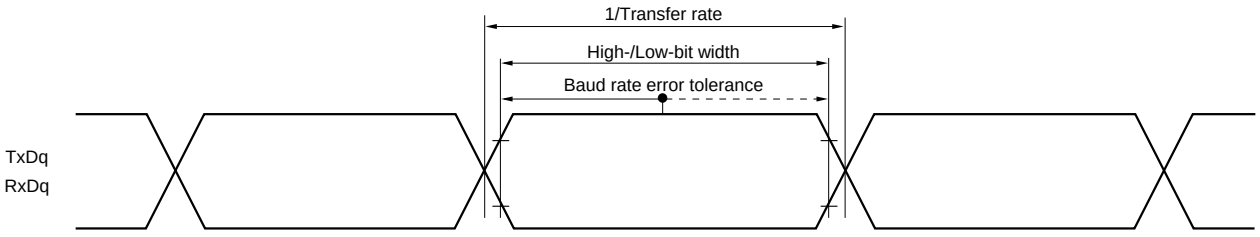
4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

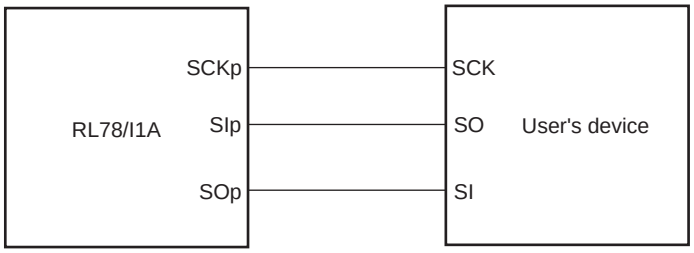
Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

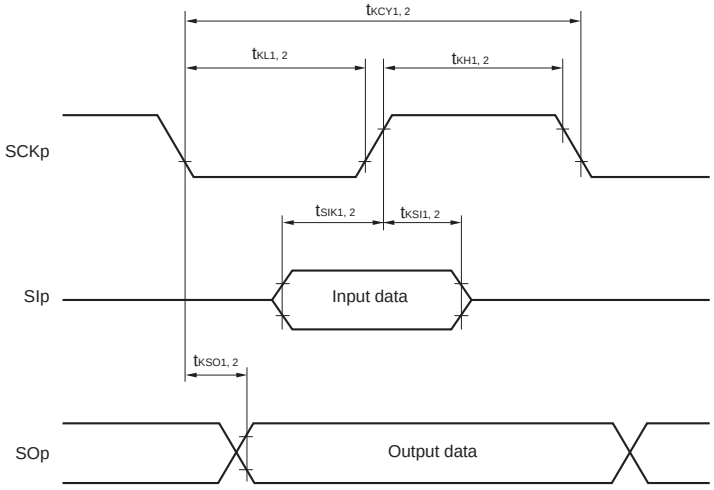
2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))



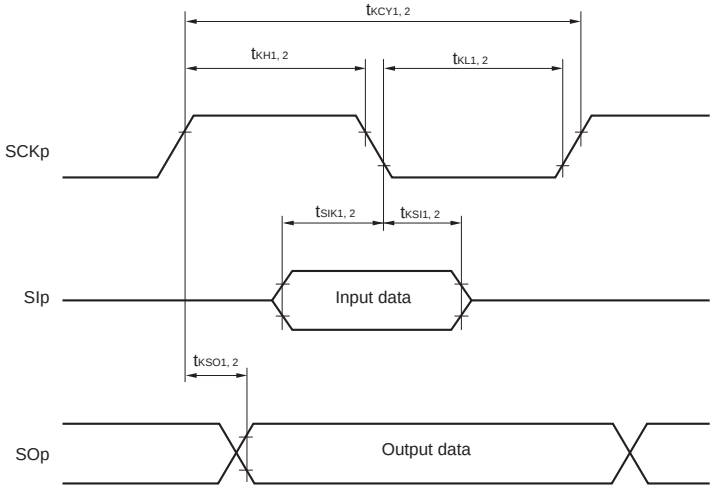
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00)

2. m: Unit number, n: Channel number (mn = 00)

(4) Communication at different potential (2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		Unit
					MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			$f_{MCK}/6$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 2		3.3	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			$f_{MCK}/6$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 2		3.3	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 20 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03)

(4) Communication at different potential (2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		Unit
					MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			**Note 1**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8[Note 2]	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			**Note 3**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2[Note 4]	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

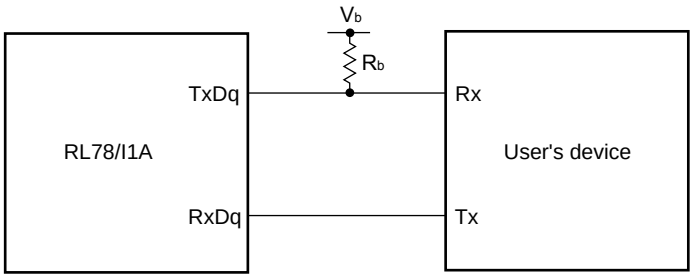
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]: Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

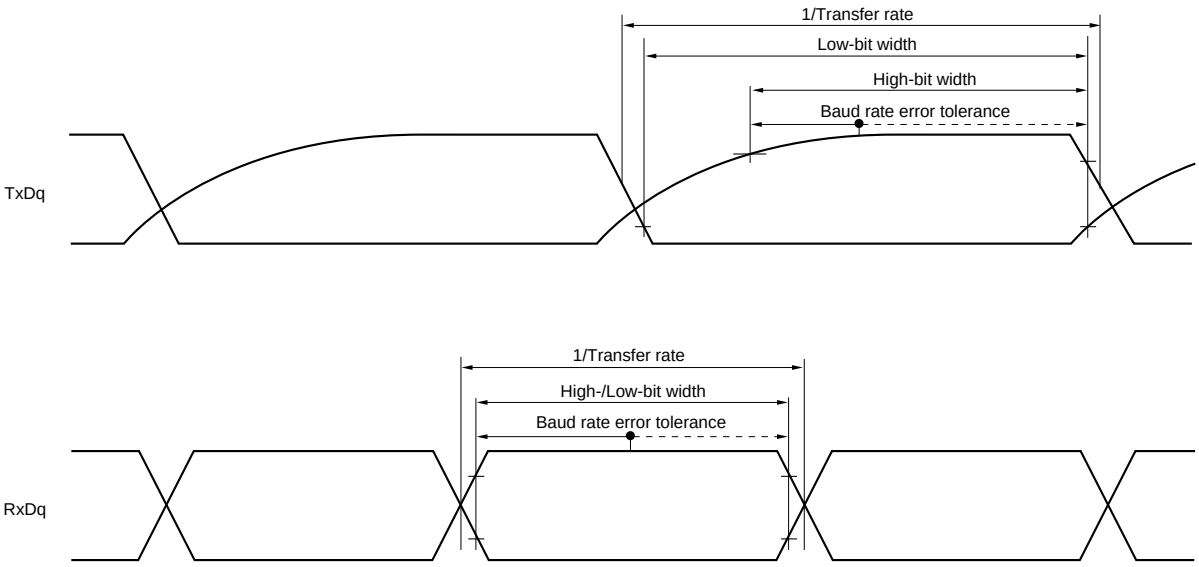
2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03))

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]: Communication line (TxDq) pull-up resistance, V_b[V]: Communication line voltage

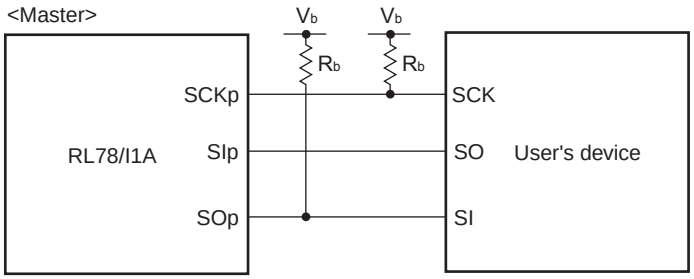
2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 1)

(5) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	600		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	1000		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 80		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 170		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 28		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 40		ns
SIp setup time (to SCKp↑)[Note 1]	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		160		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		250		ns
SIp hold time (from SCKp↑)[Note 1]	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		40		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		40		ns
Delay time from SCKp↓ to SOp output[Note 1]	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			160	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			250	ns
SIp setup time (to SCKp↓)[Note 2]	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		80		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		80		ns
SIp hold time (from SCKp↓)[Note 2]	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		40		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		40		ns
Delay time from SCKp↑ to SOp output[Note 2]	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			80	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			80	ns

(**Note**, **Caution** and **Remark** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

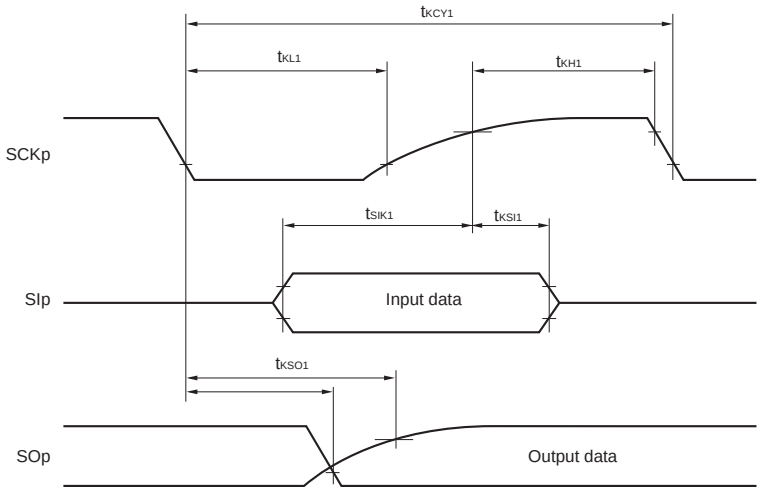
2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

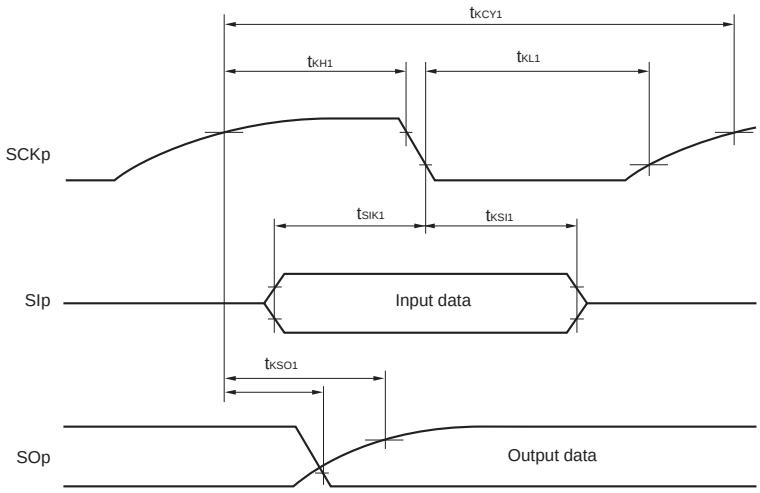
Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

(6) DALI/UART4 mode

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate				f_{MCK}/12	bps
		Maximum transfer rate theoretical value f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}		1.6	Mbps

Remark f_{MCK}: Operation clock frequency of DALI/UART.
(Operation clock to be set by the serial clock select register 4 (SPS4).)

33.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	0	100	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		μs
Hold time[Note 1]	$t_{HD:STA}$		4.0		μs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		μs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		μs
Data setup time (reception)	$t_{SU:DAT}$		250		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		μs
Bus-free time	t_{BUF}		4.7		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I^2C fast mode

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	fast mode: f_{CLK} ≥ 3.5 MHz	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$		0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}		1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$		0.6		μs
Bus-free time	t_{BUF}		1.3		μs

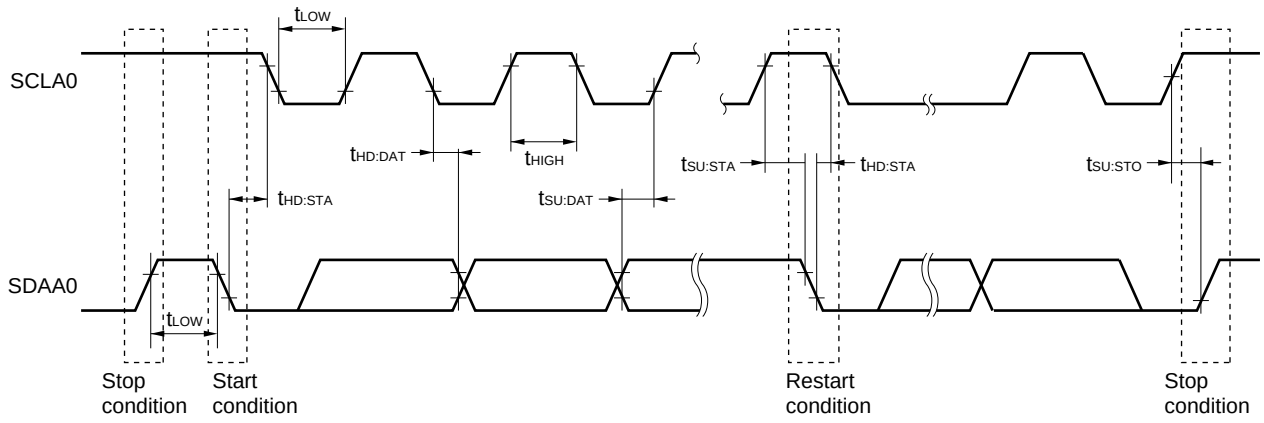
Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



33.6 Analog Characteristics

33.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (–) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (–) = AV_{REFM}
ANI0 to ANI2, ANI4 to ANI7	Refer to **33.6.1 (1)**.	Refer to **33.6.1 (3)**.	Refer to **33.6.1 (3)**.
ANI16 to ANI19	Refer to **33.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **33.6.1 (1)**.		–

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin: ANI2, ANI4 to ANI7, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +125°C, 2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Note 3]			1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2, ANI4 to ANI7	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.8		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±0.25	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±2.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]				±1.5	LSB
Analog input voltage	V_{AIN}	ANI2, ANI4 to ANI7		0		AV_{REFP}	V
		Internal reference voltage (HS (high-speed main) mode)		V_{BGR} [Note 4]			V
		Temperature sensor output voltage (HS (high-speed main) mode)		V_{TMPS25} [Note 4]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

4. Refer to **33.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI16 to ANI19

(T_A = –40 to +125°C, 2.7 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}[Note 3]			1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin : ANI16 to ANI19	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} < 5.5 V	3.4		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD}[Note 3]				±0.35	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution AV_{REFP} = V_{DD}[Note 3]				±0.35	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD}[Note 3]				±3.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD}[Note 3]				±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI19		0		AV_{REFP} and V_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error: Add ±0.2%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution			1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI2, ANI4 to ANI7, ANI16 to ANI19	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		39	μs
Conversion time	t_{CONV}	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.8		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution				±0.60	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution				±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution				±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution				±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI2, ANI4 to ANI7		0		V_{DD}	V
		ANI16 to ANI19		0		V_{DD}	V
		Internal reference voltage (HS (high-speed main) mode)		V_{BGR} [Note 3]			V
		Temperature sensor output voltage (HS (high-speed main) mode)		V_{TMPS25} [Note 3]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **33.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI0, ANI2, ANI4 to ANI7, ANI16 to ANI19

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} Note 4 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		bit
Conversion time	t_{CONV}	8-bit resolution	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution			±1.0	LSB
Analog input voltage	V_{AIN}		0		V_{BGR} Note 3	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **33.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS}, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV_{REFM}.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.

33.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +125°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/C
Operation stabilization wait time	t_{AMP}		5			μs

33.6.3 Programmable gain amplifier

(T_A = −40 to +125°C, 2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOPGA}					±5	±10	mV
Input voltage range	V_{IPGA}				0		0.9V_{DD}/gain	V
Gain error[Note 1]		4, 8 times					±1	%
		16 times					±1.5	%
		32 times					±2	%
Slew rate[Note 1]	SR_{RPGA}	Rising edge	4.0 V ≤ V_{DD} ≤ 5.5 V	4, 8 times	4			V/μs
				16, 32 times	1.4			V/μs
			2.7 V ≤ V_{DD} < 4.0 V	4, 8 times	1.8			V/μs
				16, 32 times	0.5			V/μs
	SR_{FPGA}	Falling edge	4.0 V ≤ V_{DD} ≤ 5.5 V	4, 8 times	3.2			V/μs
				16, 32 times	1.4			V/μs
			2.7 V ≤ V_{DD} < 4.0 V	4, 8 times	1.2			V/μs
				16, 32 times	0.5			V/μs
Operation stabilization wait time[Note 2]	t_{PGA}	4, 8 times			5			μs
		16, 32 times			10			μs

Notes 1. When V_{IPGA} = 0.1V_{DD}/gain to 0.9V_{DD}/gain.

2. Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

Remark These characteristics apply when AV_{REFM} is selected as GND of the PGA by using the CVRVS1 bit.

33.6.4 Comparator

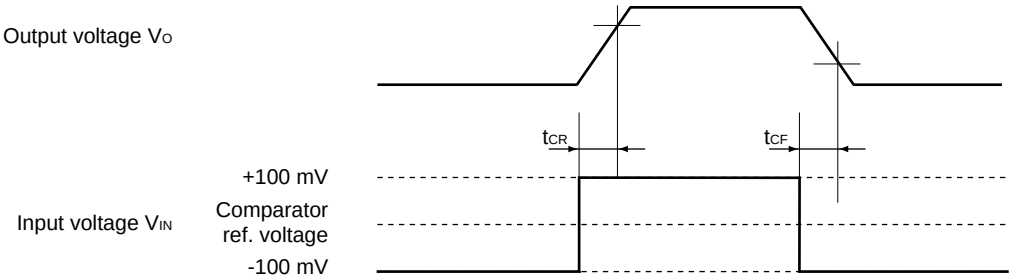
(T_A = −40 to +125°C, 2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOCMP}			±5	±40	mV
Input voltage range	V_{ICMP}	CMP0P to CMP5P	0		V_{DD}	V
		CMPCOM	0.045		0.9V_{DD}	V
Internal reference voltage deviation	ΔV_{IREF}	CmRVM register values: 7FH to 80H (m = 0 to 2)			±2	LSB
		Other than above			±1	LSB
Response time	t_{CR}, t_{CF}	Input amplitude = ±100 mV		70	150	ns
Operation stabilization wait time[Note 1]	t_{CMP}	3.3 V ≤ V_{DD} ≤ 5.5 V	1			μs
		2.7 V ≤ V_{DD} < 3.3 V	3			μs
Reference voltage stabilization wait time	t_{VR}	CVRE: 0 to 1 [Note 2]	10			μs

Notes 1. Time required until a state is entered where the DC and AC specifications of the comparator are satisfied after the operation of the comparator has been enabled (CMPnEN bit = 1: n = 0 to 5)

2. Enable comparator output (CnOE bit = 1; n = 0 to 5) after enabling operation of the internal reference voltage generator (by setting the CVREm bit to 1; m = 0 to 2) and waiting for the operation stabilization time to elapse.

Remark These characteristics apply when AV_{REFP} is selected as the power supply source of the internal reference voltage by using the CVRVS0 bit, and when AV_{REFM} is selected as GND of the internal reference voltage by using the CVRVS1 bit.

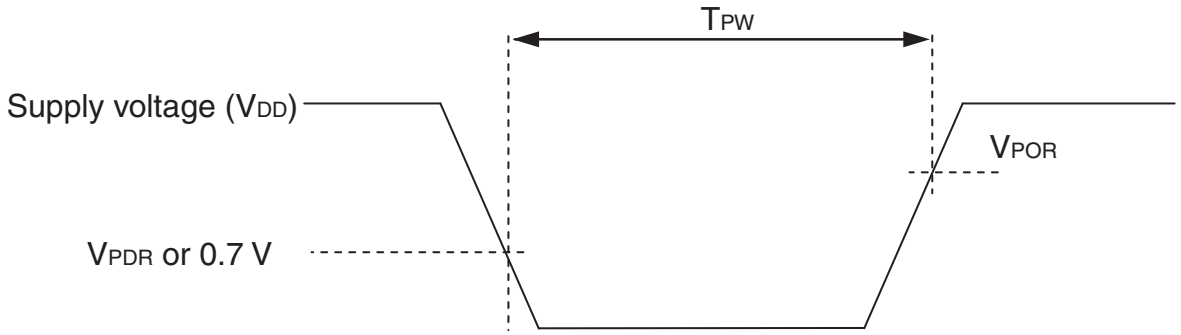


33.6.5 POR circuit characteristics

(T_A = –40 to +125°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.62	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.61	V
Minimum pulse width[Note]	T_{PW}		350			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



33.6.6 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interruput Mode

(T_A = –40 to +125°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.97	4.06	4.25	V
			Power supply fall time	3.89	3.98	4.15	V
		V_{LVD1}	Power supply rise time	3.67	3.75	3.93	V
			Power supply fall time	3.59	3.67	3.83	V
		V_{LVD2}	Power supply rise time	3.06	3.13	3.28	V
			Power supply fall time	2.99	3.06	3.20	V
		V_{LVD3}	Power supply rise time	2.95	3.02	3.17	V
			Power supply fall time	2.89	2.96	3.09	V
		V_{LVD4}	Power supply rise time	2.85	2.92	3.07	V
			Power supply fall time	2.79	2.86	2.99	V
		V_{LVD5}	Power supply rise time	2.75	2.81	2.95	V
			Power supply fall time	2.70	2.75	2.88	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +125°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage: 2.7 V			2.70	2.75	2.88	V
	V_{LVDD1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.85	2.92	3.07	V
				Falling interrupt voltage	2.79	2.86	2.99	V
	V_{LVDD2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.95	3.02	3.17	V
				Falling interrupt voltage	2.89	2.96	3.09	V
	V_{LVDD3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.97	4.06	4.25	V
				Falling interrupt voltage	3.89	3.98	4.15	V

33.6.7 Supply voltage rise inclination characteristics

(T_A = –40 to +125°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage rise	SV_{DD}				54	V/ms

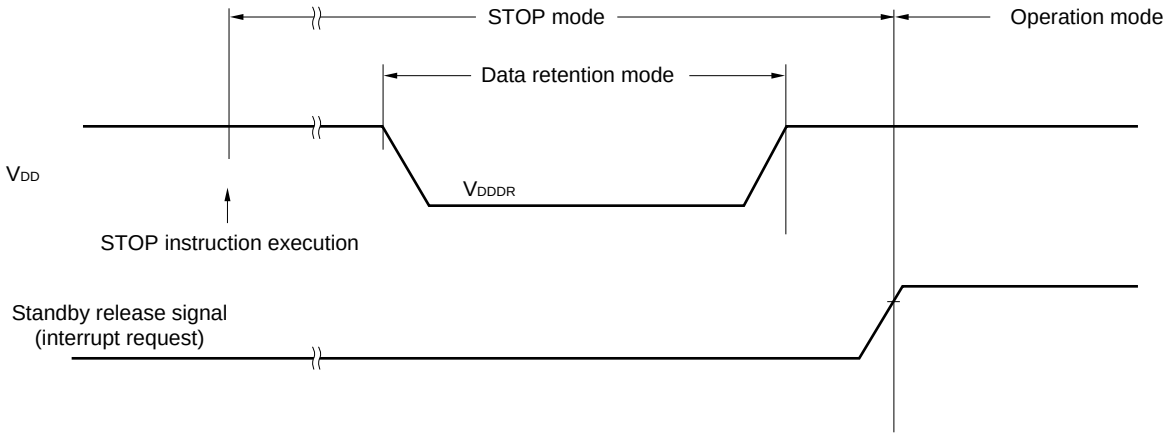
Caution Keep the internal reset status by using the LVD circuit or an external reset signal until V_{DD} rises to within the operating voltage range shown in 33.4 AC Characteristics.

33.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +125°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



33.8 Flash Memory Programming Characteristics

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		32	MHz
Number of code flash rewrites[Notes 1, 2, 3]	C_{erwr}	Retained for 20 years	T_A = 85°C[Note 3]	1,000			Times
Number of data flash rewrites[Notes 1, 2, 3]		Retained for 1 year	T_A = 25°C[Note 3]		1,000,000		
		Retained for 5 years	T_A = 85°C[Note 3]	100,000			
		Retained for 20 years	T_A = 85°C[Note 3]	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

33.9 Dedicated Flash Memory Programmer Communication (UART)

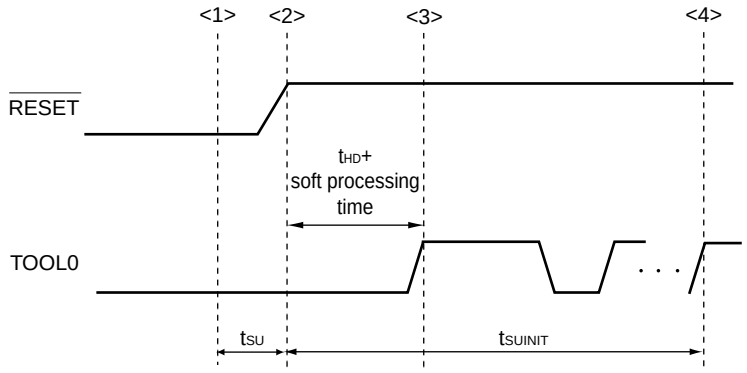
T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115.2 k		1 M	bps

33.10 Timing Specs for Switching Flash Memory Programming Modes

T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the pin reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)