Date: Apr. 24, 2015

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A024C/E	Rev.	3.00
Title	Correction for Incorrect Description Notice RL78/I1A Descriptions in the Hardware User's Manual Rev. 2.10 Changed		Information Category	Technical Notification		
Applicable Product	RL78/I1A Group R5F107xxx	Lot No. All lot	Reference Document	RL78/I1A User's Manual: Hardware Rev. 2.10 R01UH0169EJ0210 (Jul. 2013)		

This document describes misstatements found in the RL78/I1A hardware user's manual Rev. 2.10 (R01UH0169EJ0210).

List of corrections to be added in this notification

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1.3 Pin Configuration 1.3.1 20-pin products	p.4	Incorrect descriptions revised
1.3 Pin Configuration 1.3.2 30-pin products	p.5	Incorrect descriptions Revised
1.3 Pin Configuration 1.3.3 38-pin products	p.6	Incorrect descriptions Revised
Figure 13-1. Block Diagram of Operational Amplifier	p.516	Incorrect descriptions Revised
13.3.3 Programmable gain amplifier input channel select register (PGAINS)	p.519	Incorrect descriptions revised

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2	Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p)	p.380, 381	Incorrect descriptions revised
3	Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p)	p.382, 383	Incorrect descriptions revised
4	Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p)	p.384,385	Incorrect descriptions revised
5	Figure 14-1. Block Diagram of Comparator	p.527	Incorrect descriptions revised
6	Figure 14-12. Format of Peripheral Function Switch Register 0 (PFSEL0)	p.538	Incorrect descriptions revised
7	14. 5 Caution for Using Timer KB Simultaneous Operation Function	-	Caution added
8	Timing Chart of SNOOZE Mode Operation	p.666, 667, 669	Incorrect descriptions revised
9	Table 20-1. Interrupt Source List (2/3)	p.898	Caution added
10	Figure 20-1. Basic Configuration of Interrupt Function	p.900	Incorrect descriptions revised
11	Table 21-1. Operating Statuses in HALT Mode (2/2)	p.931	Incorrect descriptions revised
12	Table 21-2. Operating Statuses in STOP Mode	p.936	Incorrect descriptions revised
13	Table 21-3. Operating Statuses in SNOOZE Mode	p.942	Incorrect descriptions revised
14	32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	p.1100	Explanations added

15	33.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics	p.1142	Explanations added
16	CHAPTER 34 PACKAGE DRAWINGS 34.3 38-pin Products	p.1147	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the hardware user's manual.

Corrections in the hardware user's manual

Item	Applicable Item			Applicable Page in this notice
		Document No.	English	R01UH0169EJ0210
1	Figure 7-19. Format of Peripheral Function Switch Register 0 (PFSEL0)			p.303	p.4
2	Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p)			p.380, 381	p.6
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10	Figure 20-1. Basic Configuration of Interrupt Function			p.900	p.29
11	Table 21-1. Operating Statuses in HALT Mode (2/2)			p.931	p.31
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20	Figure 13-1. Block Diagram of Operational Amplifier			p.516	p.44
21	13.3.3 Programmable gain amplifier input channel select register (PGAINS)			p.519	p.45

Incorrect: **Bold with underline**; Correct: Gray hatched

Issued Document History

RL78/I1A Incorrect description notice, issued document history

Document Number	Issue Date	Description
TN-RL*-A024A/E	Apr. 9, 2014	First edition issued
TN-RL*-A024B/E	Nov. 21, 2014	Second edition issued Incorrect descriptions : No.16 added
TN-RL*-A024C/E	Apr. 24, 2015	Third edition issued Incorrect descriptions : No.17 to No.21 added (this document)

1. Figure 7-19. Format of Peripheral Function Switch Register 0 (PFSEL0)

Incorrect descriptions of the TMRSTEN1 and TMRSTEN0 bits of Peripheral Function Switch Register 0 (PFSEL0) are revised, and Note is added.

Incorrect:

Figure 7-19. Format of Peripheral Function Switch Register 0 (PFSEL0)

Address: F05C6H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0

CMP2STEN	CMP0STEN	Comparator interrupt selection
See **CHAPTER 14 COMPARATOR**.		

PNFEN	Use/Do not use external interrupt INTP20 noise filter
0	Use noise filter
1	Do not use noise filter

ADTRG11	ADTRG10	Timer trigger selection for A/D conversion
0	0	Timer KB0 trigger source
0	1	Timer KB1 trigger source
1	0	Timer KB2 trigger source
1	1	Setting prohibited

TMRSTEN1	**Function selection for external interrupt INTP21**
0	**External interrupt function (external interrupt generation enabled,** timer restart disabled)
1	**Timer restart function (external interrupt generation disabled, standby release disabled)**

TMRSTEN0	**Function selection for external interrupt INTP20**
0	**External interrupt function (external interrupt generation enabled,** timer restart disabled)
1	**Timer restart function (external interrupt generation disabled, standby release disabled)**

Remark See **Figure 14-1 Block Diagram of Comparator**.

Correct:

Figure 7-19. Format of Peripheral Function Switch Register 0 (PFSEL0)

Address: F05C6H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0

CMP2STEN	CMP0STEN	Comparator interrupt selection
See **CHAPTER 14 COMPARATOR**.		

PNFEN	Use/Do not use external interrupt INTP20 noise filter
0	Use noise filter
1	Do not use noise filter

ADTRG11	ADTRG10	Timer trigger selection for A/D conversion
0	0	Timer KB0 trigger source
0	1	Timer KB1 trigger source
1	0	Timer KB2 trigger source
1	1	Setting prohibited

TMRSTEN1	Switch of external interrupt INTP21 **Note**
0	External interrupt function is selected (stop mode release enabled, timer restart disabled).
1	Timer restart function is selected (stop mode release disabled, timer restart enabled).

TMRSTEN0	Switch of external interrupt INTP20 **Note**
0	External interrupt function is selected (stop mode release enabled, timer restart disabled).
1	Timer restart function/forced output stop function 2 is selected (stop mode release disabled, timer restart enabled).

Note When INTP20 or INTP21 is used as a trigger of the timer KB forced output stop function 2 or timer restart function, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

Remark See **Figure 14-1 Block Diagram of Comparator**.

2. Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p)

Incorrect descriptions of forced output stop function control register 0p (TKBPACTL0p) are revised, and Note is added.

Incorrect:

Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (1/2)

Address: F0630H (TKBPACTL00), F0632H (TKBPACTL01) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL0p	TKBPAFXS0p3	TKBPAFXS0p2	TKBPAFXS0p1	TKBPAFXS0p0	0	0	0	TKBPAFCM0p

7	6	5	4	3	2	1	0
0	TKBPAHZS0p2	TKBPAHZS0p1	TKBPAHZS0p0	TKBPAHCM0p1	TKBPAHCM0p0	TKBPAMD0p1	TKBPAMD0p0

TKBPAFXS0p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	**INTP20 can be used as a trigger.**

TKBPAFXS0p2	Comparator trigger selection for forced output stop function 2
0	Comparator 2 can not be used as a trigger.
1	**Comparator 2 can be used as a trigger.**

TKBPAFXS0p1	Comparator trigger selection for forced output stop function 2
0	Comparator 1 can not be used as a trigger.
1	**Comparator 1 can be used as a trigger.**

TKBPAFXS0p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAFCM0p	Operation mode selection for forced output stop function 2
0	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period.**
1	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.**

Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (2/2)

TKBPAHZS0p2	Comparator trigger selection for forced output stop function 1
0	Comparator 2 can not be used as a trigger.
1	**Comparator 2 can be used as a trigger.**

TKBPAHZS0p1	Comparator trigger selection for forced output stop function 1
0	Comparator 1 can not be used as a trigger.
1	**Comparator 1 can be used as a trigger.**

TKBPAHZS0p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAHCM0p1	TKBPAHCM0p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT0)** = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT0)** = 1" is invalid. Forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT0)** = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT0)** = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT0)** = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT0)** = 1 is written when the trigger signal is in its inactive period.

TKBPAMD0p1	TKBPAMD0p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Cautions 1. During timer operation, setting the other bits of the TKBPACTL0p register is prohibited. However, the TKBPACTL0p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

Correct:

Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (1/2)

Address: F0630H (TKBPACTL00), F0632H (TKBPACTL01) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL0p	TKBPAFXS0p3	TKBPAFXS0p2	TKBPAFXS0p1	TKBPAFXS0p0	0	0	0	TKBPAFCM0p
	7	6	5	4	3	2	1	0
	0	TKBPAHZS0p2	TKBPAHZS0p1	TKBPAHZS0p0	TKBPAHCM0p1	TKBPAHCM0p0	TKBPAMD0p1	TKBPAMD0p0

TKBPAFXS0p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	INTP20 can be used as a trigger. **Note 1**

TKBPAFXS0p2	Comparator trigger selection for forced output stop function 2
0	Comparator 2 can not be used as a trigger.
1	Comparator 2 can be used as a trigger. **Note 2**

TKBPAFXS0p1	Comparator trigger selection for forced output stop function 2
0	Comparator 1 can not be used as a trigger.
1	Comparator 1 can be used as a trigger. **Note 3**

TKBPAFXS0p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. **Note 2**

TKBPAFCM0p	Operation mode selection for forced output stop function 2
0	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period. **Note 4**
1	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger. **Note 4**

TKBPAHZS0p2	Comparator trigger selection for forced output stop function 1
0	Comparator 2 can not be used as a trigger.
1	Comparator 2 can be used as a trigger. **Note 2**

TKBPAHZS0p1	Comparator trigger selection for forced output stop function 1
0	Comparator 1 can not be used as a trigger.
1	Comparator 1 can be used as a trigger. **Note 3**

TKBPAHZS0p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. **Note 2**

Figure 7-73. Format of Forced Output Stop Function Control Register 0p (TKBPACTL0p) (2/2)

TKBPAHCM0p1	TKBPAHCM0p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT0p) = 1" is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level. Note 4
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT0p) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written when the trigger signal is in its inactive period. Note 4

TKBPAMD0p1	TKBPAMD0p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Notes 1. When INTP20 is used as the forced output stop function 2, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

2. When CMP0 or CMP2 is used as the timer KB forced output stop function, set CMPnSTEN = 1. See **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

3. When CMP1 is used as the timer KB forced output stop function, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

4. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).

Cautions 1. During timer operation, setting the other bits of the TKBPACTL0p register is prohibited. However, the TKBPACTL0p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

3. Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p)

Incorrect descriptions of forced output stop function control register 1p (TKBPACTL1p) are revised, and Note is added.

Incorrect:

Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) (1/2)

Address: F0670H (TKBPACTL10), F0672H (TKBPACTL11) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL1p	TKBPAFXS1p3	TKBPAFXS1p2	TKBPAFXS1p1	TKBPAFXS1p0	0	0	0	TKBPAFCM1p

7	6	5	4	3	2	1	0
0	TKBPAHZS1p2	TKBPAHZS1p1	TKBPAHZS1p0	TKBPAHCM1p1	TKBPAHCM1p0	TKBPAMD1p1	TKBPAMD1p0

TKBPAFXS1p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	**INTP20 can be used as a trigger.**

TKBPAFXS1p2	Comparator trigger selection for forced output stop function 2
0	Comparator 3 can not be used as a trigger.
1	**Comparator 3 can be used as a trigger.**

TKBPAFXS1p1	Comparator trigger selection for forced output stop function 2
0	Comparator 2 can not be used as a trigger.
1	**Comparator 2 can be used as a trigger.**

TKBPAFXS1p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAFCM1p	Operation mode selection for forced output stop function 2
0	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period.**
1	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.**

Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) (2/2)

TKBPAHZS1p2	Comparator trigger selection for forced output stop function 1
0	Comparator 3 can not be used as a trigger.
1	**Comparator 3 can be used as a trigger.**

TKBPAHZS1p1	Comparator trigger selection for forced output stop function 1
0	Comparator 2 can not be used as a trigger.
1	**Comparator 2 can be used as a trigger.**

TKBPAHZS1p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAHCM1p1	TKBPAHCM1p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT1)** = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT1)** = 1" is invalid. Forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT1)** = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT1)** = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT1)** = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT1)** = 1 is written when the trigger signal is in its inactive period.

TKBPAMD1p1	TKBPAMD1p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Cautions 1. During timer operation, setting the other bits of the TKBPACTL1p register is prohibited. However, the TKBPACTL1p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

Correct:

Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) (1/2)

Address: F0670H (TKBPACTL10), F0672H (TKBPACTL11) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL1p	TKBPAFXS1p3	TKBPAFXS1p2	TKBPAFXS1p1	TKBPAFXS1p0	0	0	0	TKBPAFCM1p
	7	6	5	4	3	2	1	0
	0	TKBPAHZS1p2	TKBPAHZS1p1	TKBPAHZS1p0	TKBPAHCM1p1	TKBPAHCM1p0	TKBPAMD1p1	TKBPAMD1p0

TKBPAFXS1p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	INTP20 can be used as a trigger. Note 1

TKBPAFXS1p2	Comparator trigger selection for forced output stop function 2
0	Comparator 3 can not be used as a trigger.
1	Comparator 3 can be used as a trigger. Note 2

TKBPAFXS1p1	Comparator trigger selection for forced output stop function 2
0	Comparator 2 can not be used as a trigger.
1	Comparator 2 can be used as a trigger. Note 3

TKBPAFXS1p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. Note 3

TKBPAFCM1p	Operation mode selection for forced output stop function 2
0	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period. Note 4
1	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger. Note 4

TKBPAHZS1p2	Comparator trigger selection for forced output stop function 1
0	Comparator 3 can not be used as a trigger.
1	Comparator 3 can be used as a trigger. Note 2

TKBPAHZS1p1	Comparator trigger selection for forced output stop function 1
0	Comparator 2 can not be used as a trigger.
1	Comparator 2 can be used as a trigger. Note 3

TKBPAHZS1p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. Note 3

Figure 7-74. Format of Forced Output Stop Function Control Register 1p (TKBPACTL1p) (2/2)

TKBPAHCM1p1	TKBPAHCM1p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT1p) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT1p) = 1" is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT1p) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT1p) = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT1p) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT1p) = 1 is written when the trigger signal is in its inactive period.

TKBPAMD1p1	TKBPAMD1p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Notes 1. When INTP20 is used as the forced output stop function 2, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

2. When CMP3 is used as the timer KB forced output stop function, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

3. When CMP0 or CMP2 is used as the timer KB forced output stop function, set CMPnSTEN = 1. For details, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

4. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).

Cautions 1. During timer operation, setting the other bits of the TKBPACTL1p register is prohibited. However, the TKBPACTL1p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

4. Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p)

Incorrect descriptions of forced output stop function control register 2p (TKBPACTL2p) are revised, and Note is added.

Incorrect:

Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) (1/2)

Address: F06B0H (TKBPACTL20) , F06B2H (TKBPACTL21) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL2p	TKBPAFXS2p3	TKBPAFXS2p2	TKBPAFXS2p1	TKBPAFXS2p0	0	0	0	TKBPAFCM2p

7	6	5	4	3	2	1	0
0	TKBPAHZS2p2	TKBPAHZS2p1	TKBPAHZS2p0	TKBPAHCM2p1	TKBPAHCM2p0	TKBPAMD2p1	TKBPAMD2p0

TKBPAFXS2p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	**INTP20 can be used as a trigger.**

TKBPAFXS2p2	Comparator trigger selection for forced output stop function 2
0	Comparator 5 can not be used as a trigger.
1	**Comparator 5 can be used as a trigger.**

TKBPAFXS2p1	Comparator trigger selection for forced output stop function 2
0	Comparator 3 can not be used as a trigger.
1	**Comparator 3 can be used as a trigger.**

TKBPAFXS2p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAFCM2p	Operation mode selection for forced output stop function 2
0	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period.**
1	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger.**

Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) (2/2)

TKBPAHZS2p2	Comparator trigger selection for forced output stop function 1
0	Comparator 5 can not be used as a trigger.
1	**Comparator 5 can be used as a trigger.**

TKBPAHZS2p1	Comparator trigger selection for forced output stop function 1
0	Comparator 4 can not be used as a trigger.
1	**Comparator 4 can be used as a trigger.**

TKBPAHZS2p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

TKBPAHCM2p1	TKBPAHCM2p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT2)** = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT2)** = 1" is invalid. Forced output stop function 1 is cleared when **Hi-Z stop trigger (TKBPAHTT2)** = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT2)** = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "**Hi-Z stop trigger (TKBPAHTT2)** = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after **Hi-Z stop trigger (TKBPAHTT2)** = 1 is written when the trigger signal is in its inactive period.

TKBPAMD2p1	TKBPAMD2p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Cautions 1. During timer operation, setting the other bits of the TKBPACTL2p register is prohibited. However, the TKBPACTL2p register can be refreshed (the same value is written).

2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

Correct:

Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) (1/2)

Address: F06B0H (TKBPACTL20) , F06B2H (TKBPACTL21) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
TKBPACTL2p	TKBPAFXS2p3	TKBPAFXS2p2	TKBPAFXS2p1	TKBPAFXS2p0	0	0	0	TKBPAFCM2p
	7	6	5	4	3	2	1	0
	0	TKBPAHZS2p2	TKBPAHZS2p1	TKBPAHZS2p0	TKBPAHCM2p1	TKBPAHCM2p0	TKBPAMD2p1	TKBPAMD2p0

TKBPAFXS2p3	External interruption trigger selection for forced output stop function 2
0	INTP20 can not be used as a trigger.
1	INTP20 can be used as a trigger. **Note 1**

TKBPAFXS2p2	Comparator trigger selection for forced output stop function 2
0	Comparator 5 can not be used as a trigger.
1	Comparator 5 can be used as a trigger. **Note 2**

TKBPAFXS2p1	Comparator trigger selection for forced output stop function 2
0	Comparator 3 can not be used as a trigger.
1	Comparator 3 can be used as a trigger. **Note 2**

TKBPAFXS2p0	Comparator trigger selection for forced output stop function 2
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. **Note 3**

TKBPAFCM2p	Operation mode selection for forced output stop function 2
0	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period. **Note 4**
1	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger. **Note 4**

TKBPAHZS2p2	Comparator trigger selection for forced output stop function 1
0	Comparator 5 can not be used as a trigger.
1	Comparator 5 can be used as a trigger. **Note 2**

TKBPAHZS2p1	Comparator trigger selection for forced output stop function 1
0	Comparator 4 can not be used as a trigger.
1	Comparator 4 can be used as a trigger. **Note 2**

TKBPAHZS2p0	Comparator trigger selection for forced output stop function 1
0	Comparator 0 can not be used as a trigger.
1	Comparator 0 can be used as a trigger. **Note 3**

Figure 7-75. Format of Forced Output Stop Function Control Register 2p (TKBPACTL2p) (2/2)

TKBPAHCM2p1	TKBPAHCM2p0	Clear condition selection for forced output stop function 1
0	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT2p) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT2p) = 1" is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT2p) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT2p) = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing "forced output stop function release trigger (TKBPAHTT2p) = 1" is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT2p) = 1 is written when the trigger signal is in its inactive period.

TKBPAMD2p1	TKBPAMD2p0	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	0	Output fixed at low level	Output fixed at low level
1	1	Output fixed at high level	Output fixed at high level

Notes 1. When INTP20 is used as the forced output stop function 2, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

2. When CMP4 or CMP5 is used as the timer KB forced output stop function, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

3. When CMP0 is used as the timer KB forced output stop function, set CMP0STEN = 1. For details, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

4. When timer KB is stopped (TKBCEn = 0) without waiting for the next counter period, the forced output stop function is kept on until timer KB is restarted (TKBCEn = 1).

Cautions 1. During timer operation, setting the other bits of the TKBPACTL2p register is prohibited. However, the TKBPACTL2p register can be refreshed (the same value is written).

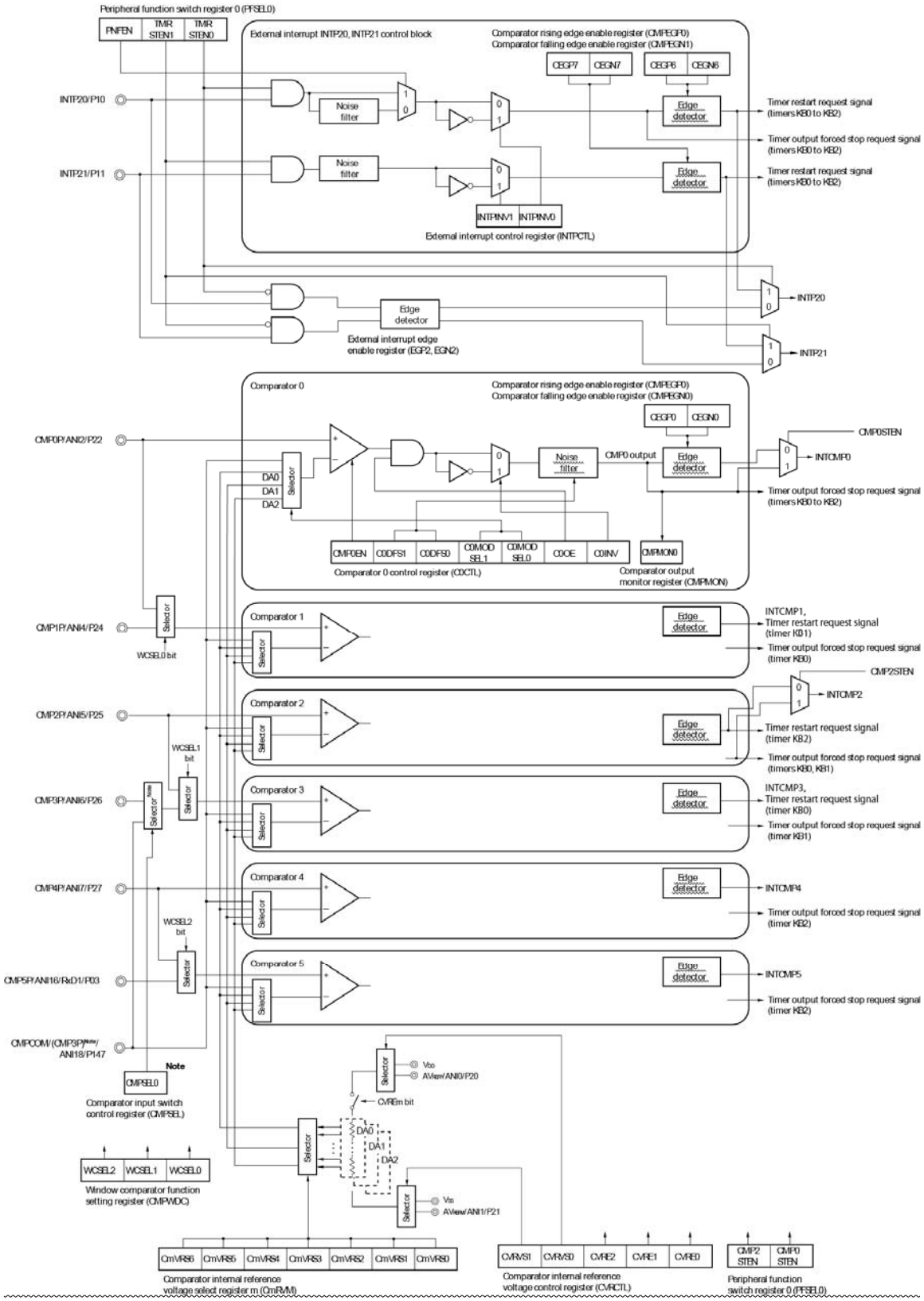
2. Be sure to clear bits 11 to 9 and 7 to "0".

Remark n = 0 to 2, p = 0, 1

5. Figure 14-1. Block Diagram of Comparator

Incorrect names of the noise filter and the edge detection circuit in the block diagram are revised, and Note is added.

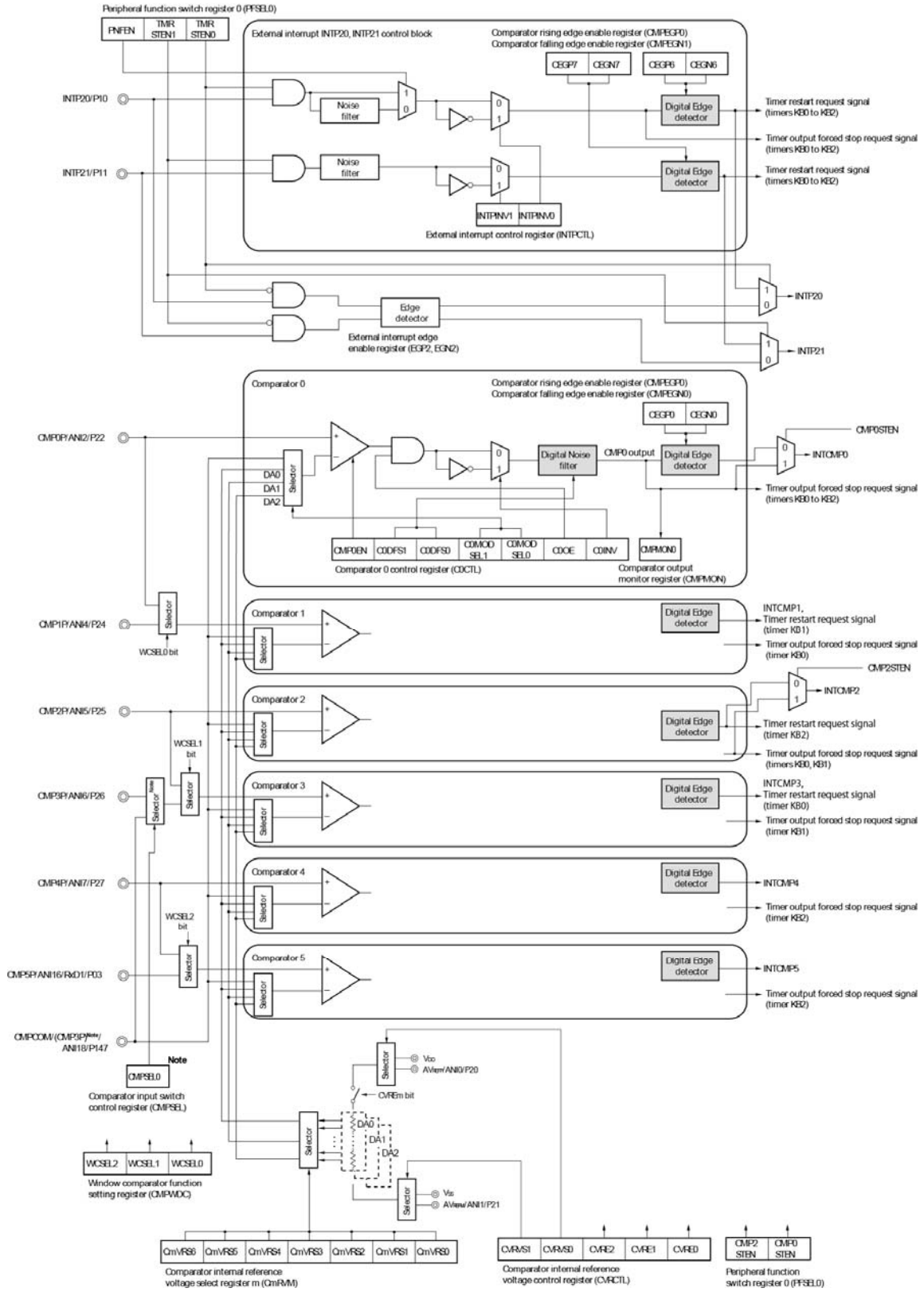
Incorrect:



Note 20-pin products only. ANI16/CMP3P/P26 is selected by default for 30- and 38-pin products.

Remark m = 0 to 2

Correct:



Note 20-pin products only. ANI16/CMP3P/P26 is selected by default for 30- and 38-pin products.

Caution When INTP20, INTP21, and comparator are used as the timer KB forced output stop function 2 or timer KB restart function, see 14. 5 Caution for Using Timer KB Simultaneous Operation Function.

Remark m = 0 to 2

6. Figure 14-12. Format of Peripheral Function Switch Register 0 (PFSEL0)

Incorrect descriptions of the comparator and external interrupts are revised, and Notes are added.

Incorrect:

Figure 14-12. Format of Peripheral Function Switch Register 0 (PFSEL0)

Address: F05C6H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0

CMP2STEN	Comparator 2 detection interrupt (INTCMP2) switching
0	STOP mode clear disabled
1	STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register)

CMP0STEN	Comparator 0 detection interrupt (INTCMP0) switching
0	STOP mode clear disabled
1	STOP mode clear enabled, but only when not using noise filter (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register)

PNFEN	Use/Do not use external interrupt INTP20 noise filter
0	Use noise filter
1	Do not use noise filter

TMRSTEN1	External interrupt INTP21 function select
0	External interrupt function (can be generated external interrupt, but cannot be used for timer restart function)
1	Timer restart function (cannot be generated external interrupt, and cannot release standby mode)

TMRSTEN0	External interrupt INTP20 function select
0	External interrupt function (can be generated external interrupt, but cannot be used for timer restart function)
1	Timer restart function (cannot be generated external interrupt, and cannot release standby mode)

Caution Comparator detection interrupt other than CMP0 and CMP2 cannot be used to clear the STOP mode.

Correct:

Figure 14-12. Format of Peripheral Function Switch Register 0 (PFSEL0)

Address: F05C6H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	3	2	<1>	<0>
PFSEL0	0	CMP2STEN	CMP0STEN	PNFEN	ADTRG11	ADTRG10	TMRSTEN1	TMRSTEN0

CMP2STEN	Comparator 2 detection interrupt (INTCMP2) switching Note 1
0	Signal via digital edge detect circuit is selected. STOP mode release is disabled.
1	Forced output stop request signal is selected. STOP mode release is enabled, but only when not using noise filter. (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register)

CMP0STEN	Comparator 0 detection interrupt (INTCMP0) switching Note 1
0	Signal via digital edge detect circuit is selected. STOP mode release is disabled.
1	Forced output stop request signal is selected. STOP mode release is enabled, but only when not using noise filter. (Can be set when operating in low-power RTC mode (RTCLPC = 1 in the OSMC register)

PNFEN	Use/Do not use external interrupt INTP20 noise filter
0	Use noise filter
1	Do not use noise filter

TMRSTEN1	External interrupt INTP21 function switching Note 2
0	External interrupt function is selected. (STOP mode release is enabled, but cannot be used for timer restart function)
1	Timer restart function is selected. (STOP mode release is disabled, but can be used for timer restart function)

TMRSTEN0	External interrupt INTP20 function switching Note 2
0	External interrupt function is selected. (STOP mode release is enabled, but cannot be used for timer restart function)
1	Timer restart function/forced output stop function 2 is selected. (STOP mode release is disabled, but can be used for timer restart function)

Notes 1. When the interrupt for CMP0 and CMP2 is used, adopt a function used with the interrupt input signal.

When the CMP0 and CMP2 are used as a trigger of the timer KB forced output stop function, set CMPnSTEN = 1.

When the CMP2 is used as a trigger of the timer restart function for timer KB, set CMP2STEN = 0.

For details, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

2. When INTP20 and INTP21 are used as a trigger of the timer KB forced output stop function 2 or timer restart function, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

Caution Comparator detection interrupt other than CMP0 and CMP2 cannot be used to clear the STOP mode.

Remark n = 0, 2

7. 14. 5 Caution for Using Timer KB Simultaneous Operation Function

As respects of INTP2m and comparator, Caution for Using Timer KB Simultaneous Operation Function is added.

Incorrect:

No applicable item

Correct:

14. 5 Caution for Using Timer KB Simultaneous Operation Function

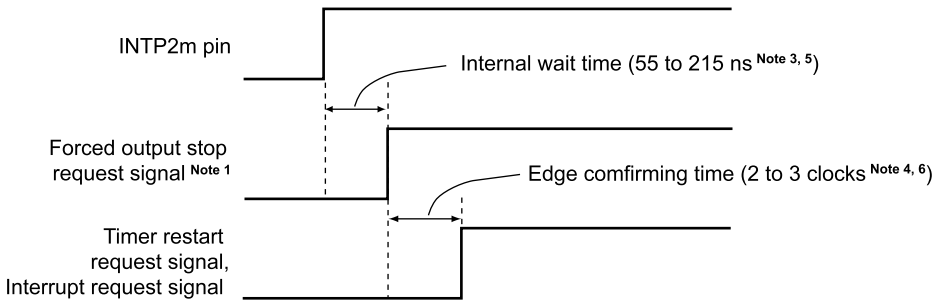
In addition to their use as an external interrupt input, the INTP2m pin output and the comparator output signal can be used as a trigger for functions that operate simultaneously with timer KB, such as the forced output stop function and timer restart function. The settings in peripheral function switch register 0 (PFSEL0) and the edge selection registers must be specified according to the function used. The width of the active signal required until each function starts operating differs.

When using INTP2m or the comparator output signal, refer to Tables 14-4 to 14-6 to specify the necessary register settings, and configure external circuits so that the required active signal width is assured.

Table 14-4. Relationship of INTP2m function, register settings, and active signal width

Function	Peripheral enable register setting	Edge setting registers	Necessary active signal width to operate each function		
			Interrupt	Forced output stop	Timer restart
External interrupt (STOP release is enabled)	TMRSTENm = 0	EGPn, EGNn	To 1 μs	-	-
Forced output stop Note 1	TMRSTENm = 1	CEGPp, CEGNp Note 2	55 to 215 ns Note 3 + 2 to 3 clocks Note 4	55 to 215 ns Note 3, 5	-
Timer restart	TMRSTENm = 1	CEGPp, CEGNp	55 to 215 ns Note 3 + 2 to 3 clocks Note 4	-	55 to 215 ns Note 3 + 2 to 3 clocks Note 4, 6

Figure 14-18. Generation Timing of Forced Output Stop Signal and Timer Restart Request Signal by INTP2m



Notes 1. Only INTP20 can be used as a trigger for forced output stop function 2.

2. The active level of INTP20 (used for forced output stop function 2) is high. Edge selection is only applied to detection of an interrupt signal.

3. 5 to 15 ns when noise filtering on INTP20 is disabled (PNFEN = 1)

4. For f_{CLK} or f_{PLL} (when PLLON = 1)

5. An additional output delay time (10 to 40 ns) is required from when forced output stop function 2 starts operating to when the level of the timer KB output changes.

Notes 6. Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.

Remark m = 0, 1 n = 20, 21 p = 7, 6

Table 14-5. Relationship of comparator 0 and 2 functions, register settings, and active signal width

Function	Peripheral enable register setting	Edge setting registers	Necessary active signal width to operate each function		
			Interrupt	Forced output stop	Timer restart
External interrupt (STOP release is enabled Note 1)	CMPnSTEN = 1	Rising edge only Note 2	To 150 ns Note 3	-	-
External interrupt (STOP release is disabled)	CMPnSTEN = 0	CEGPn, CEGNn	To 150 ns Note 3 + 2 to 3 clocks Note 4, 5	-	-
Forced output stop	CMPnSTEN = 1	**Note 6**	To 150 ns Note 3	To 150 ns Note 3, 7	-
Timer restart	CMPnSTEN = 0	CEGPn, CEGNn	To 150 ns Note 3 + 2 to 3 clocks Note 4, 5	-	To 150 ns Note 3 + 2 to 3 clocks Note 4, 5

Figure 14-19. Generation Timing of Forced Output Stop Request Signal by Comparator 0 and 2 (CMPnSTEN = 1)

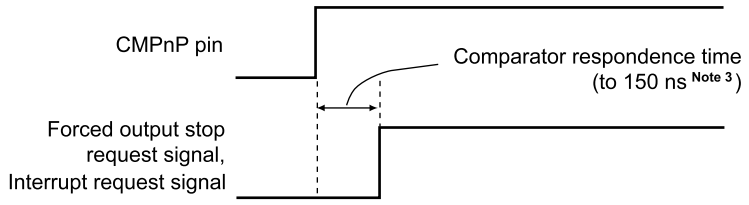
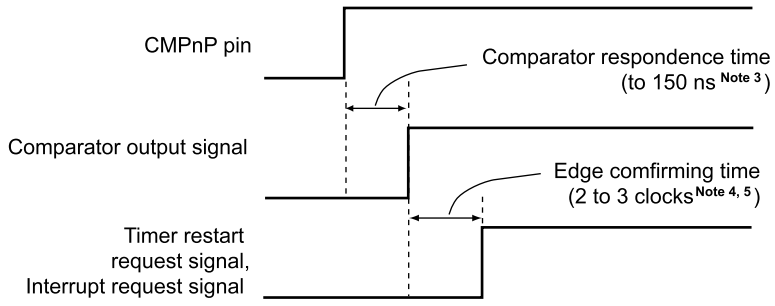


Figure 14-20. Generation Timing of Timer Restart Request Signal by Comparator 0 and 2 (CMPnSTEN = 0)



Notes 1. When noise filtering is set to "0, 0" by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL)

2. To change the level of the edge direction, invert the comparator output signal by using the CnINV bit in the comparator n control register (CnCTL).

3. This is the time required when noise filtering is set to "0, 0" by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL).

If a setting other than "0, 0" is specified, the specified noise elimination width is added.

4. For f_{CLK} or f_{PLL} (when PLLON = 1)

Notes 5. Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.

6. The active level of INTP20 (used for forced output stop function 2) is high.

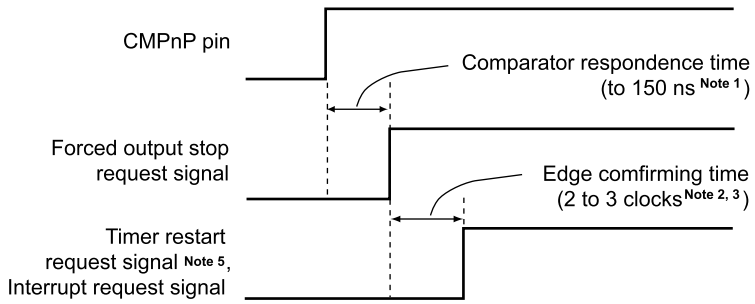
7. An additional output delay time (10 to 40 ns) is required from when forced output stop function 2 starts operating to when the level of the timer KB output changes.

Remark n = 0, 2

Table 14-6. Relationship of comparator 1, 3, 4, and 5 functions, register settings, and active signal width

Function	Peripheral enable register setting	Edge setting registers	Necessary active signal width to operate each function		
			Interrupt	Forced output stop	Timer restart
External interrupt (STOP release is disabled)	-	CEGPn, CEGNn	To 150 ns Note 1 + 2 to 3 clocks Note 2, 3	-	-
Forced output stop	-	**Note 4**	To 150 ns Note 2 + 2 to 3 clocks Note 3, 4	To 150 ns Note 2, 5	-
Timer restart Note 6	-	CEGPn, CEGNn	To 150 ns Note 2 + 2 to 3 clocks Note 3, 4	-	To 150 ns Note 2 + 2 to 3 clocks Note 3, 4

Figure 14-21. Generation Timing of Forced Output Stop Request Signal and Timer Restart Request Signal by Comparator 1, 3, 4, and 5



Notes 1. When noise filtering is set to "0, 0" by using the CnDFS1 and CnDFS0 bits in the comparator n control register (CnCTL). If a setting other than "0, 0" is specified, the specified noise elimination width is added.

2. For f_{CLK} or f_{PLL} (when PLLON = 1)

3. Until the timer restart function starts operating, an additional clock cycle is required after the timer restart request signal is received, and an additional output delay time (10 to 40 ns) is required until the level of the timer KB output changes.

4. The active level of INTP20 (used for forced output stop function 2) is high.

5. An additional output delay time (10 to 40 ns) is required from when forced output stop function 2 starts operating to when the level of the timer KB output changes.

6. The timer restart function can be used for comparator 1 and 3 only .

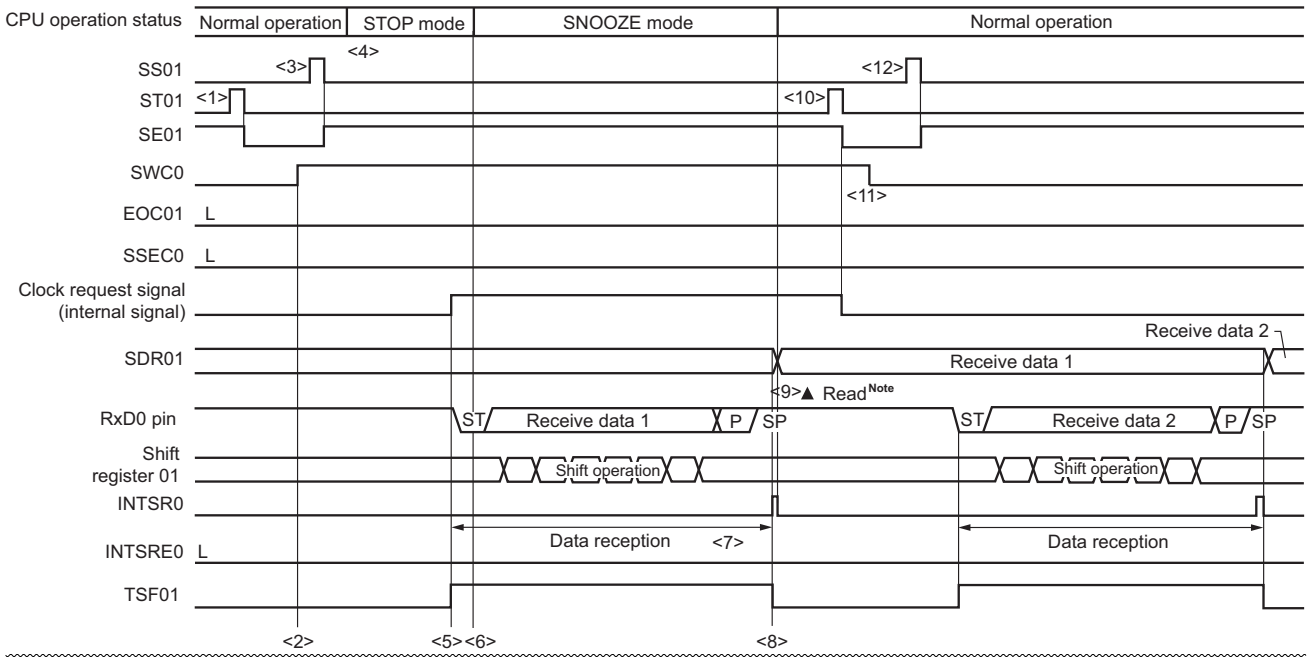
Remark n = 1, 3 to 5

8. Timing Chart of SNOOZE Mode Operation (p.666, 667, 669)

Incorrect the clock request signal (internal signal) timing is revised.

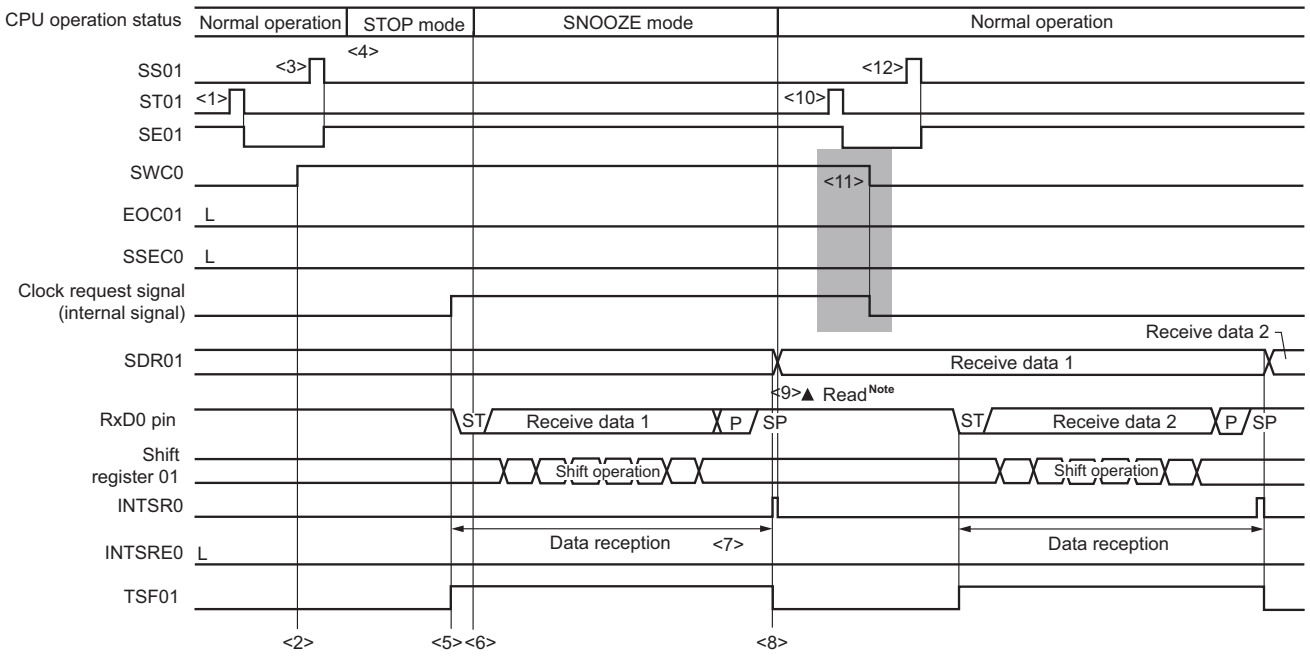
Incorrect:

Figure 15-90. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)



Correct:

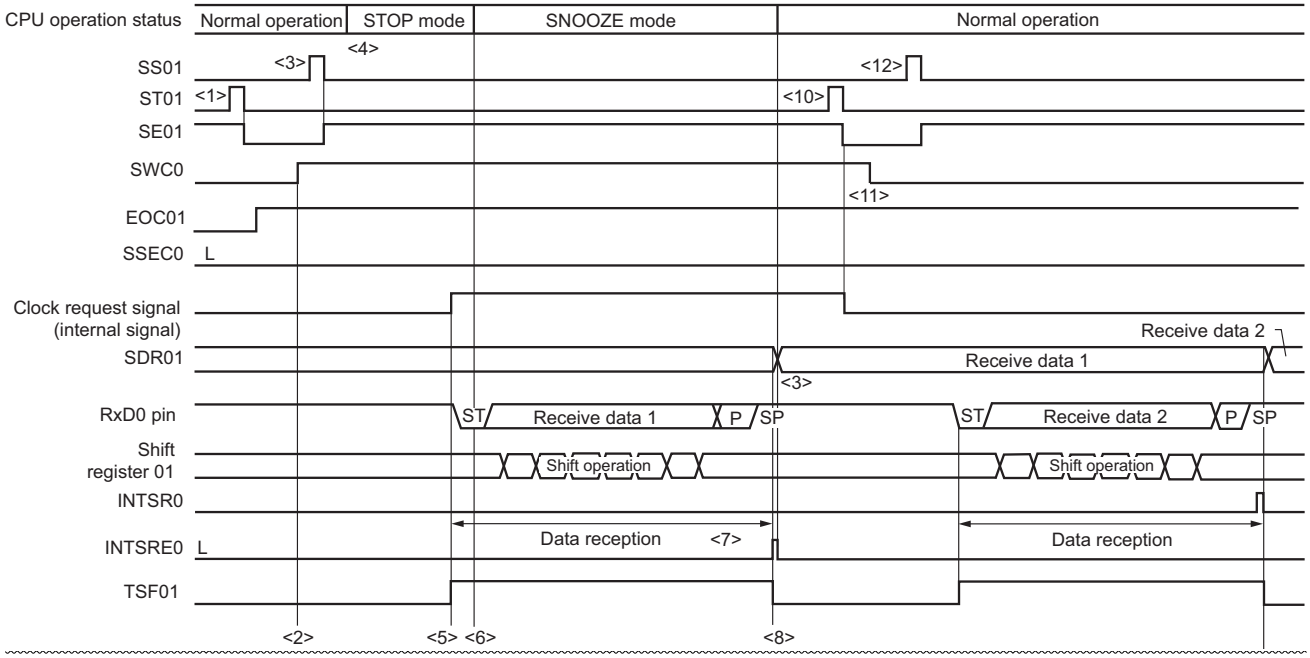
Figure 15-90. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)



Incorrect the timing chart of clock request signal (internal signal) and SDR01 is revised.

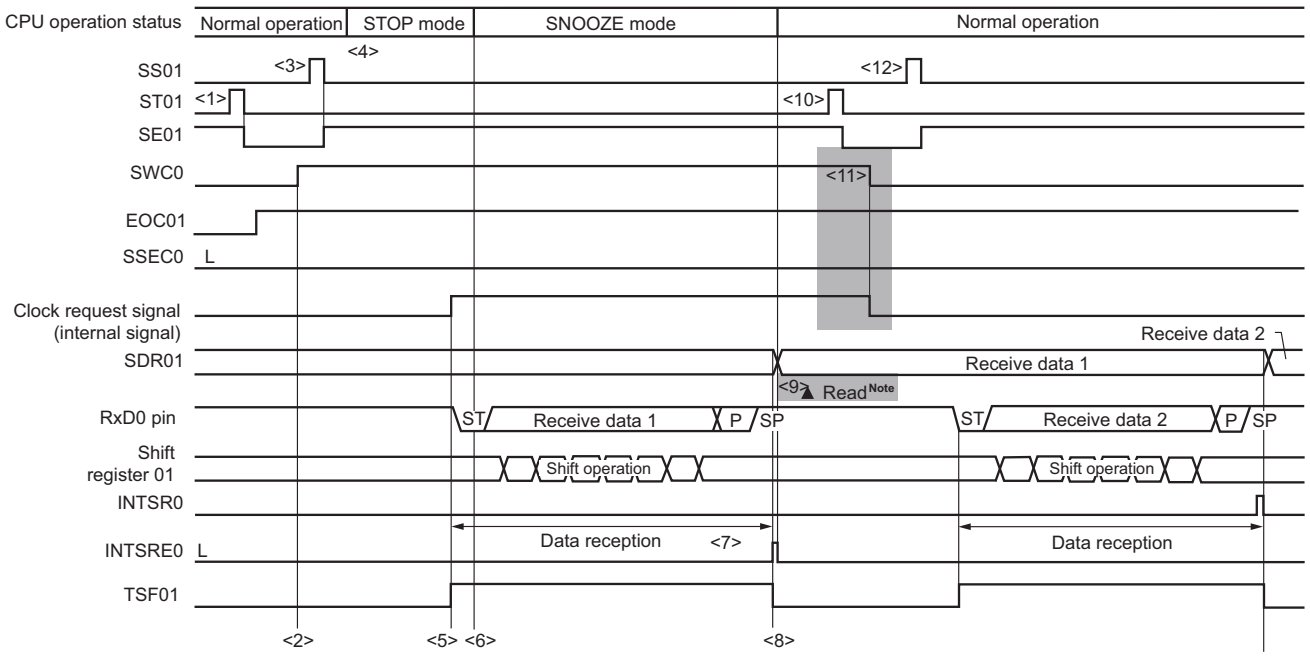
Incorrect:

Figure 15-91. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)



Correct:

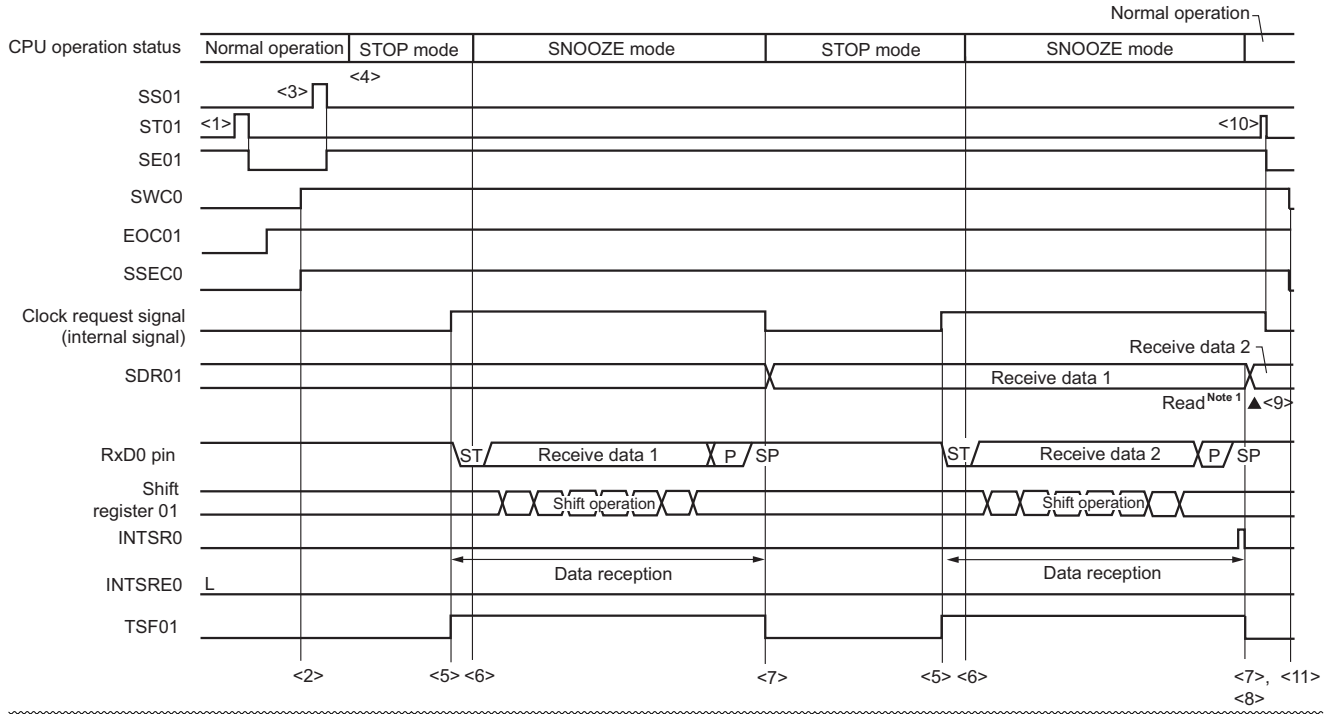
Figure 15-91. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)



Incorrect the clock request signal (internal signal) timing chart is revised.

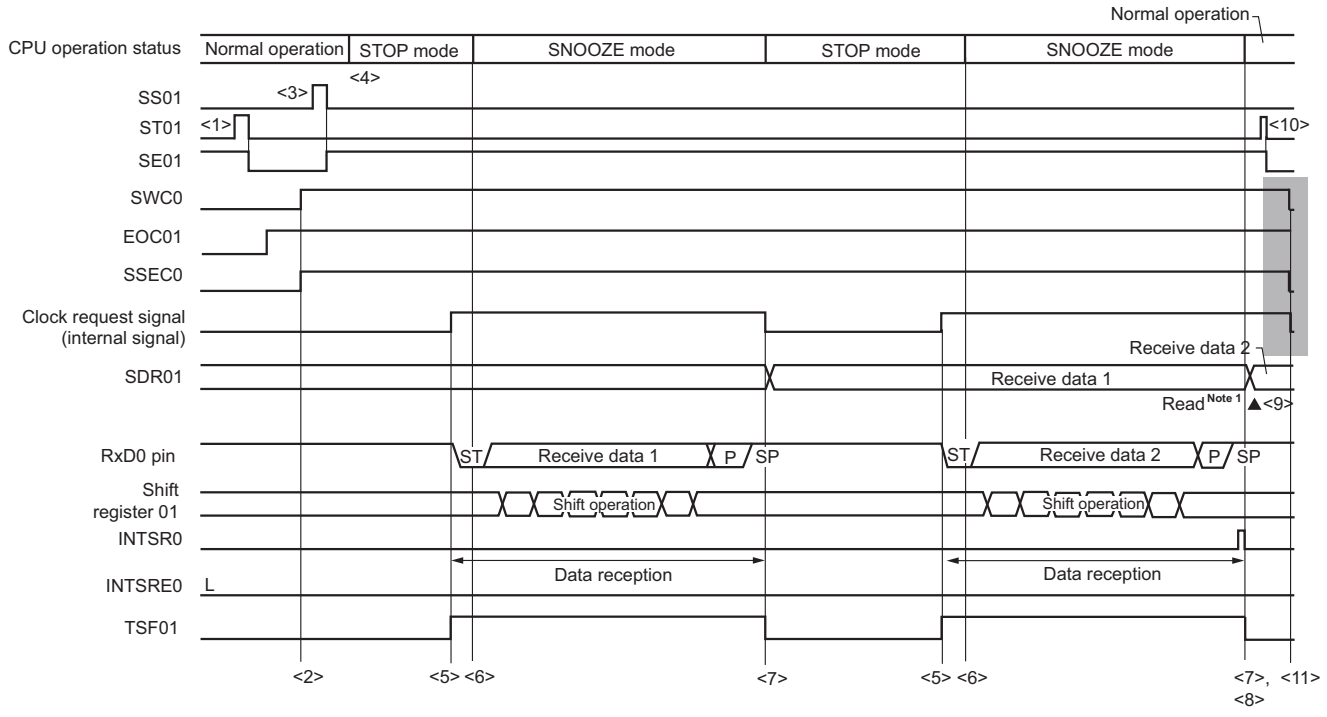
Incorrect:

Figure 15-93. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



Correct:

Figure 15-93. Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 1)



9. Table 20-1. Interrupt Source List (2/3)

Note for the interrupt source list is added.

Incorrect:

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 40 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 20-1.

3. INTCMP1, INTCMP3, INTCMP4, and INTCMP5 cannot be used to clear the STOP mode.

Correct:

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 40 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 20-1.

3. INTCMP1, INTCMP3, INTCMP4, and INTCMP5 cannot be used to clear the STOP mode.

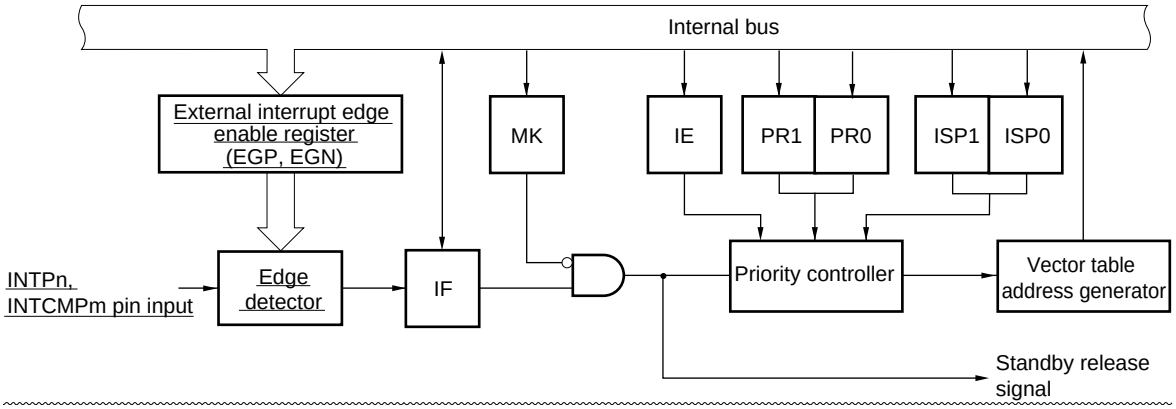
About interrupt generation timing, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

10. Figure 20-1. Basic Configuration of Interrupt Function

Incorrect the basic configuration of interrupt function is revised.

Incorrect:

(B) External maskable interrupt (INTPn, INTCMPm)



IF: Interrupt request flag

IE: Interrupt enable flag

ISP0: In-service priority flag 0

ISP1: In-service priority flag 1

MK: Interrupt mask flag

PR0: Priority specification flag 0

PR1: Priority specification flag 1

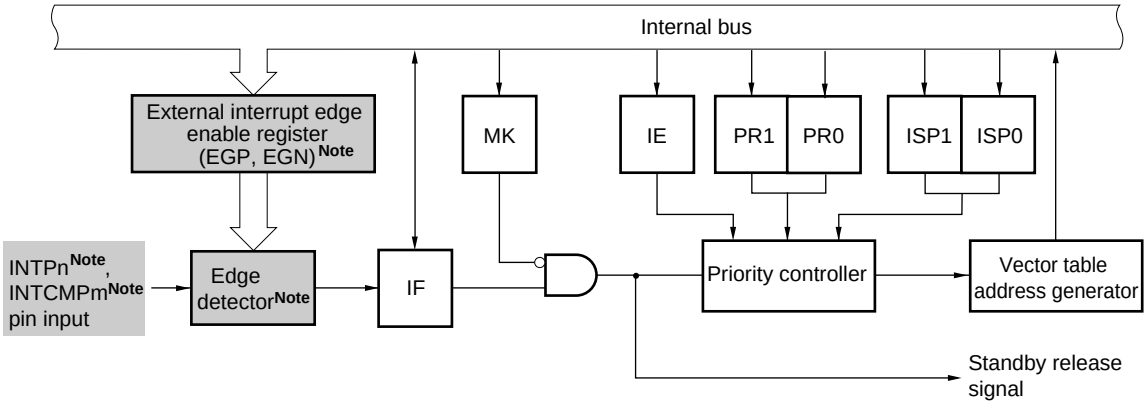
Remark 20-pin: n = 0, 20, 21, 22, m = 0 to 3

30-pin: n = 0, 4, 11, 20 to 23, m = 0 to 5

38-pin: n = 0, 3, 4, 9 to 11, 20 to 23, m = 0 to 5

Correct:

(B) External maskable interrupt (INTPn[Note], INTCMPm[Note])



Note According to setting for using of the timer KB simultaneous function (the timer KB forced output stop function and timer restart function), the interrupt signal pass and the interrupt generation timing and the edge enable register for INTP20 and INTP21 and INTCMPm vary. For details, see **14. 5 Caution for Using Timer KB Simultaneous Operation Function**.

IF: Interrupt request flag

IE: Interrupt enable flag

ISP0: In-service priority flag 0

ISP1: In-service priority flag 1

MK: Interrupt mask flag

PR0: Priority specification flag 0

PR1: Priority specification flag 1

Remark 20-pin: n = 0, 20, 21, 22, m = 0 to 3

30-pin: n = 0, 4, 11, 20 to 23, m = 0 to 5

38-pin: n = 0, 3, 4, 9 to 11, 20 to 23, m = 0 to 5

11. Table 21-1. Operating Statuses in HALT Mode (2/2)

Incorrect description about the comparator operation in HALT mode is revised.

Incorrect:

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock	
			When CPU Is Operating on XT1 Clock (f_{XT})	When CPU Is Operating on External Subsystem Clock (f_{EXS})
System clock			Clock supply to the CPU is stopped	
	Main system clock	f_{IH}	Operation disabled	
		f_X		
		f_{EX}		
	Subsystem clock	f_{XT}	Operation continues (cannot be stopped)	Cannot operate
		f_{EXS}	Cannot operate	Operation continues (cannot be stopped)
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops	
CPU			Operation stopped	
Code flash memory				
Data flash memory				
RAM				
Port (latch)			Status before HALT mode was set is retained	
Timer array unit			Operable when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).	
Timer KB0 to KB2				
Timer KC0				
Real-time clock (RTC)			Operable	
12-bit interval timer				
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**	
A/D converter			Operation disabled	
Programmable gain amplifier			Operable (However, this is not used, since the operation has been disabled for the A/D converter that is the destination for input of the PGA output signal)	
Comparator			Operable (When in the low-consumption RTC mode (RTCLPC = 1 in the OSMC register), this can be used only when the STOP mode cancel is set (CMPnSTEN = 1 in the PFSEL0 register) by the comparator interrupt detection and the noise filter is not used (n = 0, 2))	

(Omitted)

Correct:

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock	
			When CPU Is Operating on XT1 Clock (f_{XT})	When CPU Is Operating on External Subsystem Clock (f_{EXS})
System clock			Clock supply to the CPU is stopped	
	Main system clock	f_{IH}	Operation disabled	
		f_X		
		f_{EX}		
	Subsystem clock	f_{XT}	Operation continues (cannot be stopped)	Cannot operate
		f_{EXS}	Cannot operate	Operation continues (cannot be stopped)
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops	
CPU			Operation stopped	
Code flash memory				
Data flash memory				
RAM				
Port (latch)			Status before HALT mode was set is retained	
Timer array unit			Operable when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).	
Timer KB0 to KB2				
Timer KC0				
Real-time clock (RTC)			Operable	
12-bit interval timer				
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**	
A/D converter			Operation disabled	
Programmable gain amplifier			Operable (However, this is not used, since the operation has been disabled for the A/D converter that is the destination for input of the PGA output signal)	
Comparator			Only CMP0 and CMP2 are operable. (When in the low-consumption RTC mode (RTCLPC = 1 in the OSMC register), CMPn can be used only when the STOP mode cancel is set (CMPnSTEN = 1 in the PFSEL0 register) by the comparator interrupt detection and the noise filter is not used. (n = 0, 2))	

(Omitted)

12. Table 21-2. Operating Statuses in STOP Mode

Incorrect description about the comparator operation in STOP mode is revised.

Incorrect:

STOP Mode Setting / Item			When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{IH}	Stopped		
		f_X			
		f_{EX}			
	Subsystem clock	f_{XT}	Status before STOP mode was set is retained		
		f_{EXS}			
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops		
CPU			Operation stopped		
Code flash memory					
Data flash memory					
RAM					
Port (latch)			Status before STOP mode was set is retained		
Timer array unit			Operation disabled		
Timer KB0 to KB2					
Timer KC0					
Real-time clock (RTC)			Operable		
12-bit interval timer					
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**		
A/D converter			Wakeup operation is enabled (switching to the SNOOZE mode)		
Programmable gain amplifier			Operable		
Comparator			Operable (Only for channels set to enable cancellation of STOP mode and when digital filter is not used)		

(Omitted)

Correct:

STOP Mode Setting / Item			When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{IH}	Stopped		
		f_X			
		f_{EX}			
	Subsystem clock	f_{XT}	Status before STOP mode was set is retained		
		f_{EXS}			
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops		
CPU			Operation stopped		
Code flash memory					
Data flash memory					
RAM					
Port (latch)			Status before STOP mode was set is retained		
Timer array unit			Operation disabled		
Timer KB0 to KB2					
Timer KC0					
Real-time clock (RTC)			Operable		
12-bit interval timer					
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**		
A/D converter			Wakeup operation is enabled (switching to the SNOOZE mode)		
Programmable gain amplifier			Operable		
Comparator			Only CMP0 and CMP2 are operable when the STOP mode cancel is set (CMPnSTEN = 1 in the PFSEL0 register) by the comparator interrupt detection and the noise filter is not used. (n = 0, 2)		

(Omitted)

13. Table 21-3. Operating Statuses in SNOOZE Mode

Incorrect description about the comparator operation in SNOOZE mode is revised.

Incorrect:

Item \ STOP Mode Setting			When Inputting CSI00/UART0 Data Reception Signal or A/D Converter Timer Trigger Signal While in STOP Mode
			When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})
System clock			Clock supply to the CPU is stopped
	Main system clock	f_{IH}	Operation started
		f_X	Stopped
		f_{EX}	
	Subsystem clock	f_{XT}	Use of the status while in the STOP mode continues
		f_{EXS}	
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops
CPU			Operation stopped
Code flash memory			
Data flash memory			
RAM			
Port (latch)			Use of the status while in the STOP mode continues
Timer array unit			Operation disabled
Timer KB0 to KB2			
Timer KC0			
Real-time clock (RTC)			Operable
12-bit interval timer			
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**
A/D converter			Operable
Programmable gain amplifier			Operable
Comparator			Operable (Only for channels set to enable cancellation of STOP mode and when digital filter is not used)

(Omitted)

Correct:

STOP Mode Setting / Item			When Inputting CSI00/UART0 Data Reception Signal or A/D Converter Timer Trigger Signal While in STOP Mode
			When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})
System clock			Clock supply to the CPU is stopped
	Main system clock	f_{IH}	Operation started
		f_X	Stopped
		f_{EX}	
	Subsystem clock	f_{XT}	Use of the status while in the STOP mode continues
		f_{EXS}	
	f_{IL}		Set by bits 0 (WDSTBYON) and 4 (WDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and WDTON = 0: Stops • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, WDTON = 1, and WDSTBYON = 0: Stops
CPU			Operation stopped
Code flash memory			
Data flash memory			
RAM			
Port (latch)			Use of the status while in the STOP mode continues
Timer array unit			Operation disabled
Timer KB0 to KB2			
Timer KC0			
Real-time clock (RTC)			Operable
12-bit interval timer			
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**
A/D converter			Operable
Programmable gain amplifier			Operable
Comparator			Only CMP0 and CMP2 are operable when the STOP mode cancel is set (CMPnSTEN = 1 in the PFSEL0 register) by the comparator interrupt detection and the noise filter is not used. (n = 0, 2)

(Omitted)

14. 32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

Descriptions of the data memory STOP mode low supply voltage data retention characteristics are added.

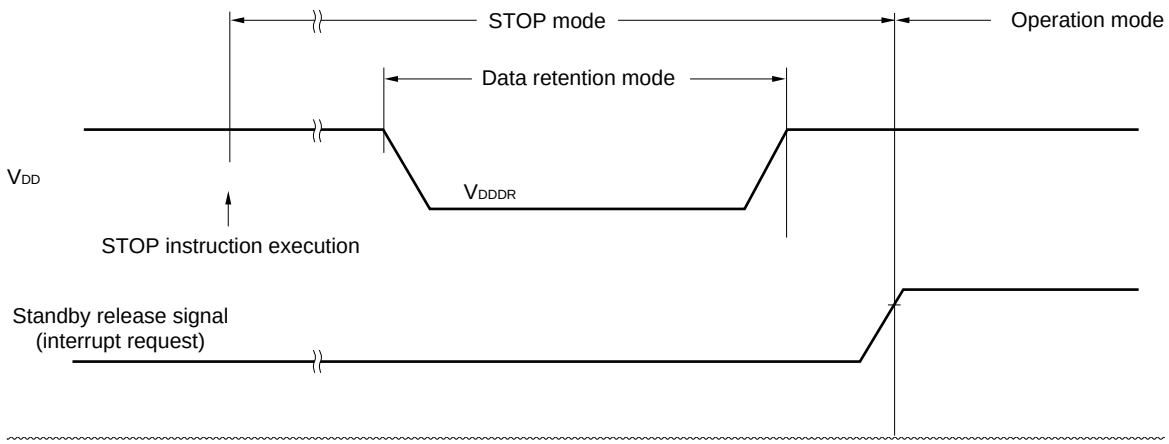
Incorrect:

32.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



Correct:

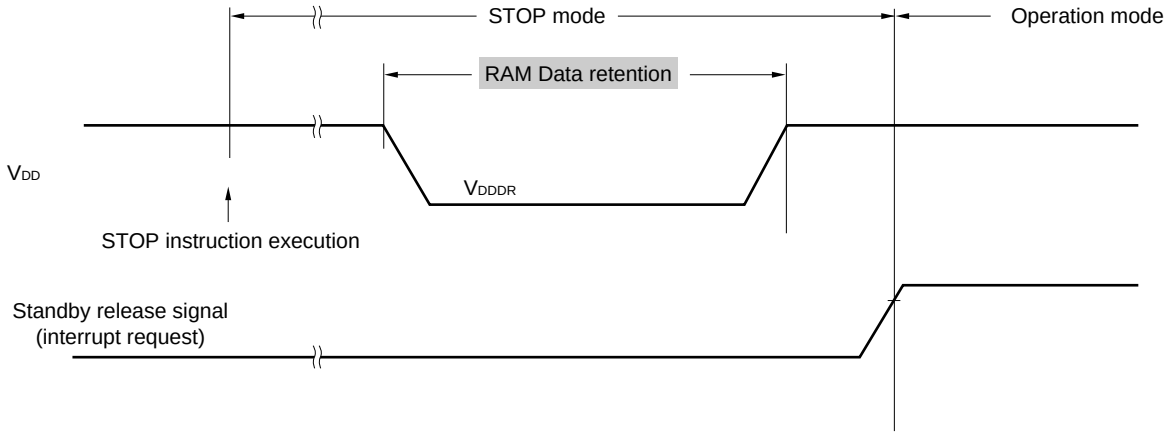
32.7 RAM Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Caution When CPU is operated at the voltage of out of the operation voltage range, RAM data is not retained. Therefore, set STOP mode before the supplied voltage is below the operation voltage range.



15. 33.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

Descriptions of the data memory STOP mode low supply voltage data retention characteristics are added.

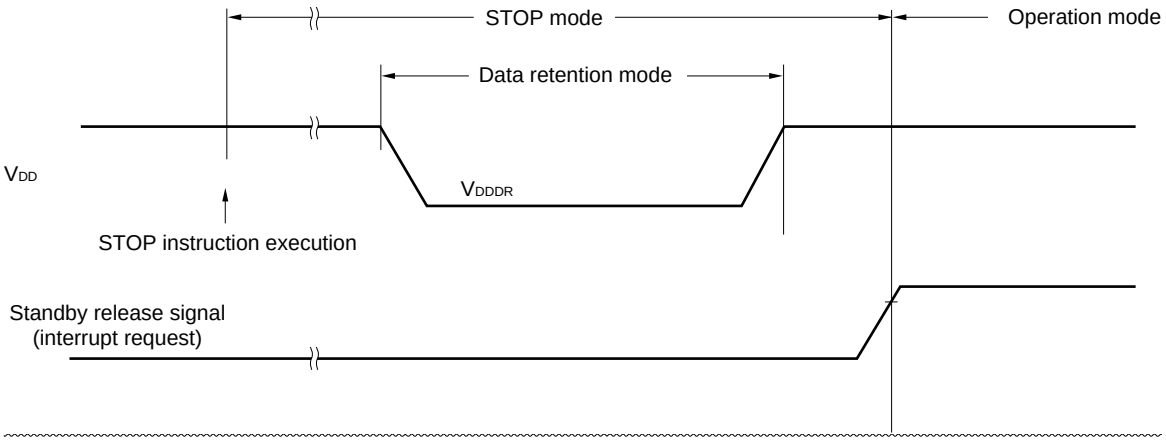
Incorrect:

33.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +125°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47[Note]		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



Correct:

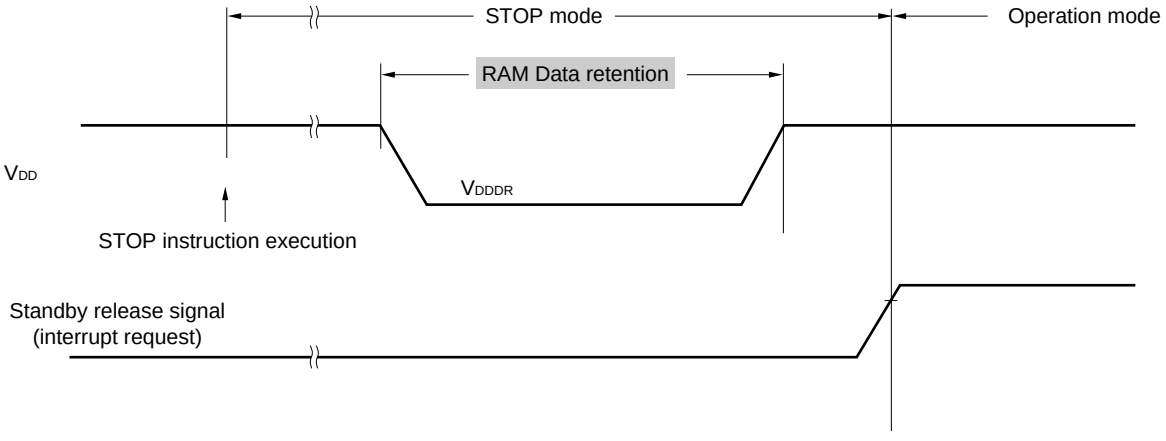
33.7 RAM Data Retention Characteristics

(T_A = –40 to +125°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47[Note]		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.

Caution When CPU is operated at the voltage of out of the operation voltage range, RAM data is not retained. Therefore, set STOP mode before the supplied voltage is below the operation voltage range.

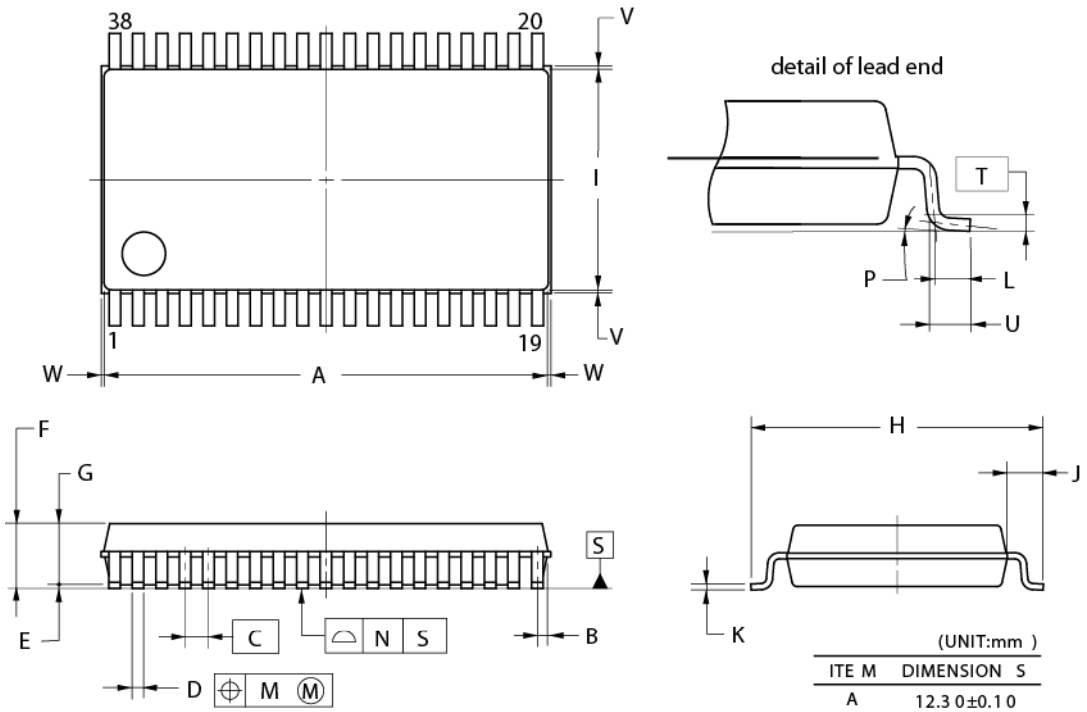


16. 34.3 38-pin Products

Incorrect descriptions of the package code and dimensions are revised.

Incorrect:

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-SSOP38-6.1x12.3-0.65	PRSP0038JA-B	P38MC-65-GAA-2	0.3



NOT E

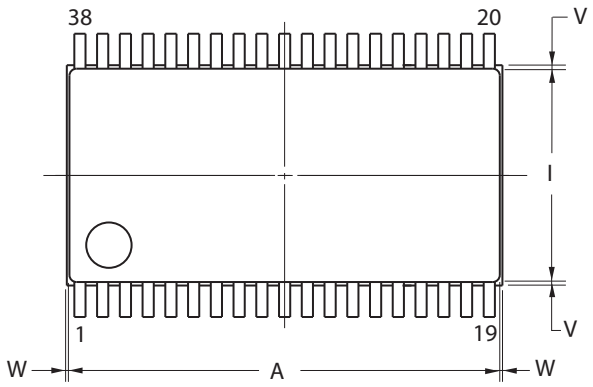
Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition .

(UNIT:mm)

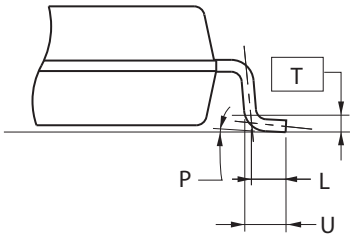
ITE M	DIMENSION S
A	12.30±0.10
B	0.30
C	0.65 (T.P.)
D	$0.30^{+0.10}_{-0.05}$
E	0.125±0.075
F	2.00 MAX .
G	1.70±0.10
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.10}_{-0.05}$
L	0.50
M	0.10
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX .
W	0.15 MAX .

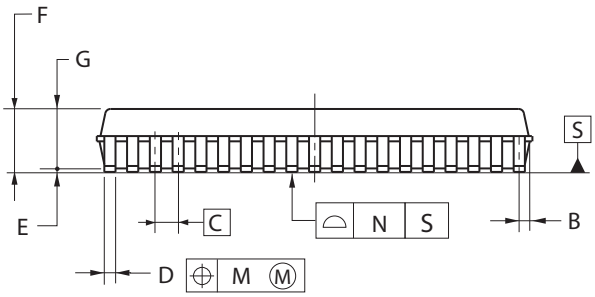
Correct:

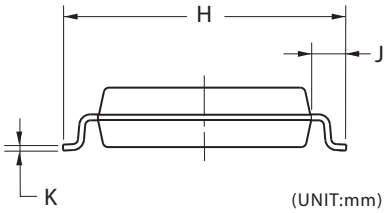
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-SSOP38-0300-0.65	PRSP0038JA-A	P38MC-65-2A4-2	0.3



detail of lead end







NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

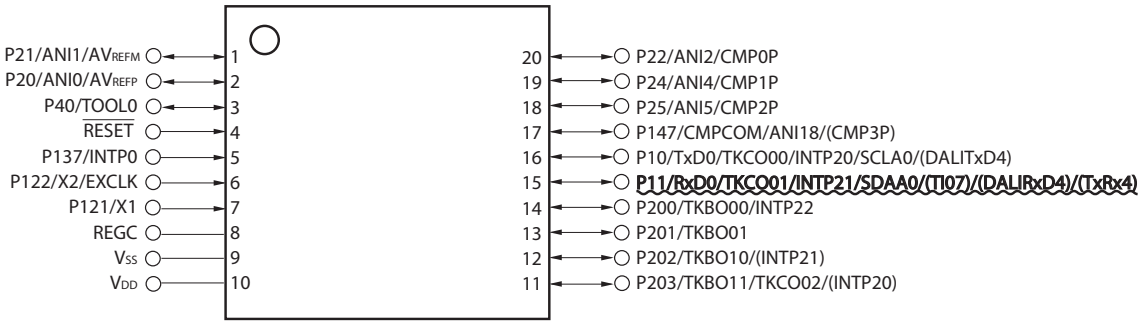
(UNIT:mm)

ITEM	DIMENSIONS
A	12.30±0.10
B	0.30
C	0.65 (T.P.)
D	0.32 +0.08 -0.07
E	0.125±0.075
F	2.00 MAX.
G	1.70±0.10
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	0.17 +0.08 -0.07
L	0.50
M	0.10
N	0.10
P	3° +7° -3°
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

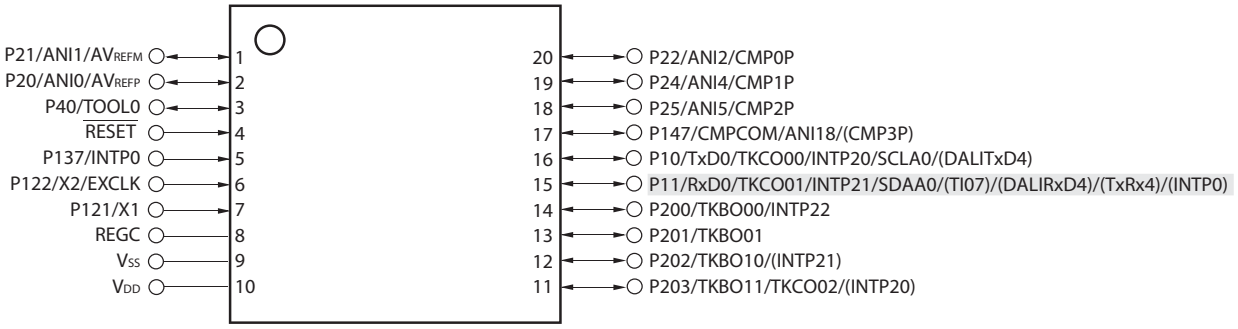
17. 1.3.1 20-pin products

Incorrect alternate-function pin is revised.

Incorrect:



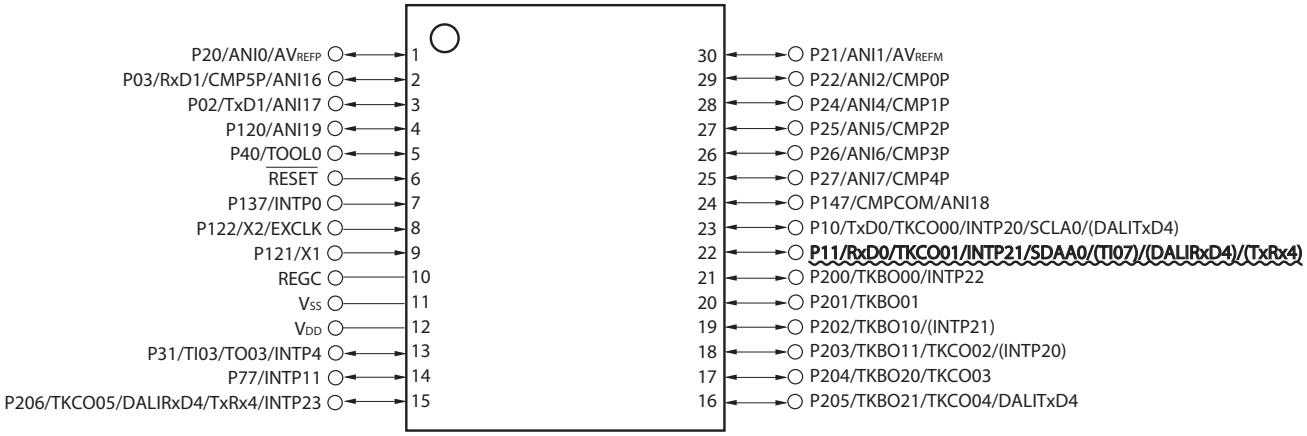
Correct:



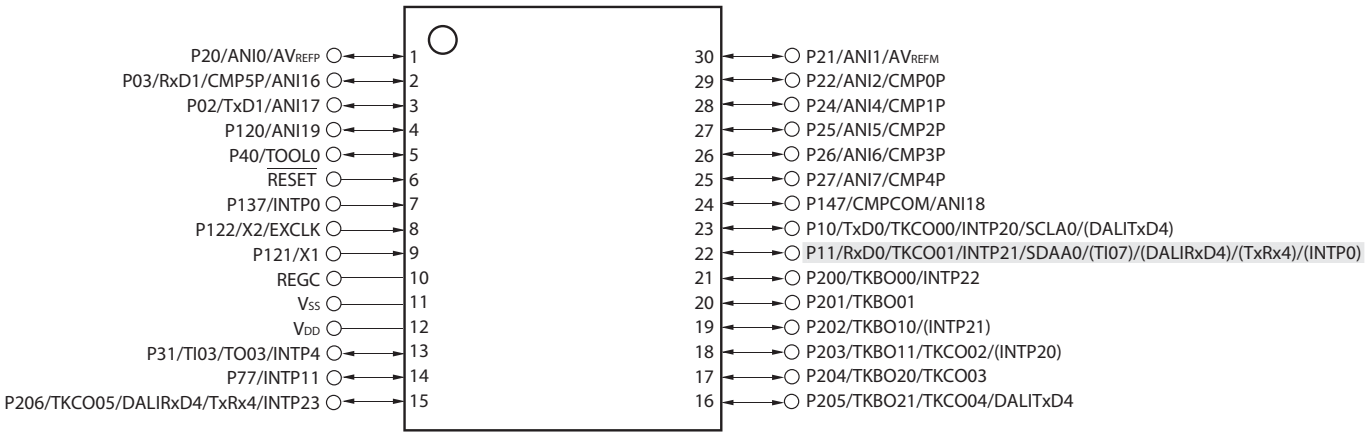
18. 1.3.2 30-pin products

Incorrect alternate-function pin is revised.

Incorrect:



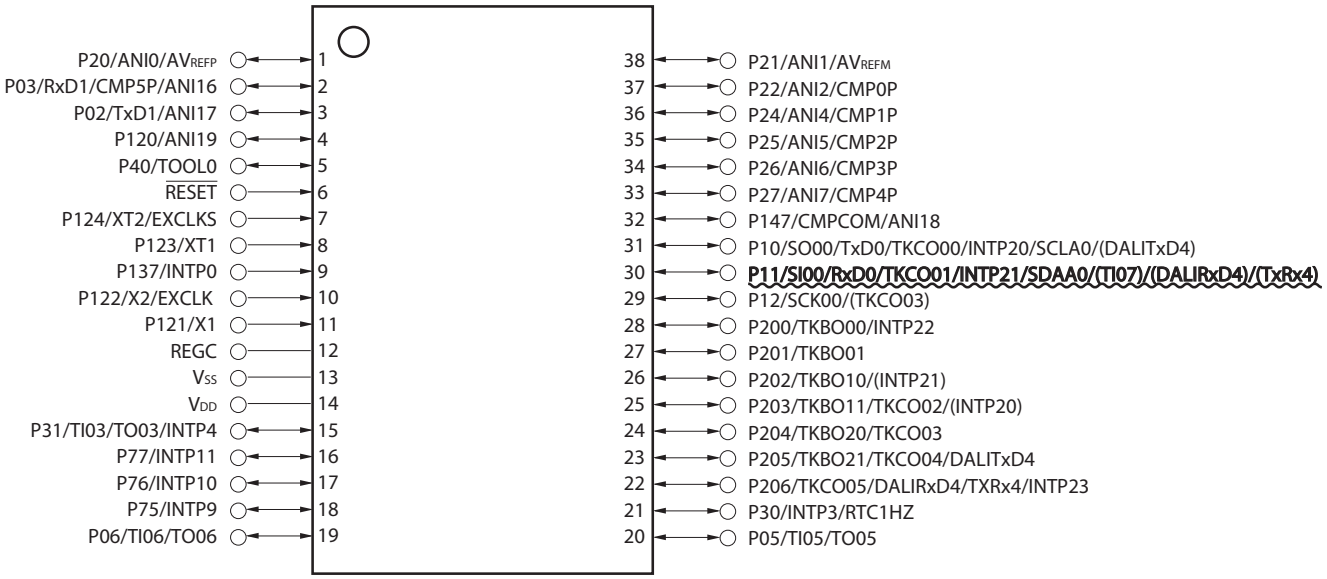
Correct:



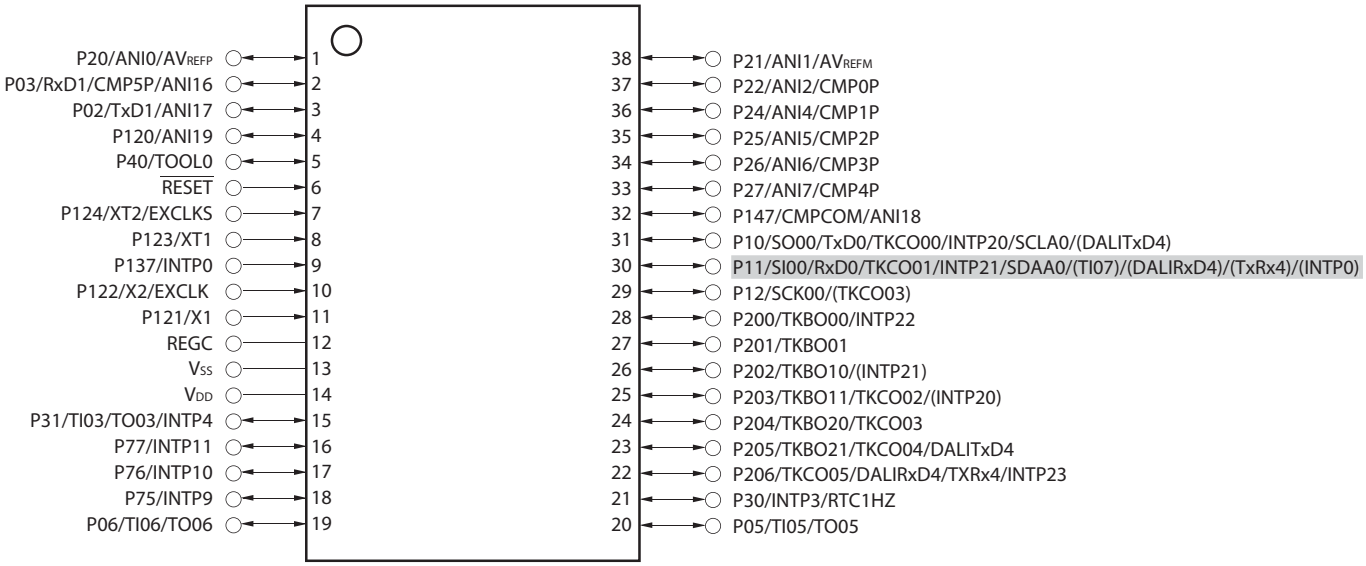
19. 1.3.3 38-pin products

Incorrect alternate-function pin is revised.

Incorrect:



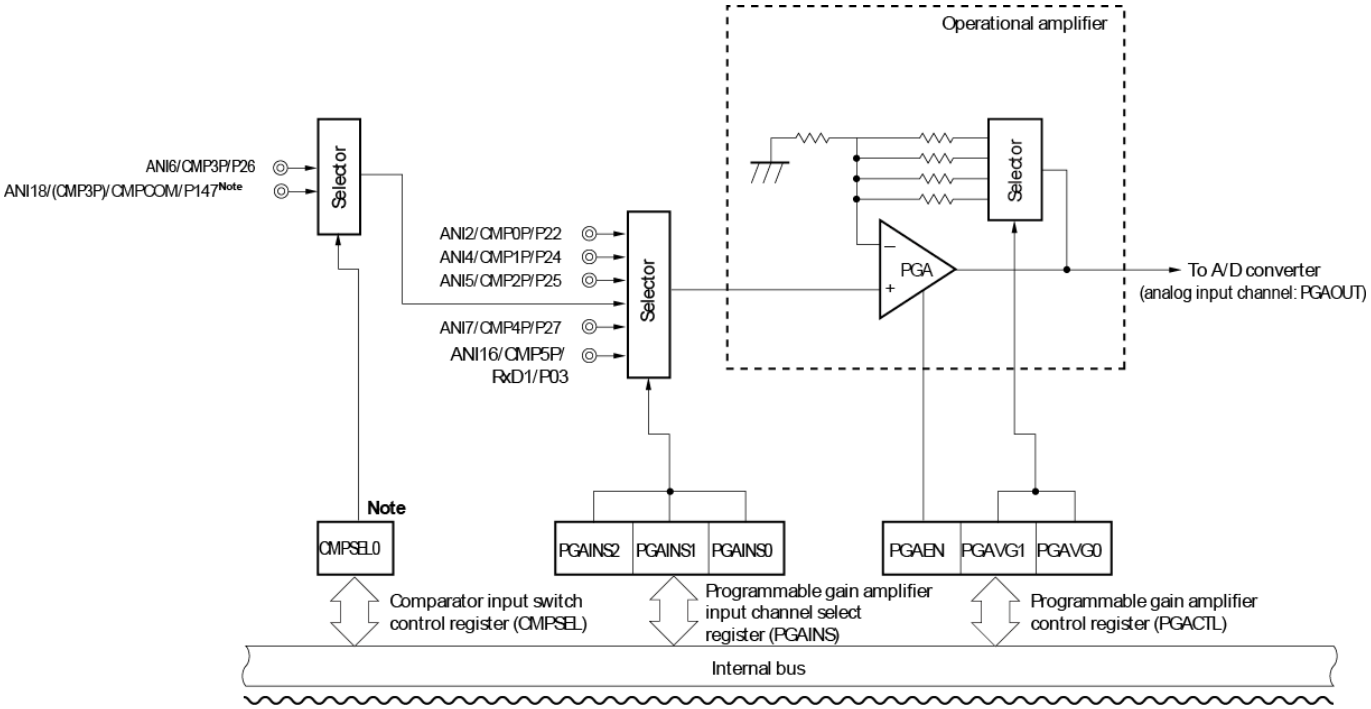
Correct:



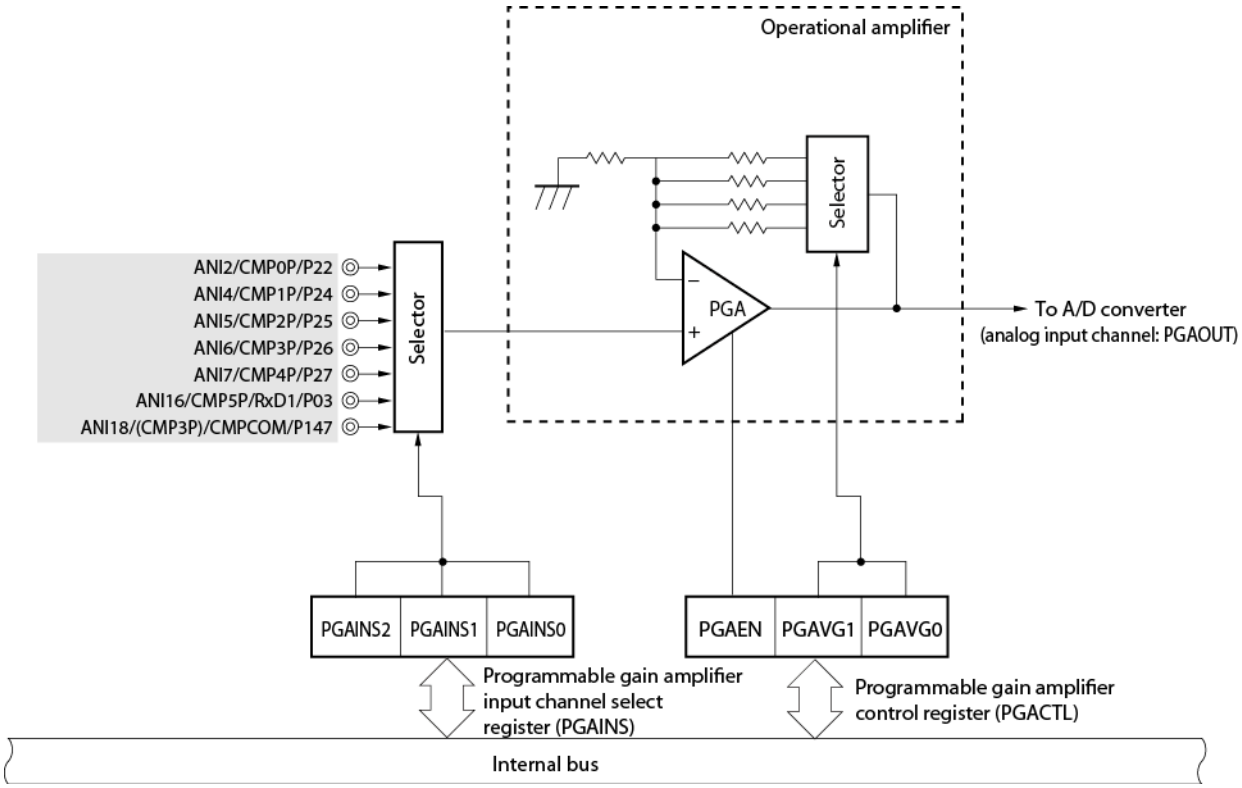
20. Figure 13-1. Block Diagram of Operational Amplifier

Incorrect block diagram is revised.

Incorrect:



Correct:



21. 13.3.3 Programmable gain amplifier input channel select register (PGAINS)

Incorrect description of programmable gain amplifier input channel select register (PGAINS) is revised.

Incorrect:

Figure 13-4. Format of Programmable Gain Amplifier Input Channel Select Register (PGAINS)

Address: F0551H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PGAINS	0	0	0	0	0	PGAINS2	PGAINS1	PGAINS0

PGAINS2	PGAINS1	PGAINS0	Analog input channel for input to programmable gain amplifier
0	0	0	ANI2/CMP0P
0	0	1	ANI4/CMP1P
0	1	0	ANI5/CMP2P
0	1	1	ANI6/CMP3P **or ANI18/(CMP3P)**Note
1	0	0	ANI7/CMP4P
1	0	1	ANI16/CMP5P
Other than above			Setting prohibited

Note Selected by the comparator input switch control register (CMPSEL) (20-pin products only)

Caution Set the PGAINS register during stop operation of the programmable gain amplifier (PGAEN = 0).

Correct:

Figure 13-4. Format of Programmable Gain Amplifier Input Channel Select Register (PGAINS)

Address: F0551H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PGAINS	0	0	0	0	0	PGAINS2	PGAINS1	PGAINS0

PGAINS2	PGAINS1	PGAINS0	Analog input channel for input to programmable gain amplifier
0	0	0	ANI2/CMP0P
0	0	1	ANI4/CMP1P
0	1	0	ANI5/CMP2P
0	1	1	ANI6/CMP3P
1	0	0	ANI7/CMP4P
1	0	1	ANI16/CMP5P
1	1	0	ANI18/CMPCOM/(CMP3P Note)
Other than above			Setting prohibited

Note Selected by the comparator input switch control register (CMPSEL) (20-pin products only)

Caution Set the PGAINS register during stop operation of the programmable gain amplifier (PGAEN = 0).