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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0124A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G1H Descriptions in the User's Manual: Hardware Rev. 1.30 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G1H Group	Lot No. All lots	Reference Document	RL78/G1H User's Manual: Hardware Rev. 1.30 R01UH0575EJ0130 (Jun. 2022)		

This document describes misstatements found in the RL78/G1H User's Manual: Hardware Rev. 1.30 (R01UH0575EJ0130).

Corrections

Applicable Item	Applicable Page	Contents
9.3.4 Real-time clock control register 1 (RTCC1)	Page 242	Incorrect descriptions revised
Figure 9-20. Procedure for Reading Real-time Clock	Page 254	Incorrect descriptions revised
Figure 9-21. Procedure for Writing Real-time Clock	Page 255	Incorrect descriptions revised
31.3.2 Supply current characteristics	Page 828 to Page 831	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0575EJ0130	
1	9.3.4 Real-time clock control register 1 (RTCC1)		Page 242	Page 3
2	Figure 9-20. Procedure for Reading Real-time Clock		Page 254	Page 4
3	Figure 9-21. Procedure for Writing Real-time Clock		Page 255	Page 4
4	31.3.2 Supply current characteristics		Page 828 to Page 831	Page 5 to Page 7

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G1H Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0124A/E	Jan. 20, 2023	First edition issued Corrections No.1 to No.5 revised (this document)

1. 9.3.4 Real-time clock control register 1 (RTCC1) (Page 242)

Incorrect:

Figure 11-6. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)

RIFG	Constant-period interrupt status flag
0	Fixed-cycle interrupt is not generated.
1	Fixed-cycle interrupt is generated.
This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to “1”. This flag is cleared when “0” is written to it. Writing “1” to it is invalid.	

RWST	Wait status flag of real-time clock
0	Counter is operating.
1	Mode to read or write counter value
This status flag indicates whether the setting of the RWAIT bit is valid. Before reading or writing the counter value, confirm that the value of this flag is 1.	

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
This bit controls the operation of the counter. Be sure to write “1” to it to read or write the counter value. As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When RWAIT = 1, it takes up to one cycle of f_{RTC} until the counter value can be read or written (RWST = 1). When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up. However, when it wrote a value to second count register, it will not keep the overflow event.	

Correct:

Figure 11-6. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)

RIFG	Constant-period interrupt status flag
0	Fixed-cycle interrupt is not generated.
1	Fixed-cycle interrupt is generated.
This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to “1”. This flag is cleared when “0” is written to it. Writing “1” to it is invalid.	

RWST	Wait status flag of real-time clock
0	Counter is operating.
1	Mode to read or write counter value
This status flag indicates whether the setting of the RWAIT bit is valid. Before reading or writing the counter value, confirm that the value of this flag is 1.	

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value
This bit controls the operation of the counter. Be sure to write “1” to it to read or write the counter value. As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt. When RWAIT = 1, it takes up to one cycle of f_{RTC} until the counter value can be read or written (RWST = 1). When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up. However, when it wrote a value to second count register, it will not keep the overflow event.	

2. Figure 9-20 Procedure for Reading Real-time Clock (Page 254)

Incorrect:

Note Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

Caution **Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.**

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

Correct:

Note Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

Caution **Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.**

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

3. Figure 9-21 Procedure for Writing Real-time Clock (Page 255)

Incorrect:

Note Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

Cautions 1. **Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.**

Cautions 2. **When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.**

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence. All the registers do not have to be set and only some registers may be written.

Correct:

Note Be sure to confirm that RWST = 0 before setting HALT/STOP mode.

Cautions 1. **Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.**

Cautions 2. **When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.**

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence. All the registers do not have to be set and only some registers may be written.

4. 31.3.2 Supply current characteristics (Page 828 to Page 831)

Incorrect:

31.3.2 Supply current characteristics

(TA = −40 to +85° C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V) **(1/2)**

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fIH = 32 MHz Note 3	Basic operation	VDD = 3.0 V			2.5		mA
			HS (high-speed main) mode Note 5	fIH = 32 MHz Note 3	Normal operation	VDD = 3.0 V			5.5	10.6	mA
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input			5.9	13.2	
						Resonator connection			6.0	13.2	
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input			6.8	17.5	
						Resonator connection			6.9	17.5	

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Notes 3. When high-speed system clock and subsystem clock are stopped.

Notes 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

Notes 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remarks 2. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remarks 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remarks 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Correct:

31.3.2 Supply current characteristics

(TA = −40 to +85° C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V) **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fIH = 32 MHz Note 3	Basic operation	VDD = 3.0 V		2.5		mA
			HS (high-speed main) mode Note 5	fIH = 32 MHz Note 3	Normal operation	VDD = 3.0 V		5.5	10.6	mA
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		5.9	13.2	
						Resonator connection		6.0	13.2	
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		6.8	17.5	
						Resonator connection		6.9	17.5	

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), and LS (low-speed main) modes.
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

Notes 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Notes 3. When high-speed system clock and subsystem clock are stopped.

Notes 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

Notes 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remarks 2. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remarks 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remarks 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(TA = −40 to +85° C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fIH = 32 MHz Note 4	VDD = 3.0 V		0.5	2.63	mA
				fIH = 24 MHz Note 4	VDD = 3.0 V		0.42	2.03	
				fIH = 16 MHz Note 4	VDD = 3.0 V		0.39	1.50	
			LS (low-speed main) mode Note 7	fIH = 8 MHz Note 4	VDD = 3.0 V		270	800	μA
					VDD = 2.0 V		270	800	
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.31	1.69	mA
					Resonator connection		0.41	1.91	
				fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		0.16	0.94	
					Resonator connection		0.21	1.02	
			LS (low-speed main) mode Note 7	fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		110	610	μA
					Resonator connection		150	660	
				fMX = 8 MHz Note 3, VDD = 2.0 V	Square wave input		110	610	
					Resonator connection		150	660	
	IDD3 Note 6	STOP mode Note 8	TA = –40°C				0.19		μA
			TA = +25°C				0.30	0.59	
			TA = +50°C				0.41	3.42	
			TA = +70°C				0.80	6.03	
			TA = +85°C				1.53	10.39	

Notes 1. Total current flowing into VDD and EVDD0, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

Notes 2. During HALT instruction execution by flash memory.

Notes 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Notes 4. When high-speed system clock and subsystem clock are stopped.

Notes 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**

Notes 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

(TA = −40 to +85° C, 1.8 V ≤ VDD ≤ 3.6 V, VSS = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 6	fIH = 32 MHz Note 4	VDD = 3.0 V		0.5	2.63	mA
				fIH = 24 MHz Note 4	VDD = 3.0 V		0.42	2.03	
				fIH = 16 MHz Note 4	VDD = 3.0 V		0.39	1.50	
			LS (low-speed main) mode Note 6	fIH = 8 MHz Note 4	VDD = 3.0 V		270	800	μA
					VDD = 2.0 V		270	800	
			HS (high-speed main) mode Note 6	fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.31	1.69	mA
					Resonator connection		0.41	1.91	
				fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		0.16	0.94	
					Resonator connection		0.21	1.02	
			LS (low-speed main) mode Note 6	fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		110	610	μA
					Resonator connection		150	660	
				fMX = 8 MHz Note 3, VDD = 2.0 V	Square wave input		110	610	
					Resonator connection		150	660	
	IDD3	STOP mode Note 7	TA = –40°C				0.19		μA
			TA = +25°C				0.30	0.59	
			TA = +50°C				0.41	3.42	
			TA = +70°C				0.80	6.03	
			TA = +85°C				1.53	10.39	

Notes 1. Total current flowing into VDD and EVDD0, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The following points apply in the HS (high-speed main), LS (low-speed main) modes.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

Notes 2. During HALT instruction execution by flash memory.

Notes 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Notes 4. When high-speed system clock and subsystem clock are stopped.

Notes 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).

Notes 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz

Notes 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remarks 2. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
Remarks 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
Remarks 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

Notes 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 3.6 V@1 MHz to 8 MHz

Notes 7. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remarks 2. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
Remarks 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
Remarks 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C