

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A062A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G1G Descriptions in the Hardware User's Manual Rev. 1.20 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G1G R5F11Exxx	Lot No.	Reference Document	RL78/G1G User's Manual: Hardware Rev.1.20 R01UH0499EJ0120 (Jul. 2015)		
		All lots				

This document describes misstatements found in the RL78/G1G User's Manual: Hardware Rev.1.20 (R01UH0499EJ0120).

Corrections

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4.2.1 Port 0 Figure 4-1 Pin Block Diagram of P00	Page 71	Caution added
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4.2.2 Port 1 Figure 4-7 Pin Block Diagram of P14	Page 79	Incorrect descriptions revised
4.2.2 Port 1 Figure 4-8 Pin Block Diagram of P15	Page 80	Caution added
4.2.2 Port 1 Figure 4-9 Pin Block Diagram of P16	Page 81	Caution added
4.2.2 Port 1 Figure 4-10 Pin Block Diagram of P17	Page 82	Caution added
4.2.4 Port 3 Figure 4-12 Pin Block Diagram of P30	Page 86	Caution added
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8.4.10 Reset synchronous PWM mode Figure 8 - 57 Block Diagram of Reset Synchronous PWM Mode	Page 366	Incorrect descriptions revised
8.4.11 Complementary PWM mode Figure 8 - 59 Block Diagram of Complementary PWM Mode	Page 370	Incorrect descriptions revised
8.4.12 PWM3 mode Figure 8 - 62 Block Diagram of PWM3 Mode	Page 375	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

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	Document No. English R01UH0499EJ0120	
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3	4.2.2 Port 1 Figure 4-3 Pin Block Diagram of P10	Page 75 Page 5
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12	8.3.9 Timer RD output control register (TRDOCR) Figure 8-12 Format of Timer RD output control register(TRDOCR) [Reset Synchronous PWM Mode,Complementary PWM Mode]	- Page 14
13	8.3.11 Timer RD control register i (TRDCRi) (i = 0 or 1) Figure 8-18 Format of Timer RD control register 0 (TRDCR0) [Complementary PWM Mode]	Page 313 Page 15
14	8.3.18 Timer RD counter i (TRDi) (i = 0 or 1) Figure 8 - 31 Format of Timer RD counter i (TRDi) (i = 0 or 1) [Reset Synchronous PWM Mode and PWM3 Mode]	Page 328 Page 15
15	8.3.18 Timer RD counter i (TRDi) (i = 0 or 1) Figure 8 - 32 Format of Timer RD counter i (TRDi) (i = 0 or 1) [Complementary PWM Mode (TRD0)]	Page 328 Page 16
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~~Incorrect,OLD: Bold with underline~~; Correct,NEW: Gray hatched

Revision History

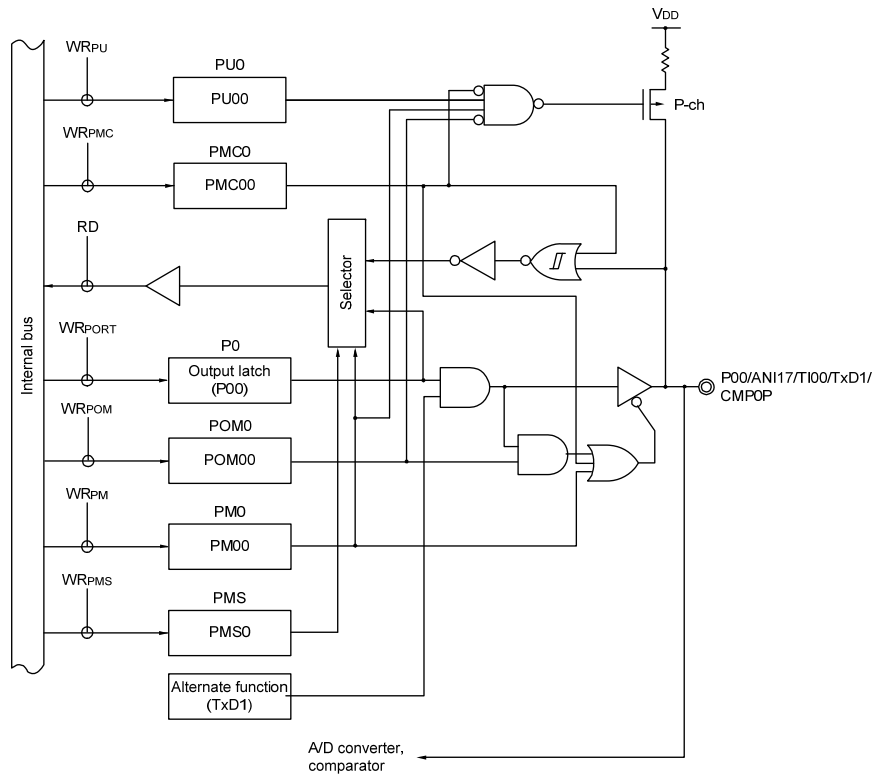
RL78/G1G User's Manual: Hardware Rev.1.20 Correction for Incorrect Description Notice

Document Number	Date	Description
TN-RL*-A062A/E	Jun. 29, 2016	First edition issued No.1 to 21 in corrections (This notice)

1. 4.2.1 Port 0 Figure 4-1 Pin Block Diagram of P00 (Page 71)

Old:

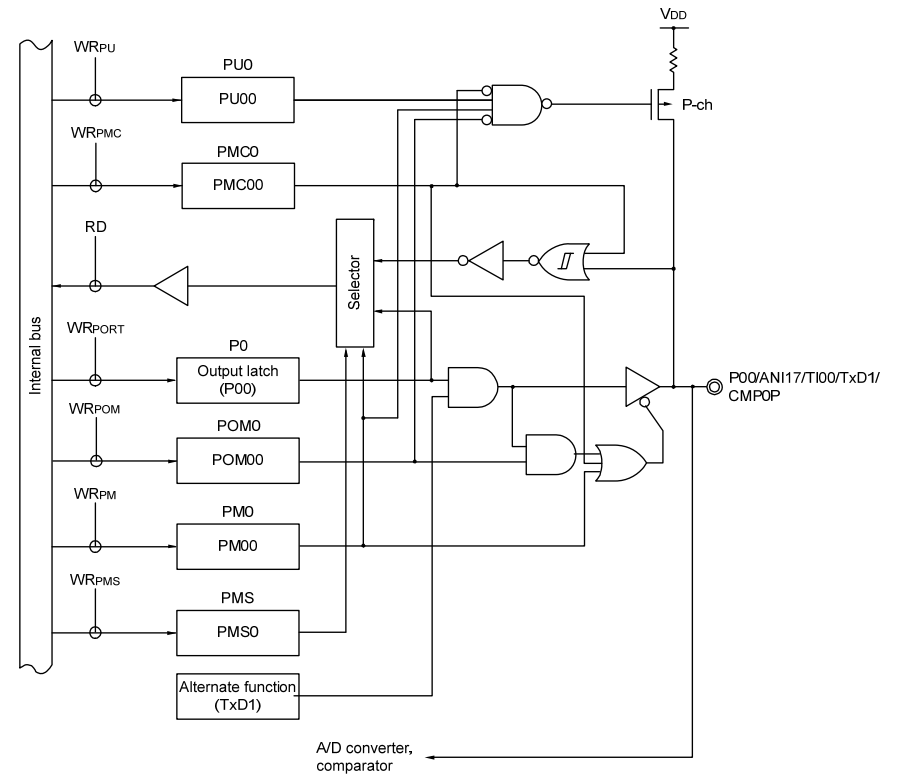
Figure 4 - 1 Block Diagram of P00



(omitted)

New:

Figure 4 - 1 Block Diagram of P00



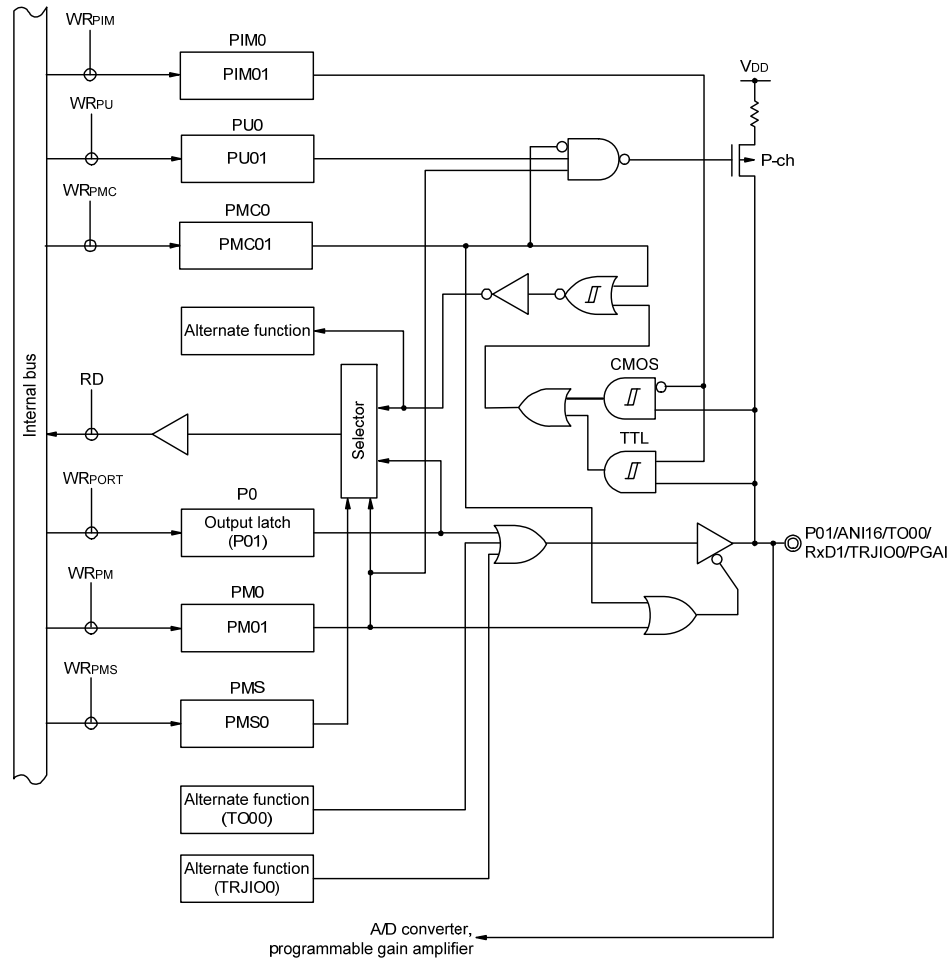
Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

(omitted)

2. 4.2.1 Port 0 Figure 4-2 Pin Block Diagram of P01 (Page 72)

Old:

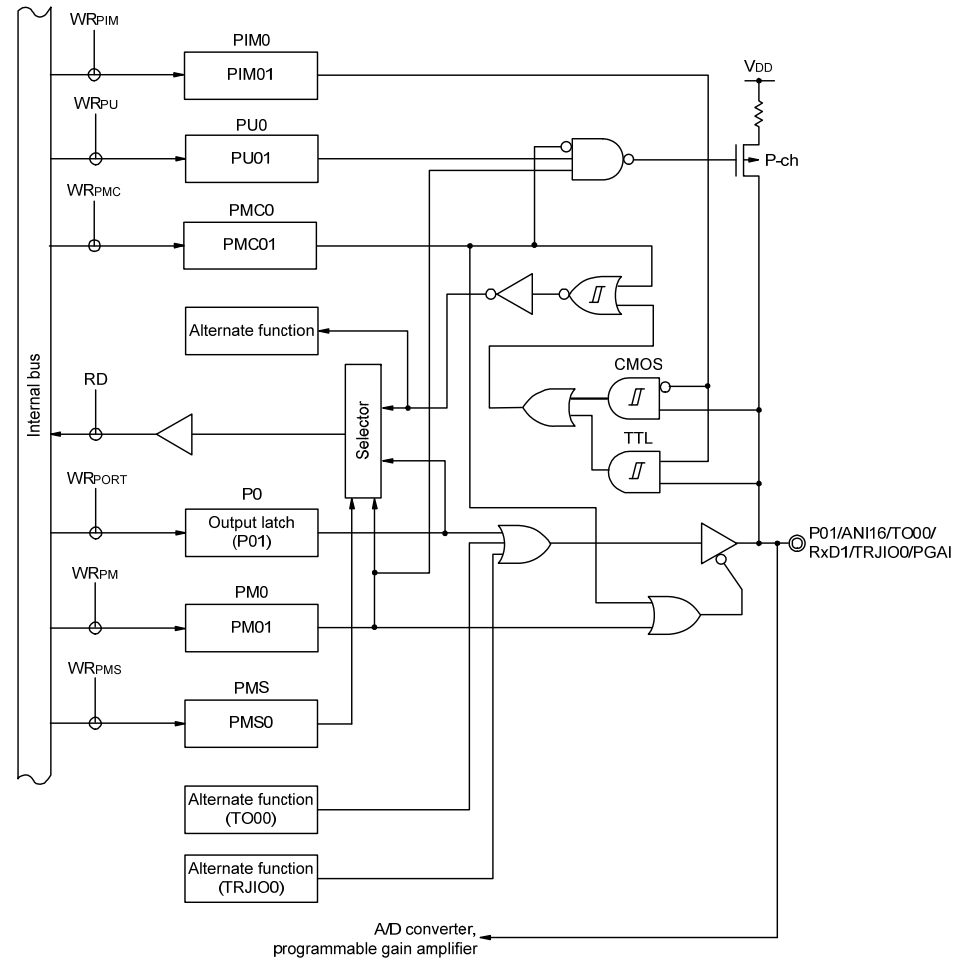
Figure 4 - 2 Block Diagram of P01



(omitted)

New:

Figure 4 - 2 Block Diagram of P01



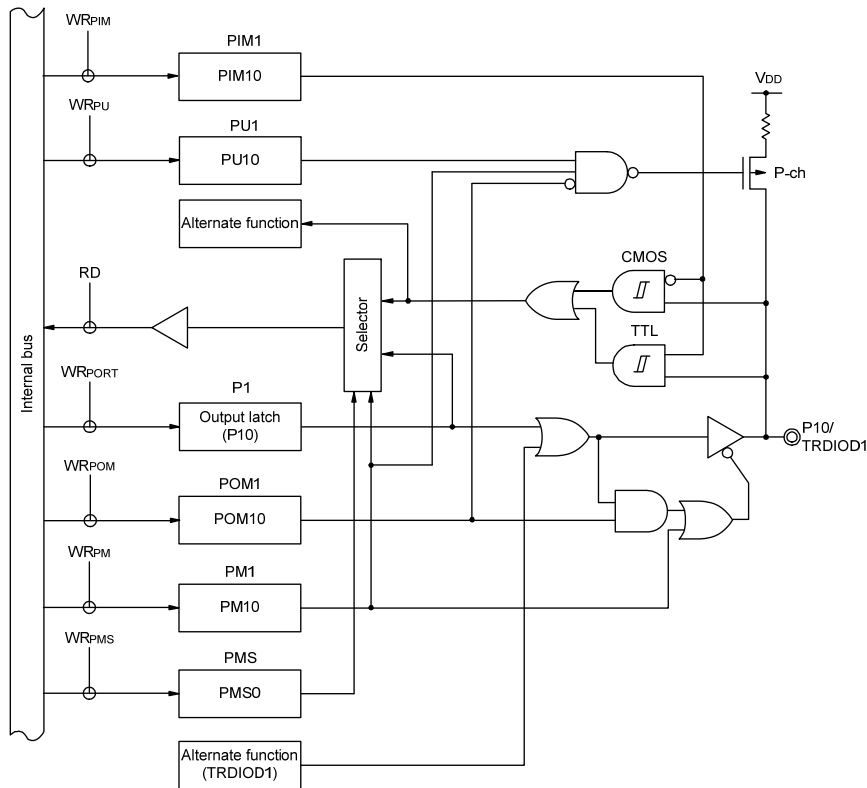
Caution Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, electric power may increase in the case of high level input. It is recommended to input a low level to prevent increase of the electric power.

(omitted)

3. 4.2.2 Port 1 Figure 4-3 Pin Block Diagram of P10 (Page 75)

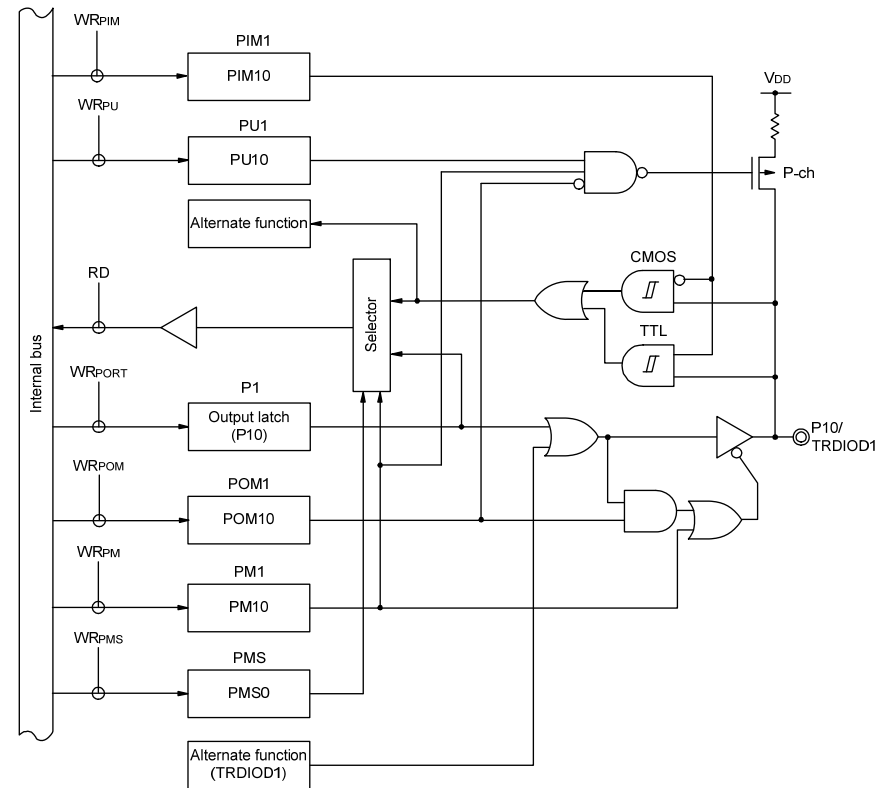
Old:

Figure 4 - 3 Block Diagram of P10



New:

Figure 4 - 3 Block Diagram of P10



Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

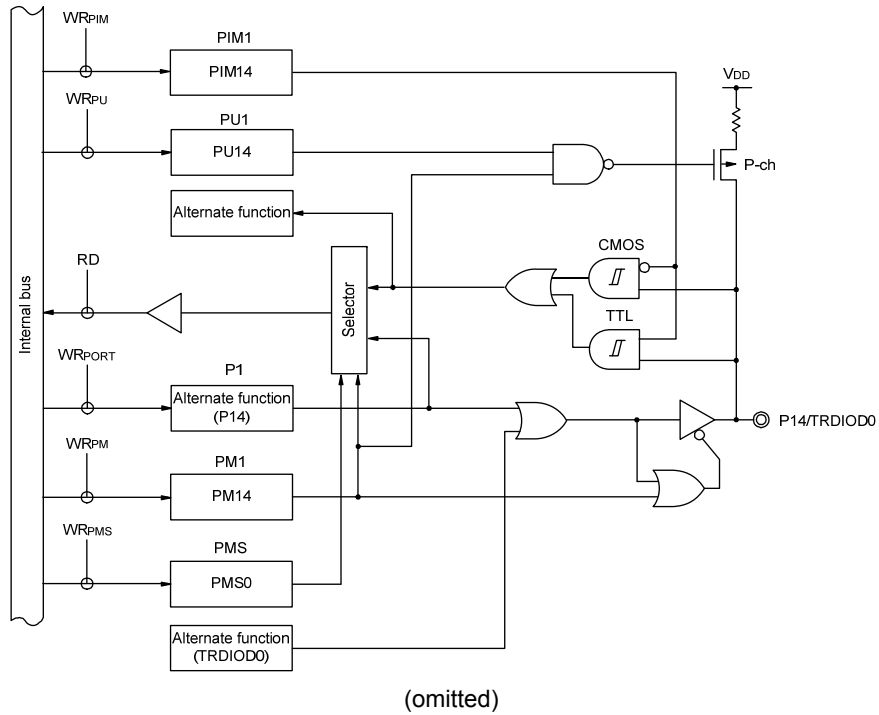
Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, electric power may increase in the case of high level input. It is recommended to input a low level to prevent increase of the electric power.

(omitted)

4. 4.2.2 Port 1 Figure 4-7 Pin Block Diagram of P14 (Page 79)

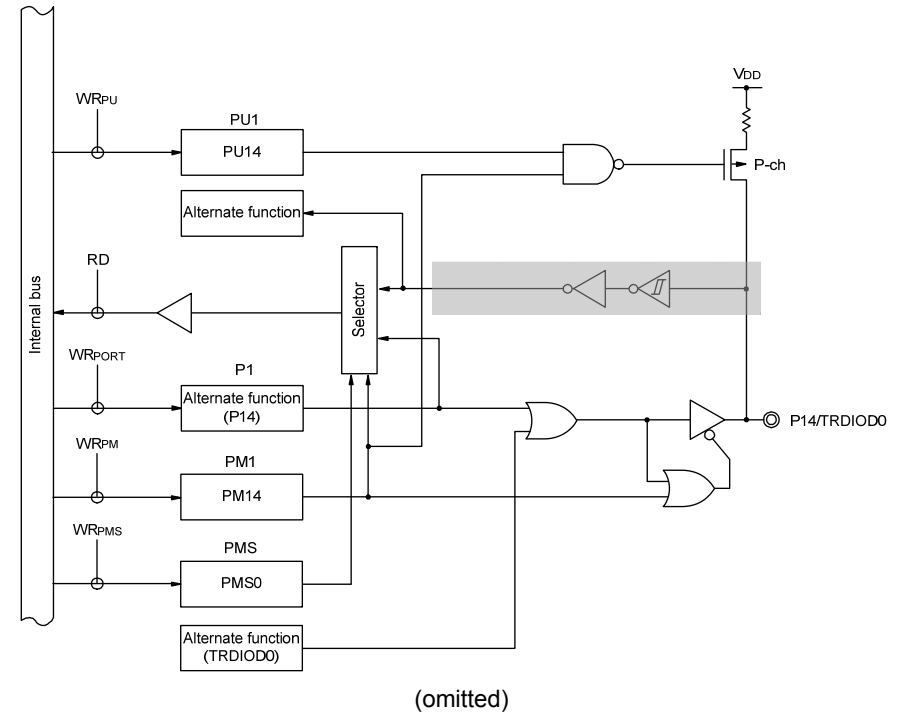
Incorrect:

Figure 4 - 7 Block Diagram of P14



Correct:

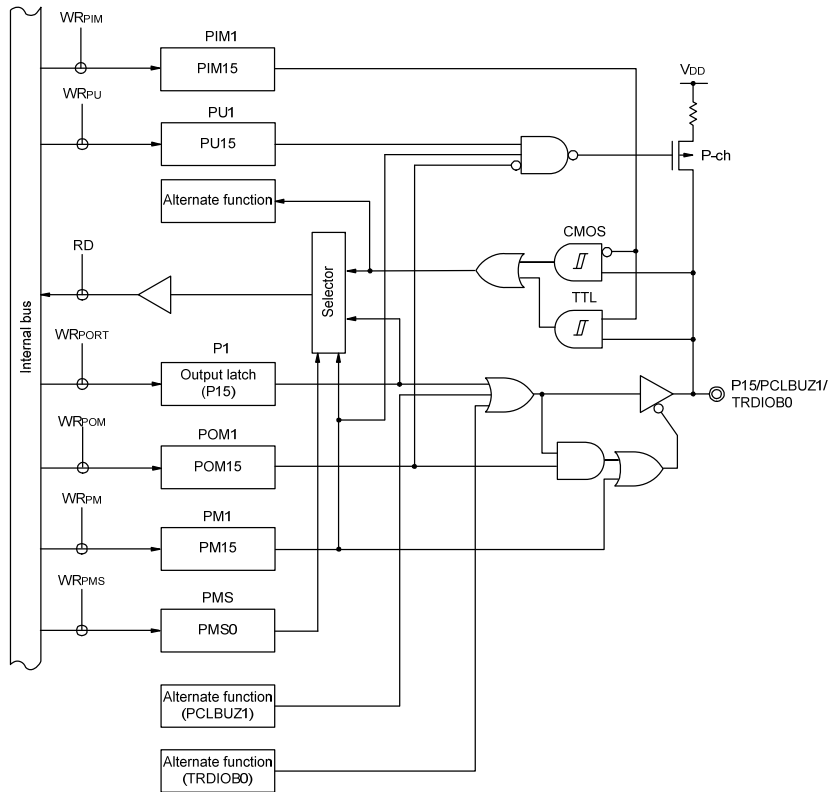
Figure 4 - 7 Block Diagram of P14



5. 4.2.2 Port 1 Figure 4-8 Pin Block Diagram of P15 (Page 80)

Old:

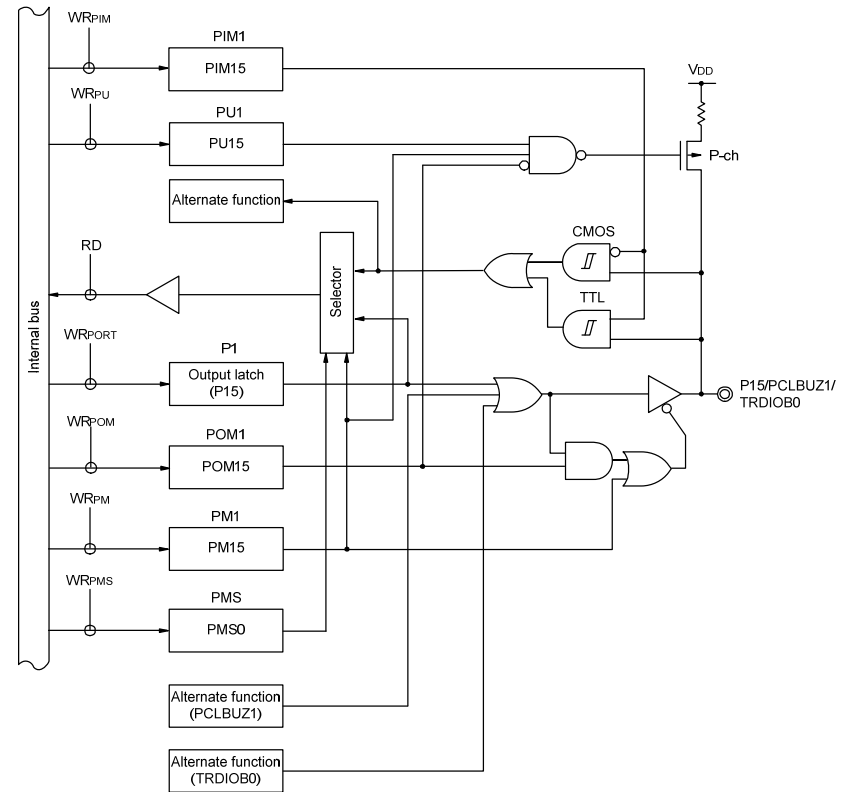
Figure 4 - 8 Block Diagram of P15



(omitted)

New:

Figure 4 - 8 Block Diagram of P15



Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

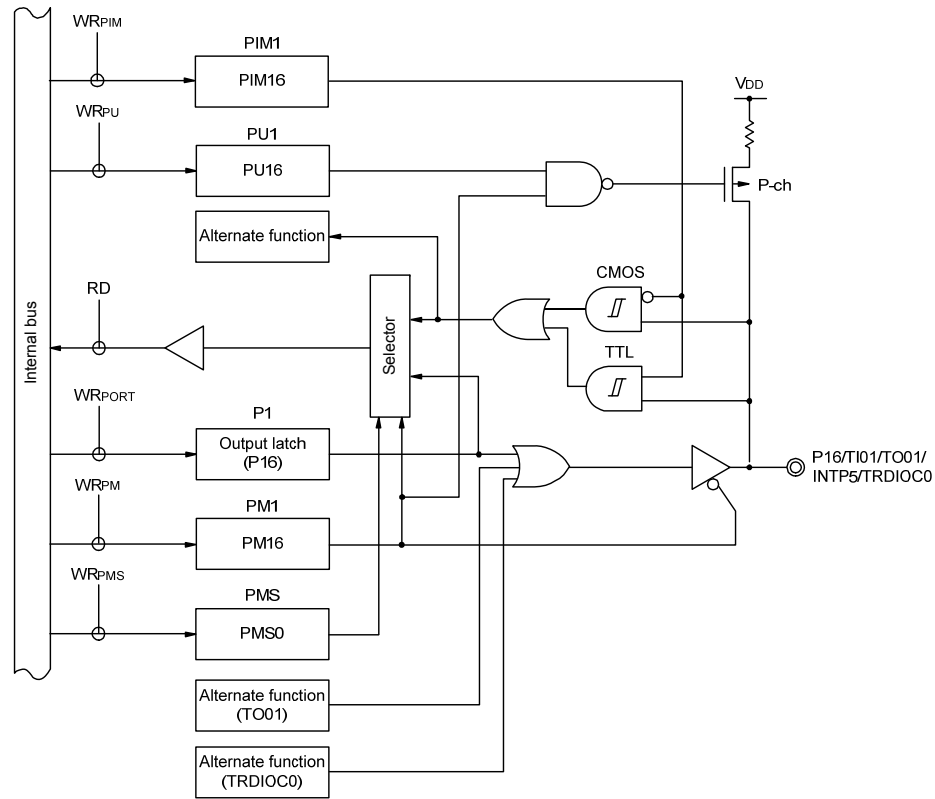
Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, electric power may increase in the case of high level input. It is recommended to input a low level to prevent increase of the electric power.

(omitted)

6. 4.2.2 Port 1 Figure 4-9 Pin Block Diagram of P16 (Page 81)

Old:

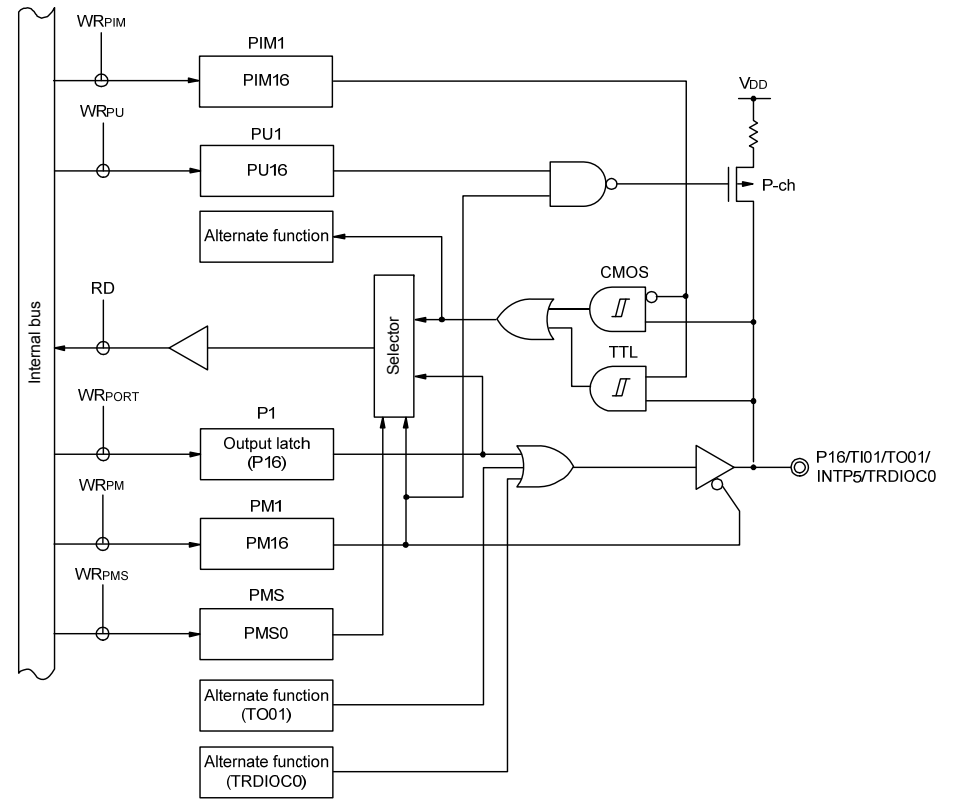
Figure 4 - 9 Block Diagram of P16



(omitted)

New:

Figure 4 - 9 Block Diagram of P16



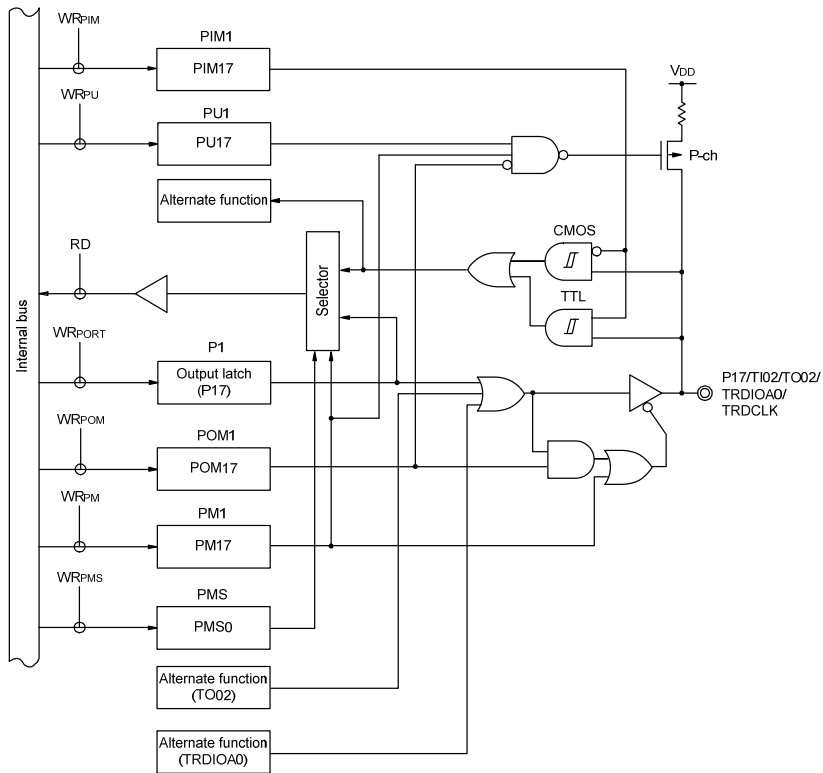
Caution Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, electric power may increase in the case of high level input. It is recommended to input a low level to prevent increase of the electric power.

(omitted)

7. 4.2.2 Port 1 Figure 4-10 Pin Block Diagram of P17 (Page 82)

Old:

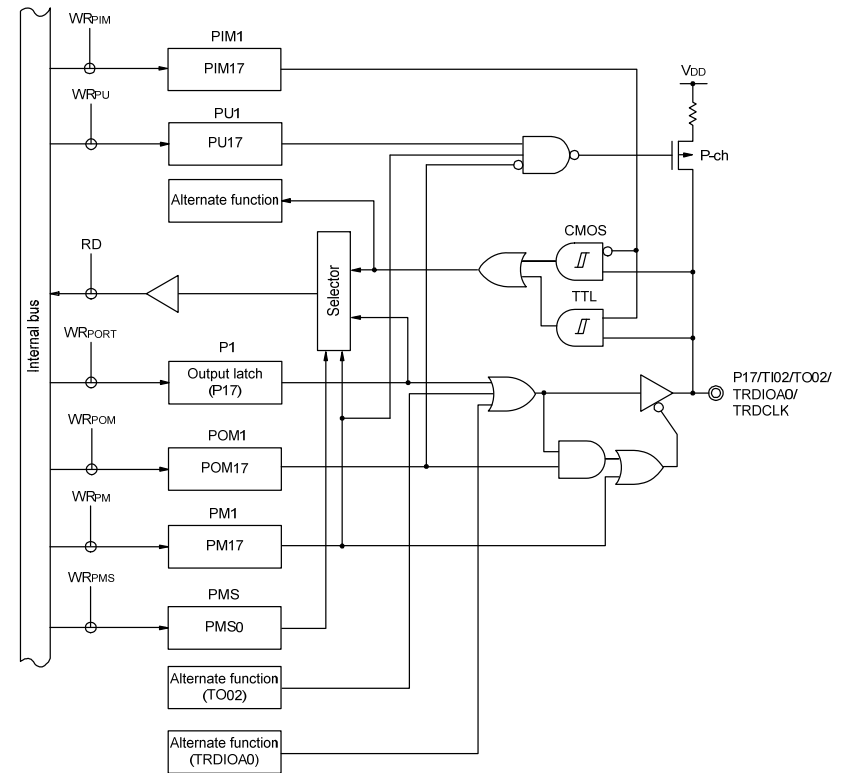
Figure 4 - 10 Block Diagram of P17



(omitted)

New:

Figure 4 - 10 Block Diagram of P17



Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

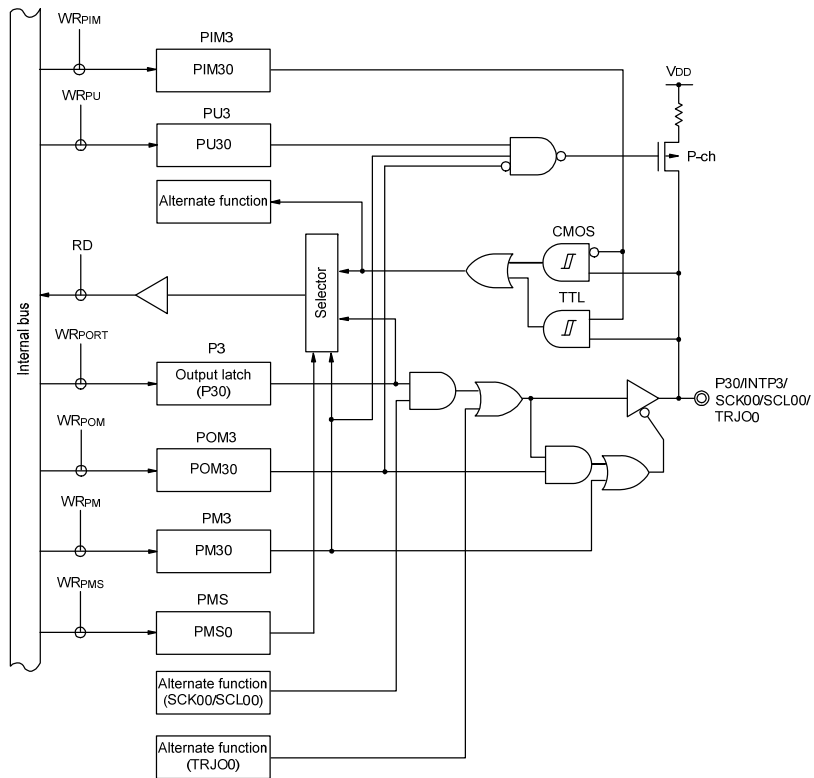
Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, electric power may increase in the case of high level input. It is recommended to input a low level to prevent increase of the electric power.

(omitted)

8. 4.2.4 Port 3 Figure 4-12 Pin Block Diagram of P30 (Page 86)

Old:

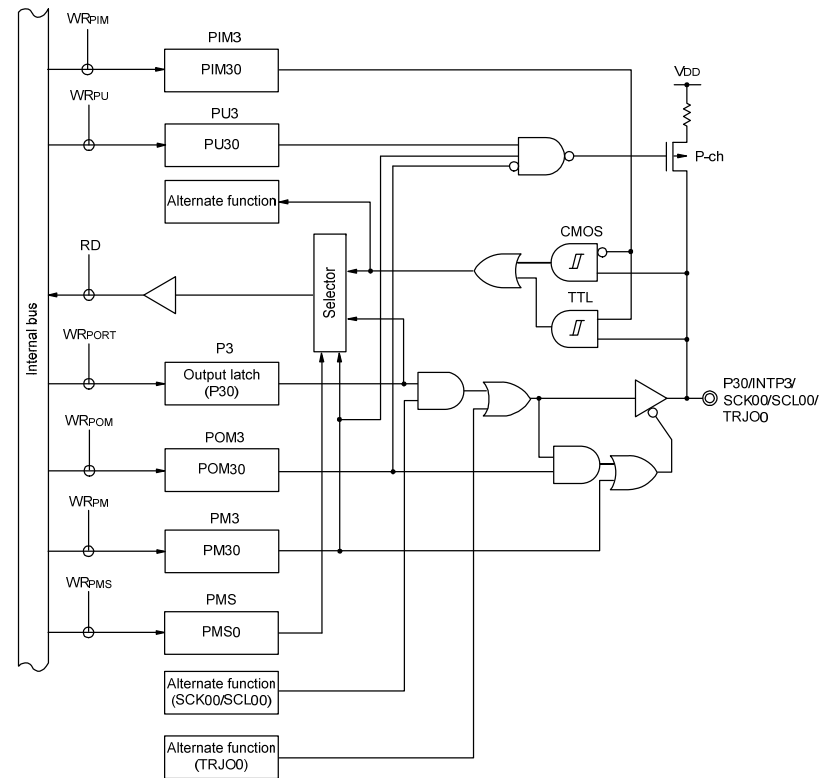
Figure 4 - 12 Block Diagram of P30



(omitted)

New:

Figure 4 - 12 Block Diagram of P30



Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

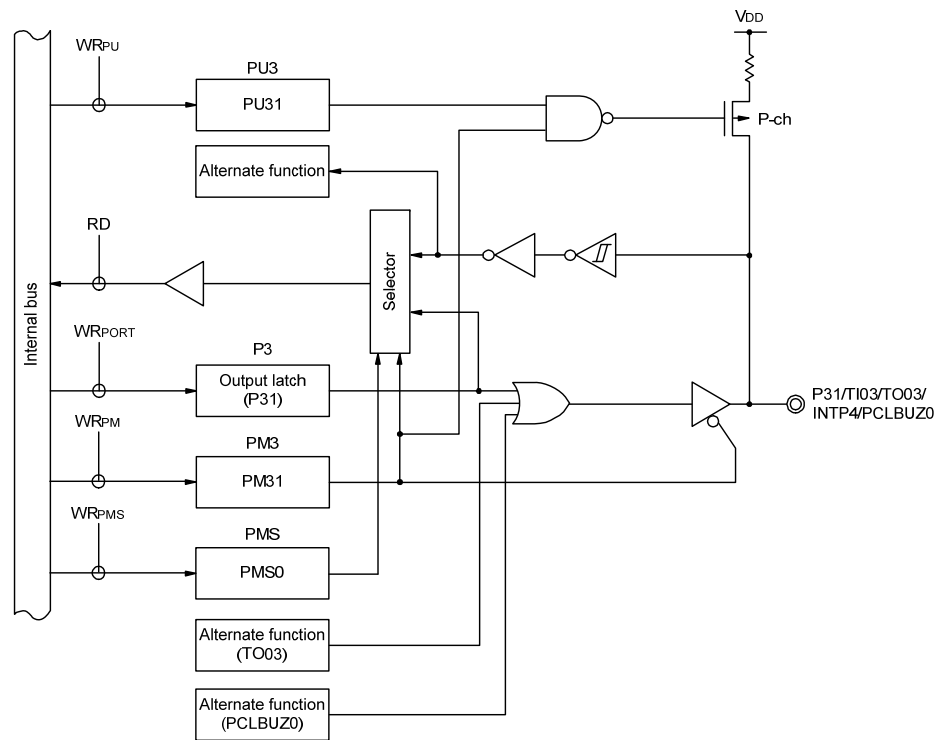
Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, electric power may increase in the case of high level input. It is recommended to input a low level to prevent increase of the electric power.

(omitted)

9. 4.2.4 Port 3 Figure 4-13 Pin Block Diagram of P31 (Page 87)

Incorrect:

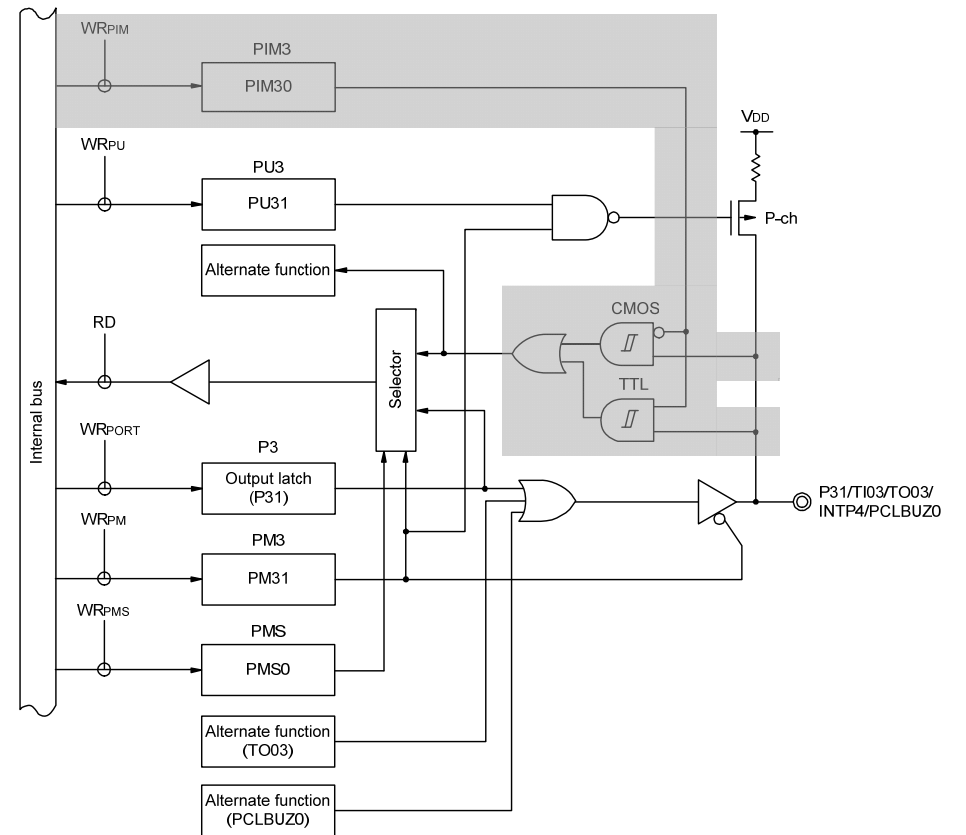
Figure 4 - 13 Block Diagram of P31



(omitted)

Correct:

Figure 4 - 13 Block Diagram of P31



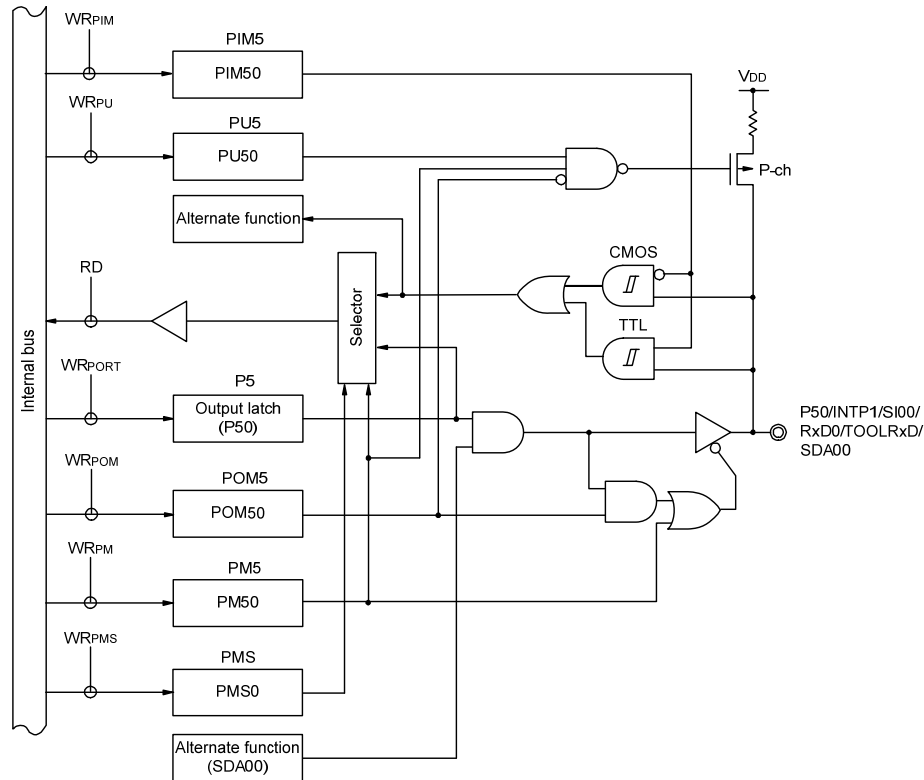
Caution Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, electric power may increase in the case of high level input. It is recommended to input a low level to prevent increase of the electric power.

(omitted)

10. 4.2.6 Port 5 Figure 4-16 Pin Block Diagram of P50 (Page 92)

Old:

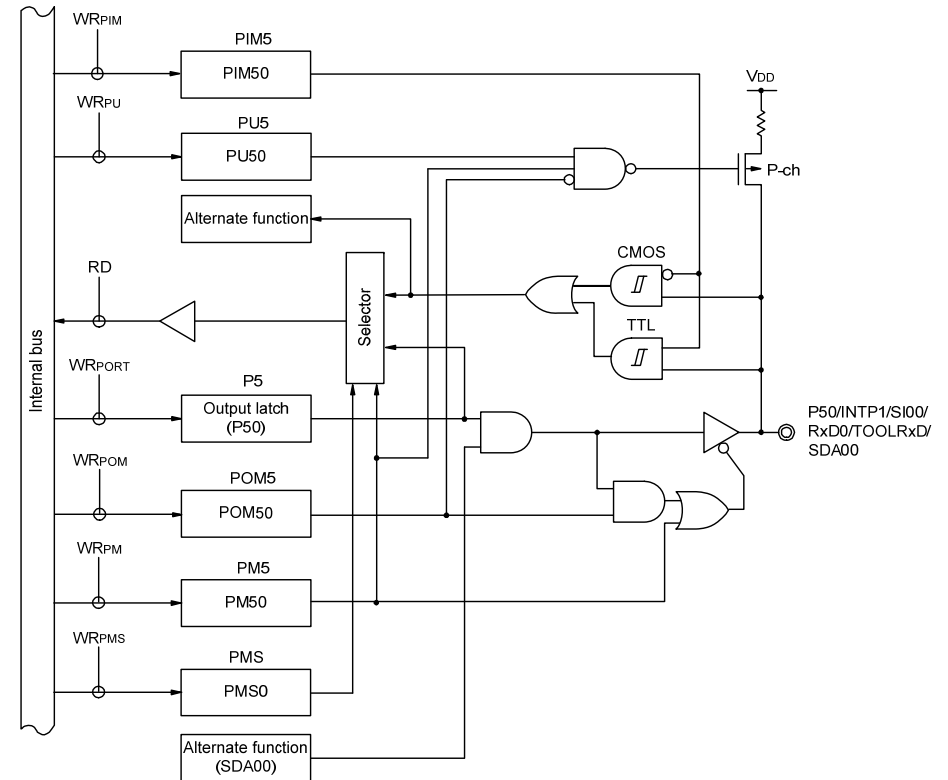
Figure 4 - 16 Block Diagram of P50



(omitted)

New:

Figure 4 - 16 Block Diagram of P50



Caution 1. A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

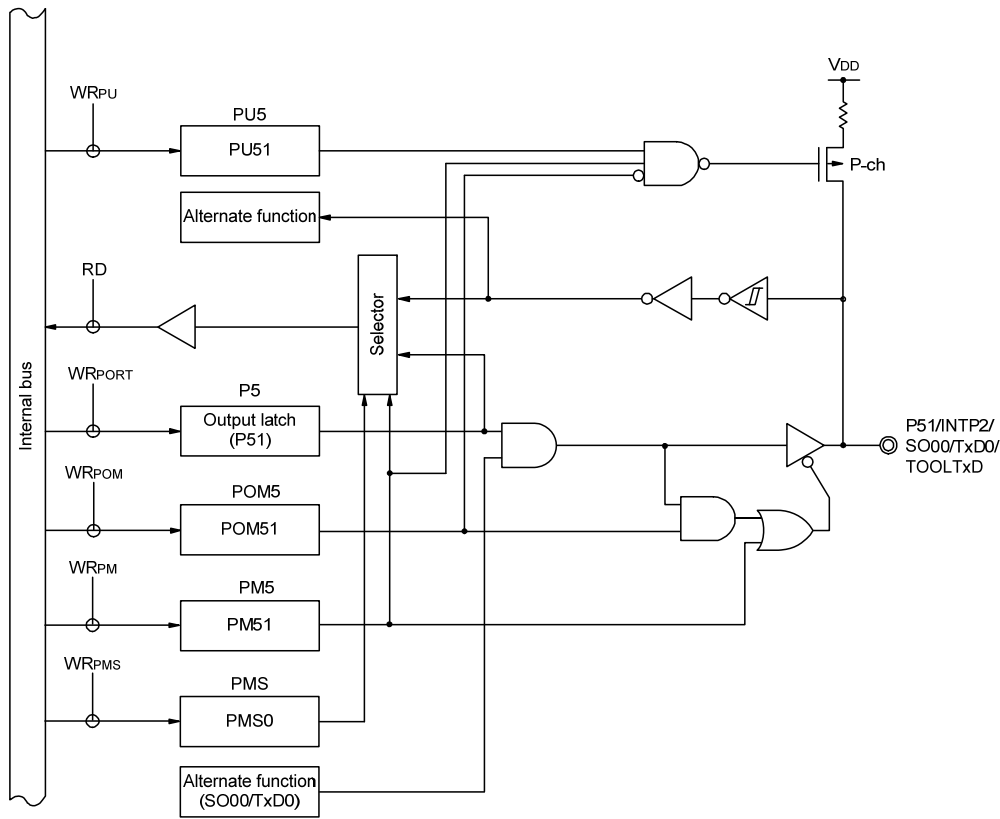
Caution 2. Because of TTL input buffer structure, if the port input mode register (PIMx) is set in TTL input buffer, electric power may increase in the case of high level input. It is recommended to input a low level to prevent increase of the electric power.

(omitted)

11. 4.2.6 Port 5 Figure 4-17 Pin Block Diagram of P51 (Page 93)

Old:

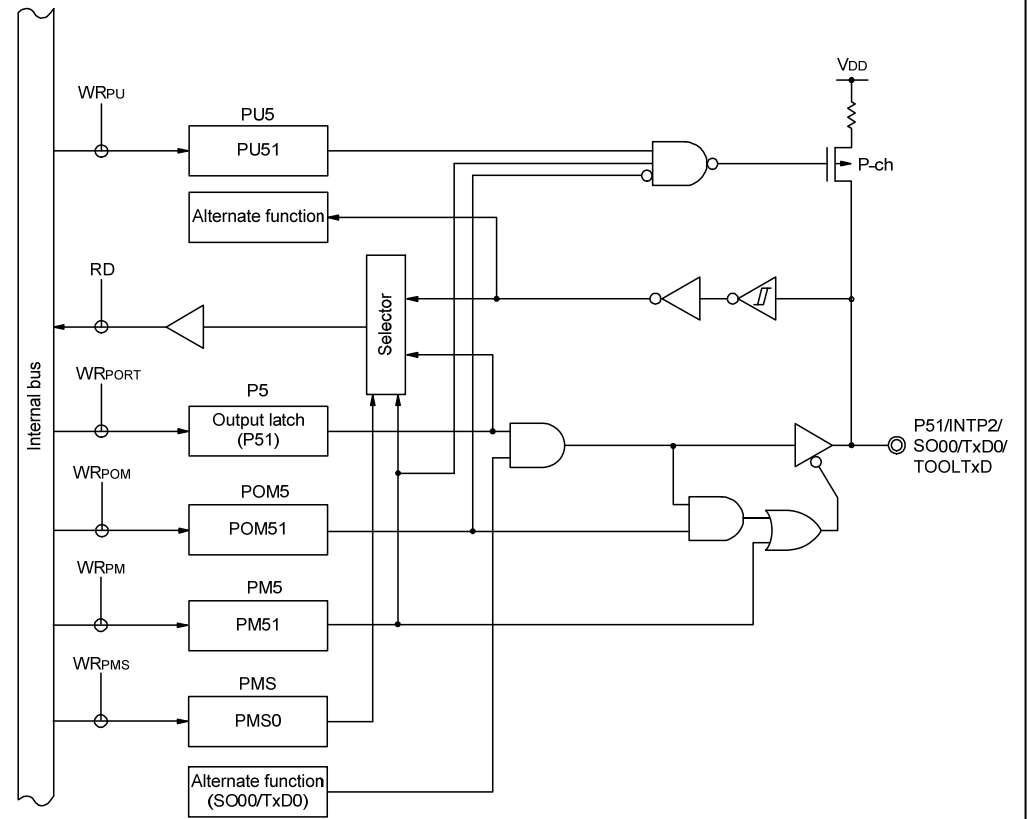
Figure 4 - 17 Block Diagram of P51



(omitted)

New:

Figure 4 - 17 Block Diagram of P51



Caution A through current may flow through if the pin is in the intermediate potential, because the input buffer is also turned on when the pin is in N-ch open-drain output mode by port output mode register (POMx).

(omitted)

12. 8.3.9 Timer RD output control register (TRDOCR)

Figure 8 - 12 Format of Timer RD output control register (TRDOCR)

[Reset Synchronous PWM Mode, Complementary PWM Mode]

Old:

Nothing

New:

Figure 8 - 12 Format of Timer RD output control register (TRDOCR)

[Reset Synchronous PWM Mode, Complementary PWM Mode]

Address: F0269H After Reset: 00H ^{Note 1} R/W

Symbol	7	6	5	4	3	2	1	0
TRDOCR	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0

TOD1, TOC1, TOB1, TOA1, TOD0, TOB0, TOA0	Setting these bits to 1 is invalid in the reset synchronous PWM mode and complementary PWM mode. Be sure to set these bits to 0. In the reset synchronous PWM mode and complementary PWM mode, the setting of the OLS1 and OLS0 bits in TRDFCR determine the initial level independently of the setting in these bits.
---	--

TOC0	TRDIOC1 initial output level select ^{Note 2}
0	Initial output L
1	Initial output H

In the reset synchronous PWM mode, the output is inverted every PWM period.
In complementary PWM mode, the output is inverted every 1/2 PWM period.

Note 1. The value after reset is undefined when FRQSEL4 = 1 in the user option byte (000C2H) and TRD0EN = 0 in the PER1 register. If it is necessary to read the initial value, set fCLK to fIH and TRD0EN = 1 before reading.

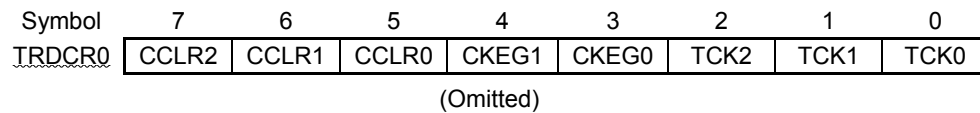
Note 2. If the pin function is set for waveform output, the initial output level is output when the TRDOCR register is set.

13. 8.3.11 Timer RD control register i (TRDCRi) (i = 0 or 1)
Figure8-18 Format of Timer RD control register 0 (TRDCR0)
[Complementary PWM Mode](page 313)

Incorrect:

Figure 8 - 18 Format of Timer RD control register 0 (TRDCR0)
 [Complementary PWM Mode]

Address: F0270H After Reset: 00H^{Note 1} R/W

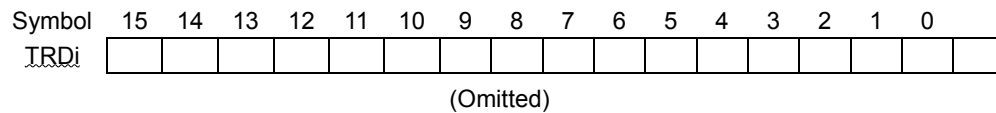


14. 8.3.18 Timer RD counter i (TRDi) (i = 0 or 1)
Figure 8 - 31 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Reset Synchronous PWM Mode and PWM3 Mode](Page 328)

Incorrect:

Figure 8 - 31 Format of Timer RD counter i (TRDi) (i = 0 or 1)
 [Reset Synchronous PWM Mode and PWM3 Mode]

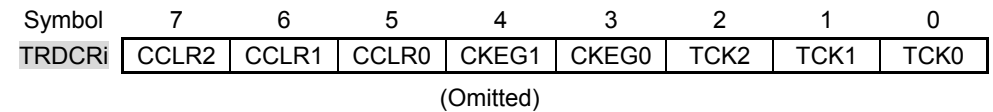
Address: F0276H (TRD0), F0286H (TRD1) After Reset: 0000H^{Note} R/W



Correct:

Figure8-19 Format of Timer RD control register i (TRDCRi) (i = 0 or 1)
 [Complementary PWM Mode]

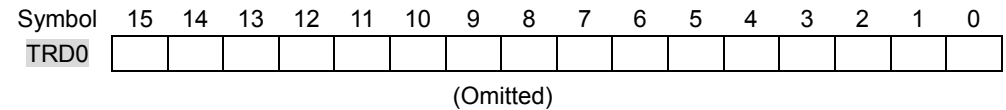
Address: F0270H (TRDCR0), F0280H (TRDCR1) After Reset: 00H^{Note 1} R/W



Correct:

Figure 8 - 32 Format of Timer RD counter 0 (TRD0)
 [Reset Synchronous PWM Mode and PWM3 Mode]

Address: F0276H (TRD0) After Reset: 0000H^{Note} R/W



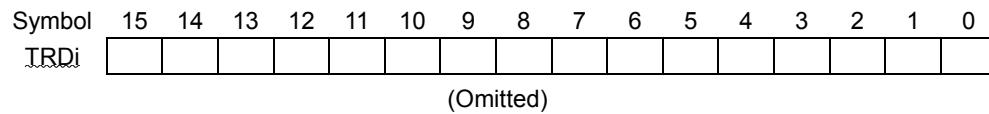
15. 8.3.18 Timer RD counter i (TRDi) (i = 0 or 1)

Figure 8 - 32 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Complementary PWM Mode (TRD0)] (Page 328)

Incorrect:

Figure 8 - 32 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Complementary PWM Mode (TRD0)]

Address: F0276H (TRD0), F0286H (TRD1) After Reset: 0000H^{Note} R/W



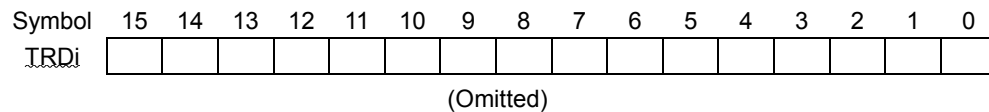
16. 8.3.18 Timer RD counter i (TRDi) (i = 0 or 1)

Figure 8 - 33 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Complementary PWM Mode (TRD1)](Page 329)

Incorrect:

Figure 8 - 33 Format of Timer RD counter i (TRDi) (i = 0 or 1)
[Complementary PWM Mode (TRD1)]

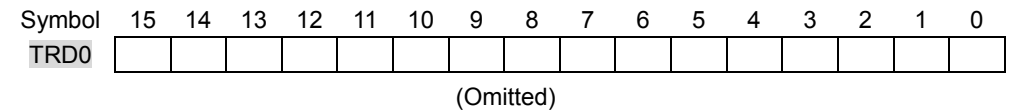
Address: F0286H (TRD1) After Reset: 0000H^{Note} R/W



Correct:

Figure 8 - 33 Format of Timer RD counter 0 (TRD0)
[Complementary PWM Mode (TRD0)]

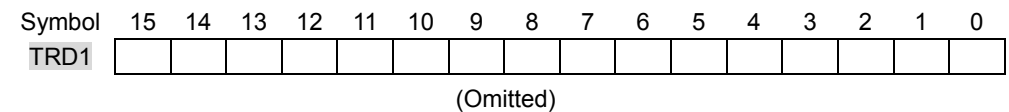
Address: F0276H (TRD0) After Reset: 0000H^{Note} R/W



Correct:

Figure 8 - 34 Format of Timer RD counter 1 (TRD1)
[Complementary PWM Mode (TRD1)]

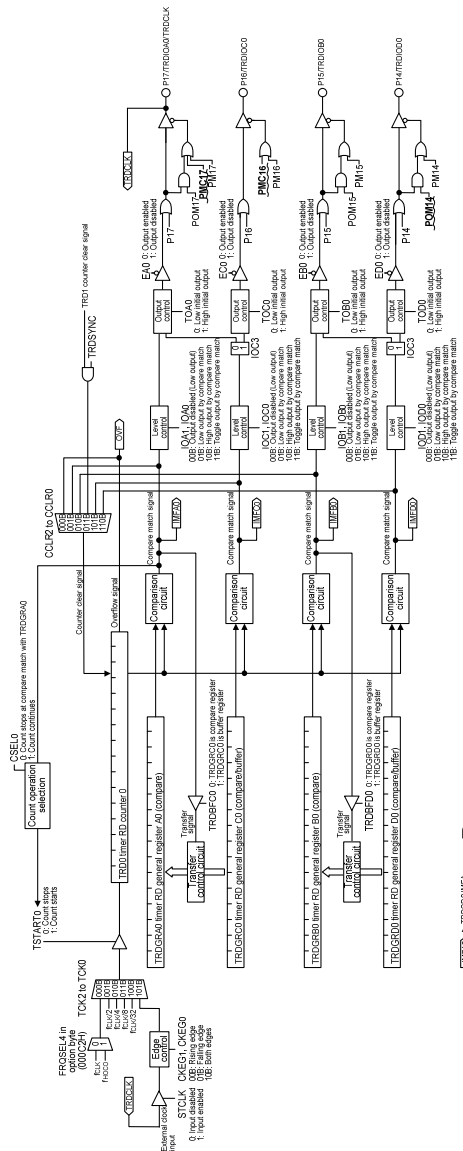
Address: F0286H (TRD1) After Reset: 0000H^{Note} R/W



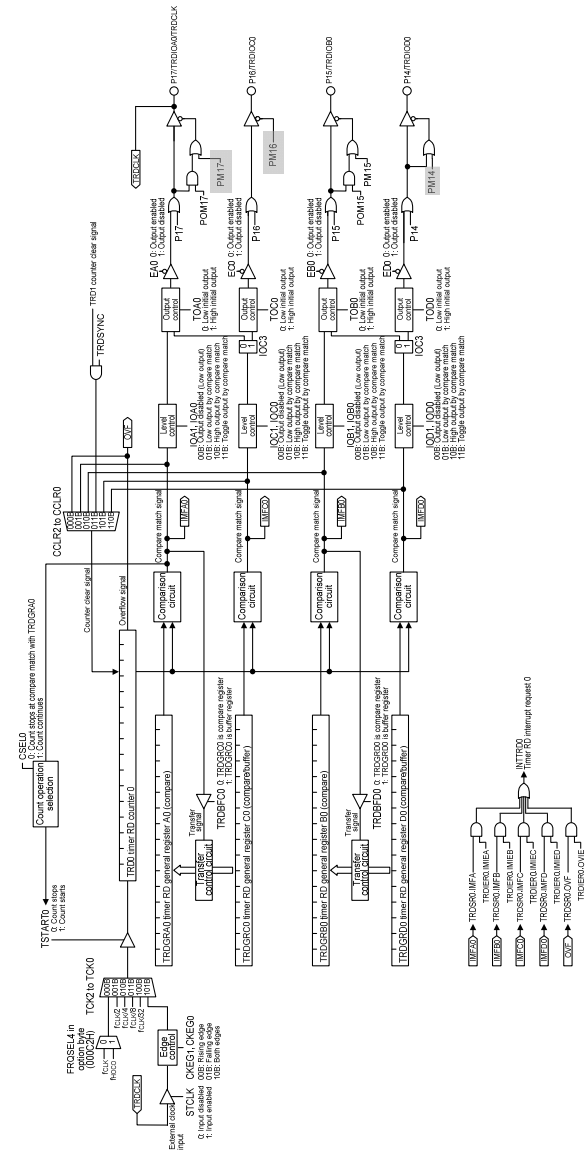
17. 8.4.8 Output compare function

Figure 8 - 50 Block Diagram of Output Compare Function (Page 355)

Incorrect:

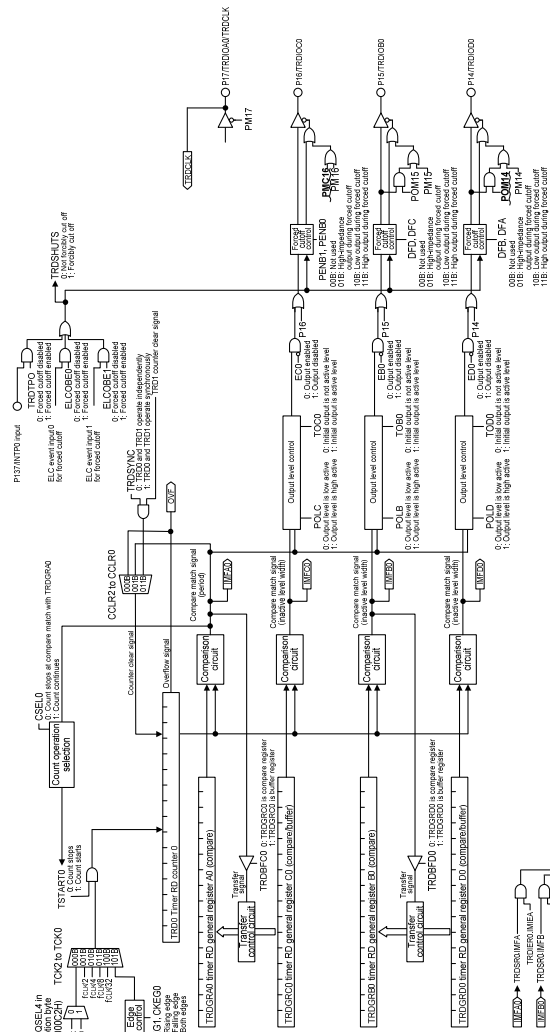


Correct:

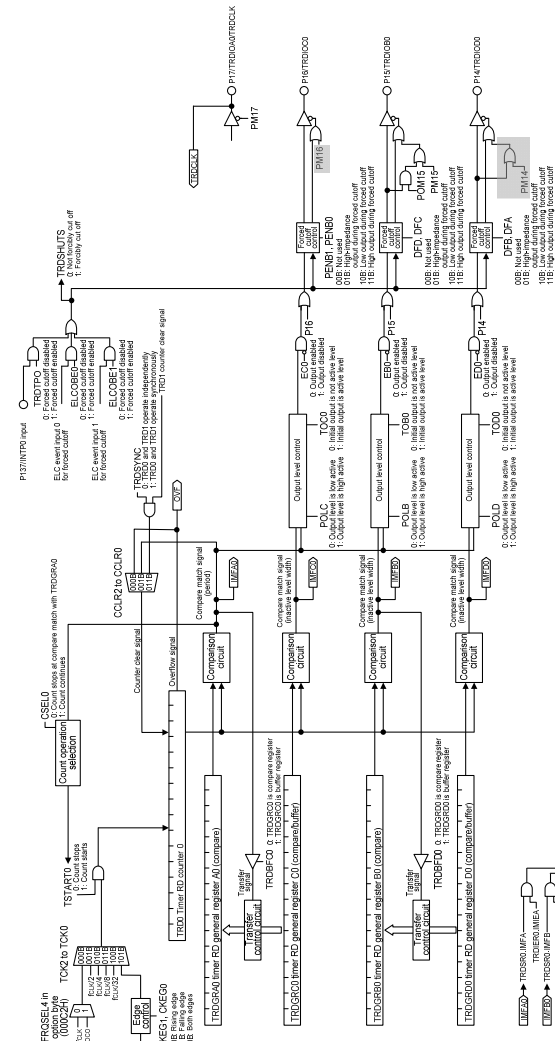


18. 8.4.9 PWM function
 Figure 8 - 54 Block Diagram of PWM Function (Page 361)

Incorrect:

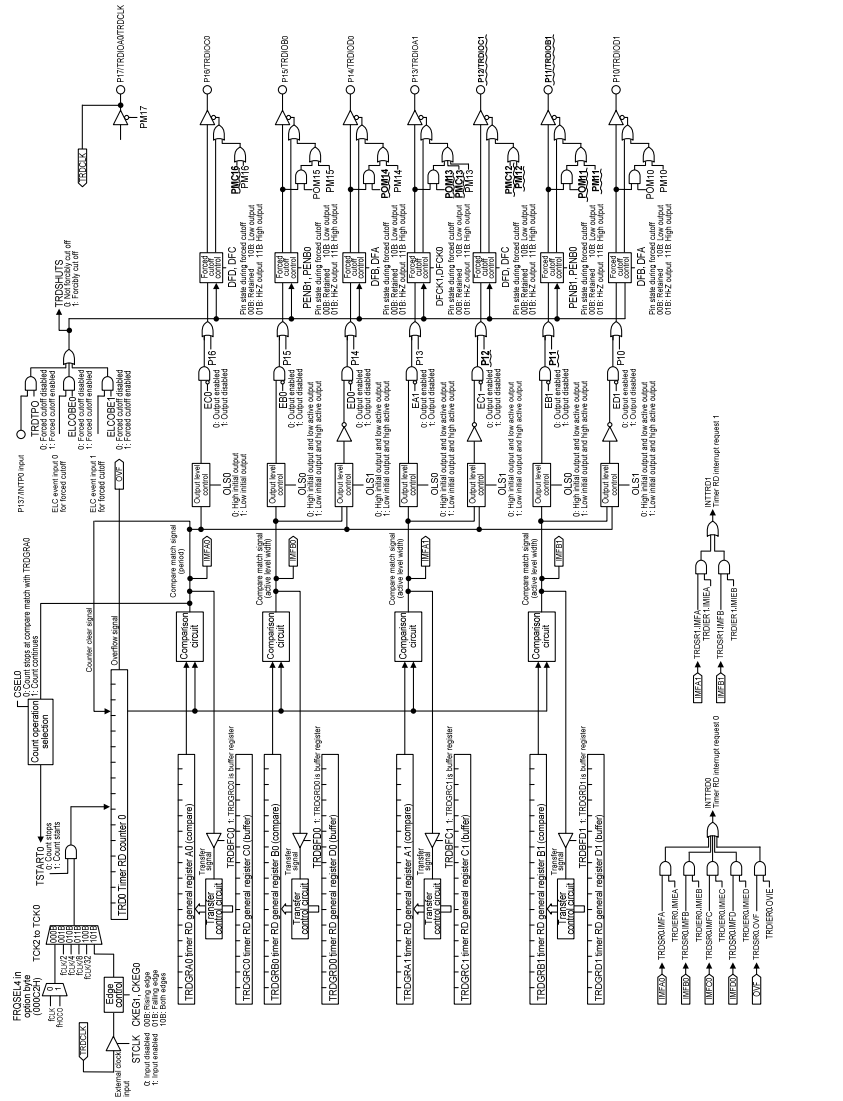


Correct:

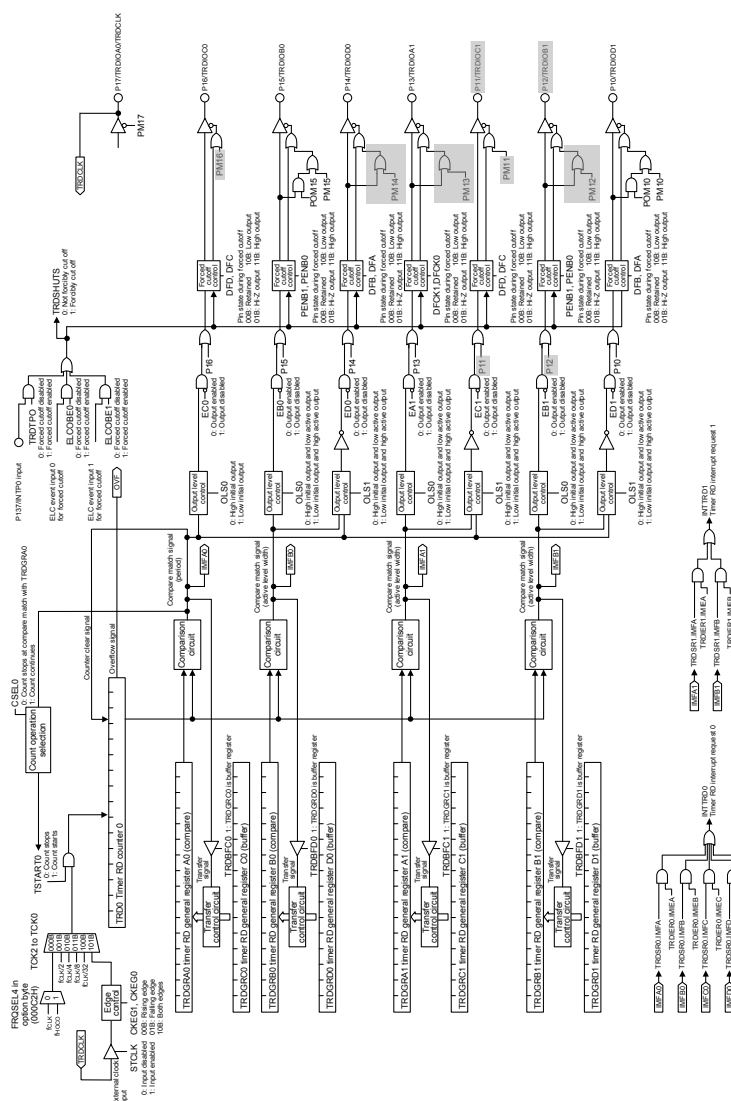


19. 8.4.10 Reset synchronous PWM mode
 Figure 8 - 57 Block Diagram of Reset Synchronous PWM Mode
 (Page 366)

Incorrect:



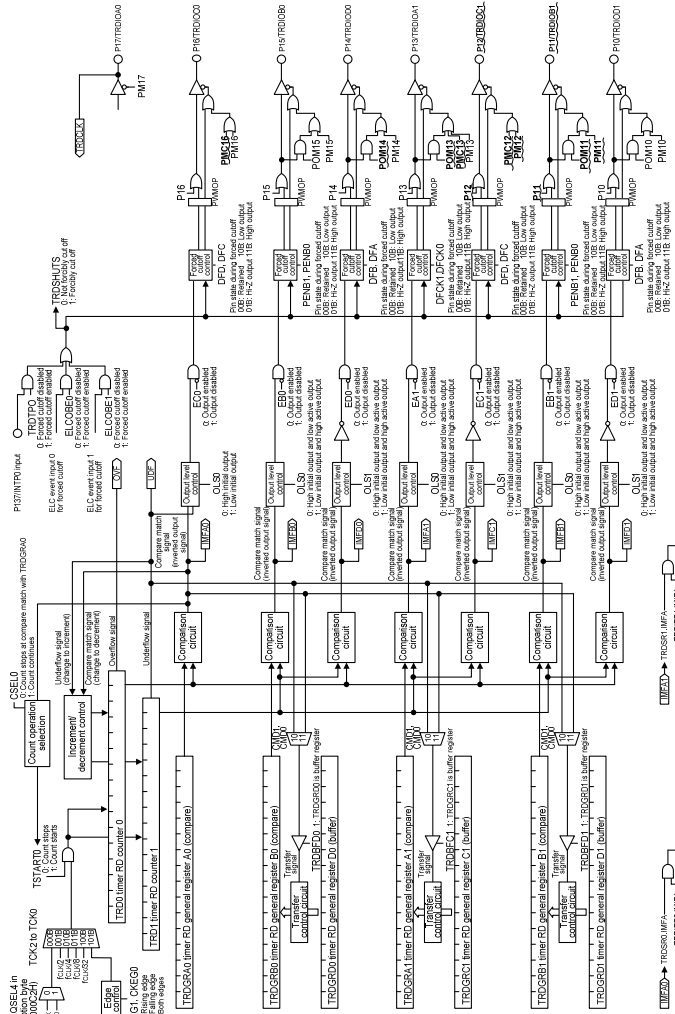
Correct:



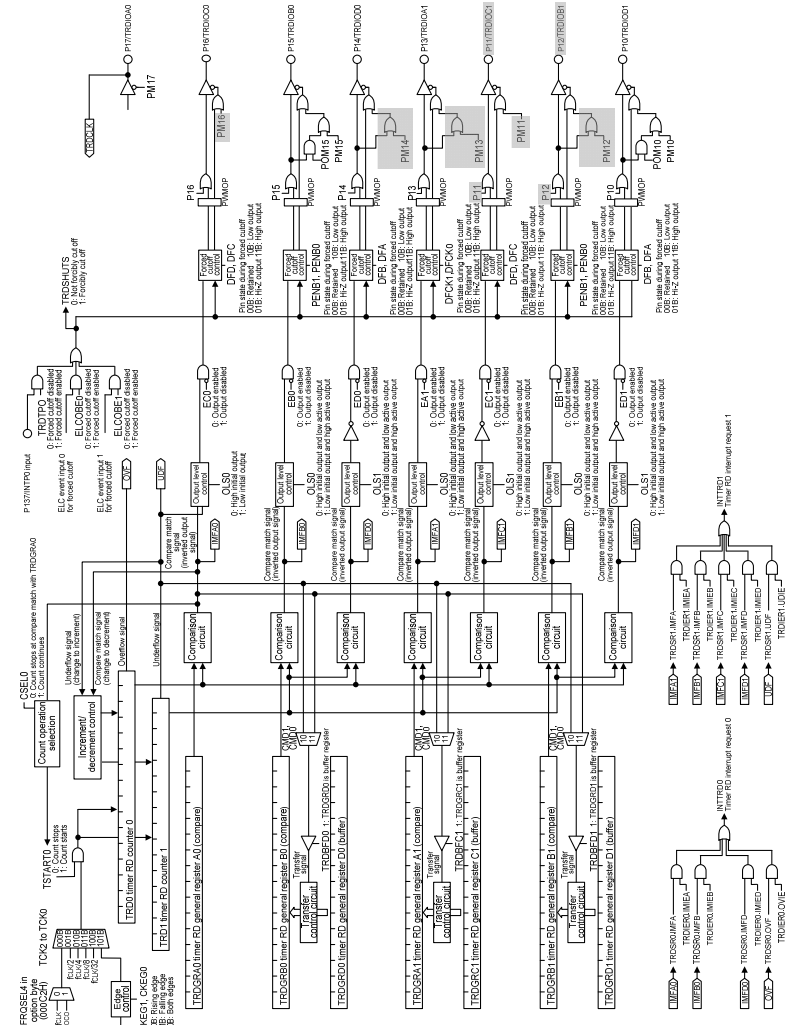
20. 8.4.11 Complementary PWM mode

Figure 8 - 59 Block Diagram of Complementary PWM Mode (Page 370)

Incorrect:



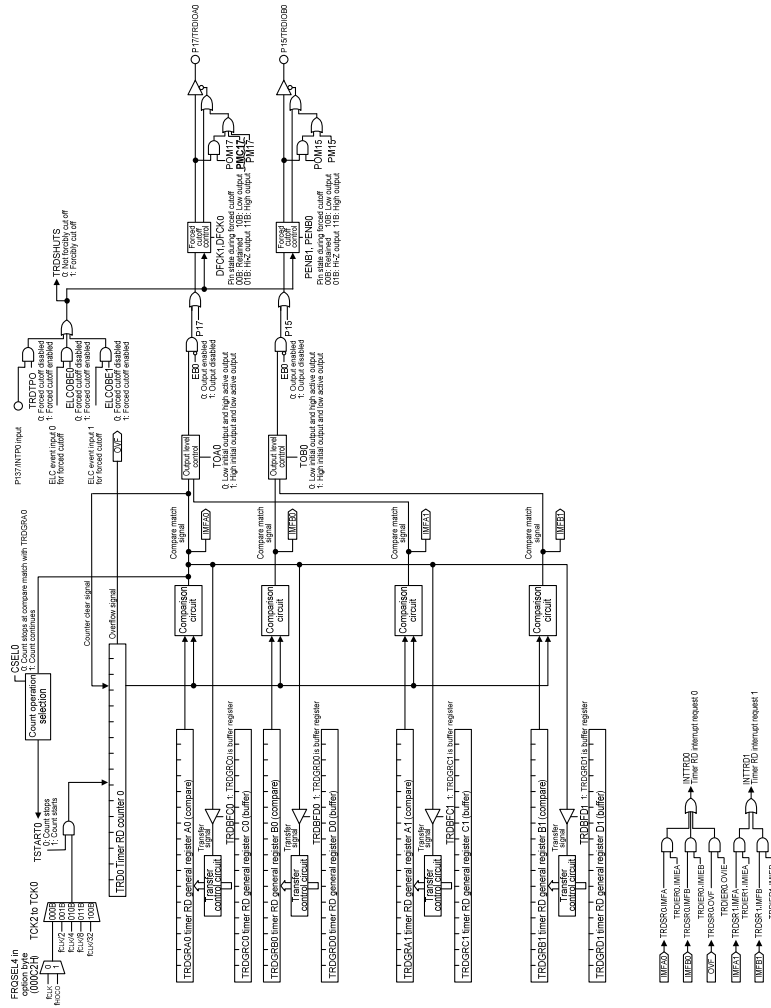
Correct:



21. 8.4.12 PWM3 mode

Figure 8 - 62 Block Diagram of PWM3 Mode (Page 375)

Incorrect:



Correct:

